Corrections to A three-dimensional simulation study of the performance of carbon nanotube field-effect transistors with doped reservoirs and realistic geometry

Gianluca Fiori
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
Giuseppe Iannaccone
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
Gerhard Klimeck
Network for Computational Nanotechnology, School of Electrical Engineering, Purdue University, West Lafayette

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Correspondence

Corrections to "A Three-Dimensional Simulation Study of the Performance of Carbon Nanotube Field-Effect Transistors With Doped Reservoirs and Realistic Geometry"

Gianluca Fiori, Giuseppe Iannaccone, and Gerhard Klimeck

The authors would like to make corrections to some results presented in [1], due to a wrong cutoff value assumed for the computation of the charge density. In particular, in order to avoid numerical problems associated with the integration of the local density of states, such a quantity had been taken to be equal to zero below the cutoff. This cutoff was removed from our code in 2006, and therefore, results in our subsequent papers on carbon nanotubes (CNTs) are correct [2]–[5]. Despite the fact that tests performed at the time seemed to demonstrate that simulations were correct, very recent simulations of ours, triggered by comments from Prof. D. L. Pulfrey on our obtained f_T values, have invalidated the already published results. Indeed, the assumed cutoff has resulted to be too high, leading to a charge underestimation in the channel, and f_T values are even higher than the maximum values expected for CNT devices [6].

This errata corrects Figs. 5–11, and 13 of the original paper and adds Fig. 14. Changed figures are presented with the same numbering as in that paper.

The results in Figs. 5 and 6 still show that CNT-FETs satisfy the International Roadmap for Semiconductors (ITRS) requirements for the $I_{\rm on}$ currents, even if the correct results differ from the previous ones by almost a factor of 4.5. As a consequence, the current per unit length is almost 1.2 times larger than the expected for high-performance devices at the 32-nm technology node (hp32: effective gate length equal to 13 nm) and is 1.1 times larger for the 22-nm technology node (hp22: effective gate length equal to 9 nm).

Since, after corrections, the $I_{\rm on}$ decreased and $I_{\rm off}$ increased, the $I_{\rm on}/I_{\rm off}$ ratio degraded, as shown in Fig. 7(b). As shown, ITRS requirements ($I_{\rm on}/I_{\rm off} \approx 7000$) are not satisfied. This however does not mean that CNTs have poor performance from the $I_{\rm on}/I_{\rm off}$ point of view. In Fig. 14, transfer characteristics for an $L = 10$ nm CNT device computed for different $V_{\rm DS}$ are shown. As can be noted, $I_{\rm off}$ decreases as drain-to-source voltages are decreased. As a consequence, it is possible to define, by means of gate workfunction tuning, a voltage window in which the $I_{\rm on}/I_{\rm off}$ ratio satisfies the ITRS requirements. For example, for $V_{\rm DS} = 0.6$ V, we obtain an $I_{\rm on}/I_{\rm off}$ ratio that is equal to 7200.

Since τ and f_T depend on $I_{\rm on}$ and g_m, Fig. 13 has to be corrected. In particular, the intrinsic delay is increased, while the cutoff frequencies decrease by almost a factor of four and are comparable with the analytical values found by Burke [7]. Compared to the ITRS requirements for the hp22-technology node, the obtained τ's are at least 2.3 times smaller.

Part of the corrected figures previously appeared in an International Electron Devices Meeting paper [8]. Corrections in these errata also apply to those results.

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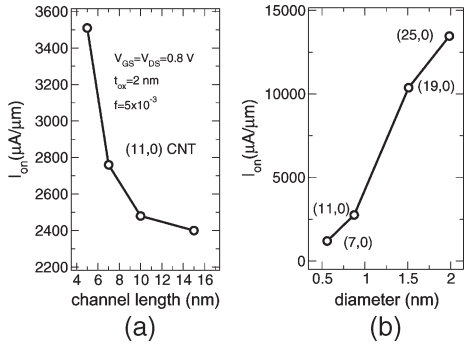

Fig. 5. (a) On-current per unit width as a function of the channel length for a double-gate CNT-FET (2-nm lateral dielectric between adjacent nanotubes). (b) $I_{\rm on}$ current per nanotube as a function of the nanotube diameter, for an $L = 7$ nm double-gate CNT-FET. $t_{\rm ox} = 2$ nm, and $f = 5 \times 10^{-3}$.

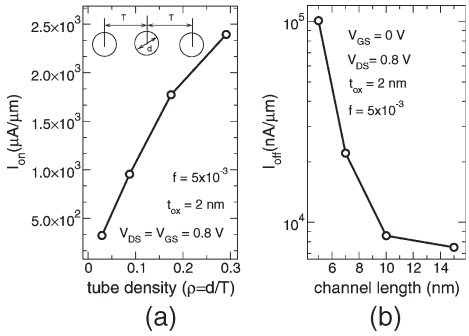

Fig. 6. (a) On-current as a function of the nanotube normalized-density per unit length $\rho = d/T$ for a double-gate CNT-FET with $L = 15$ nm. (b) Off-current as a function of the channel length for a double-gate CNT-FET.

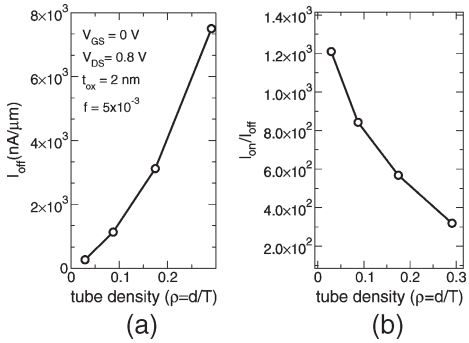

Fig. 7. (a) Off-current as a function of the nanotube normalized-density per unit length $\rho = d/T$ for a double-gate CNT-FET with $L = 15$ nm. (b) $I_{\rm on}/I_{\rm off}$ ratio as a function of the nanotube normalized-density per unit length $\rho = d/T$ for a double-gate CNT-FET with $L = 15$ nm.

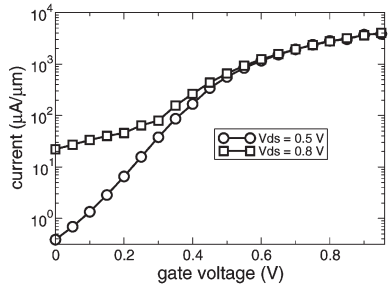

Fig. 9. Transfer characteristics for the double-gate CNT-FET with $L = 7$ nm, for $V_{\rm DS} = 0.5$ and 0.8 V; $t_{\rm ox} = 2$ nm, and $f = 5 \times 10^{-3}$.

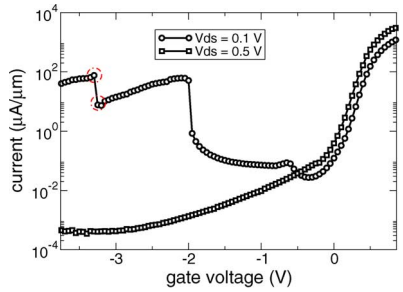

Fig. 10. Transfer characteristics for the double-gate CNT-FET with $L = 7$ nm, for $V_{\rm DS} = 0.5$ and 0.1 V; $t_{\rm ox} = 1$ nm, and $f = 5 \times 10^{-3}$.

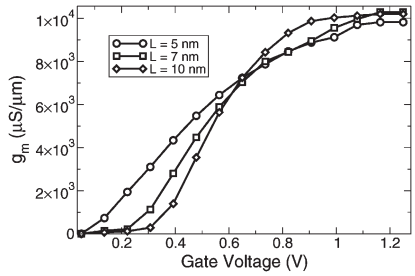

Fig. 11. Transconductance as a function of the gate voltage for double-gate CNT-FETs with different channel lengths: $L = 5$, 7, and 10 nm; $t_{\rm ox} = 2$ nm; $V_{\rm DS} = 0.8$ V; and $f = 5 \times 10^{-3}$.

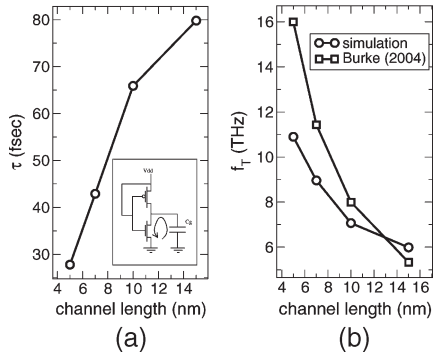

Fig. 13. (a) Inverse of the intrinsic device speed, defined as $\tau = C_G V_{\rm DD}/I_{\rm on}$ as a function of the channel length for double-gate CNT-FET, where $V_{\rm DD} = 0.8$ V and C_G is the gate capacitance. (b) Cutoff frequency as a function of the gate length, for the double-gate CNT-FET. $t_{\rm ox} = 2$ nm, and $f = 5 \times 10^{-3}$.

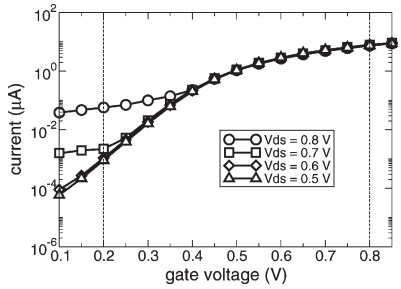

Fig. 14. Transfer characteristics for an $L = 10$ nm channel device, computed for different $V_{\rm DS}$.

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REFERENCES

[1] G. Fiori, G. Iannaccone, and G. Klimeck, "A three-dimensional simulation study of the performance of carbon nanotube field effect transistors with doped reservoirs and realistic geometry," *IEEE Trans. Electron Devices*, vol. 53, no. 8, pp. 1782–1788, Aug. 2006.

[2] G. Fiori and G. Iannaccone, "Threshold voltage dispersion and impurity scattering limited mobility in carbon nanotube field effect transistors with randomly doped reservoirs," in *Proc. ESSDERC*, Montreux, Switzerland, 2006, pp. 202–205.

[3] G. Fiori, G. Iannaccone, and G. Klimeck, "Coupled mode space approach for the simulation of realistic carbon nanotube field-effect transistors," *IEEE Trans. Nanotechnol.*, vol. 6, no. 4, pp. 475–480, Jul. 2007.

[4] S. Poli, G. Fiori, S. Reggiani, A. Gnudi, and G. Iannaccone, "Tight-binding versus effective-mass modeling of carbon nanotube FETs," in *Proc. 8th Int. Conf. ULIS*, Leuven, Belgium, Mar. 15/16 2007, pp. 43–46.

[5] S. Koswatta, N. Neophytou, D. Kienle, G. Fiori, and M. S. Lundstrom, "Dependence of DC characteristics of CNT MOSFETs on bandstructure models," *IEEE Trans. Nanotechnol.*, vol. 5, no. 4, pp. 368–372, Jul. 2006.

[6] S. Hasan, S. Salahuddin, M. Vaidyanathan, and M. A. Alam, "High-frequency performance projections for ballistic carbon-nanotube transistors," *IEEE Trans. Nanotechnol.*, vol. 5, no. 1, pp. 14–22, Jan. 2006.

[7] P. J. Burke, "AC performance of nanoelectronics: Towards a ballistic THz nanotube transistor," *Solid State Electron.*, vol. 48, no. 10/11, pp. 1981–1986, Oct./Nov. 2004.

[8] G. Fiori, G. Iannaccone, and G. Klimeck, "Performance of carbon nanotube field effect transistors with doped source and drain extensions and arbitrary geometry," in *IEDM Tech. Dig.*, 2005, pp. 529–532.