# *Modeling of Tunnelling Currents in Hf-Based Gate Stacks as a Function of Temperature and Extraction of Material Parameters*

**Andrea Campera**
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
**Giuseppe Iannaccone**
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
**Felice Crupi**
Dipartimento di Elettronica, Informatica e Sistemistica, Università della Calabria

A. Campera, G. Iannaccone, F. Crupi, *Modeling of Tunnelling Currents in Hf-Based Gate Stacks as a Function of Temperature and Extraction of Material Parameters*, IIEEE Transactions on Electron Devices, **54**, 1, pp.83-89 (2007).

# Modeling of Tunnelling Currents in Hf-Based Gate Stacks as a Function of Temperature and Extraction of Material Parameters

Andrea Campera, Giuseppe Iannaccone, *Member, IEEE*, and Felice Crupi

***Abstract*—In this paper, we show that through electrical characterization and detailed quantum simulations of the capacitance–voltage and current–voltage ($I$–$V$) characteristics, it is possible to extract a series of material parameters of alternative gate dielectrics. We have focused on $HfO_2$ and $HfSi_XO_YN_Z$ gate stacks and have extracted information on the nature of localized states in the dielectric responsible for a trap-assisted tunneling (TAT) current component and for the temperature behavior of the $I$–$V$ characteristics. Simulations are based on a one-dimensional Poisson-Schrödinger solver capable to provide the pure tunneling current and TAT component. Energy and capture cross section of traps responsible for TAT current have been extracted.**

***Index Terms*—Gate leakage, high-$k$ dielectrics, trap-assisted tunneling (TAT), trap cross section.**

## I. Introduction

THE PRESENT research and development effort focused on replacing $SiO_2$ and SiON gate stacks with high dielectric permittivity (high-$k$) gate stacks is motivated by the need of increasing the gate capacitance per unit area as the device size shrinks while at the same time maintaining the leakage tunneling current under control. Among high-$k$ dielectrics, $HfO_2$ and its silicates—in particular hafnium silicate nitride ($HfSi_XO_YN_Z$)—are considered promising alternative gate dielectrics for CMOS technology at the 45-nm node and beyond [1]–[3]. In fact, as it is well known, high-$k$ dielectrics exhibit strongly suppressed gate tunneling current with respect to silicon oxide for the same gate capacitance: of a factor $10^5$ for $HfO_2$, and a factor $10^3$ for an $HfSi_XO_YN_Z$ stack [1]. Both materials have a rather large bandgap, about 6 eV for $HfO_2$ and 7 eV for $HfSi_XO_YN_Z$ [4], [5]. Bandgap is lower with respect to conventional $SiO_2$, but the increased thickness, in any case, causes an overall leakage current suppression.

Although significant reduction of gate leakage has been achieved, the nature of the stray currents and the frequently observed flatband voltage shift and voltage bias instability [1], [6], [7] need further investigation. The effect of polysilicon depletion, which will require the use of metal gates, and the reduced effective channel mobility are other important issues, which will become more critical with the shrinking of the physical dimensions.

The main aim of this paper is the understanding of the tunneling mechanisms through such dielectrics. In order to do this, we have investigated the current–voltage ($I$–$V$) characteristics as a function of temperature. We show that the temperature dependence of $I$–$V$ characteristics in $HfO_2$ can be explained in terms of a microscopic model of trap-assisted tunneling (TAT) based on a temperature-dependent cross section. Comparison of experiments with the results of our model allows us to exclude that relevant traps for transport are localized at the $HfO_2$ interfaces (confirming some experiments [8]).

This paper is organized as follows: In Section II, we describe the structures under investigation. In Section III, we briefly discuss the Poisson-Schrödinger solver and how the tunneling current components are obtained. In Sections IV and V, we compare experimental and theoretical capacitance–voltage ($C$–$V$) and current density–voltage ($J$–$V$) characteristics, respectively, and extract the relevant physical parameters of the materials. In Section VI, we discuss in some more detail the transport model we have used to explain the temperature-dependent transport in $HfO_2$ and $HfSi_XO_YN_Z$ and the comparison with experiments, and finally, we will draw our conclusions.

## II. Experiments

We have experimentally investigated $HfO_2$ and $HfSi_XO_YN_Z$ gate stacks; the physical parameters of Hf-based dielectrics depend on the fabrication process and on the specific resulting composition. Indeed, for example, the dielectric constant of $HfSi_XO_YN_Z$ depends on the nitrogen and hafnium molar fraction in the high-$k$ layer [2], [9]. Therefore, it is important to extract with sufficient precision the physical parameters of the high-$k$ layer, as we shall do by comparing experiments with simulations. We have considered three different gate stacks, consisting of an interfacial layer (we assume it to be $SiO_2$ for the $HfO_2$ gate stack and SiON for the $HfSi_XO_YN_Z$ gate stack) of thickness $t_{\rm int}$ in contact with the silicon substrate, and of an high-$k$ layer of thickness $t_{{\rm high}-k}$ covered by an $n^+$ poly-silicon gate. The gate dielectrics have been deposited by a metal-organic chemical vapor deposition after an

Manuscript received January 3, 2006; revised October 11, 2006. This work was supported in part by the SINANO Network of Excellence under EU Contract 506844, by the MIUR-PRIN project "Alternative models and architectures for nanoMOSFETs," and by the EU PullNANO Integrated Project through the IU.NET consortium under Contract 026828. The review of this paper was arranged by Editor S. Datta.

A. Campera and G. Iannaccone are with the Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa, 56126 Pisa, Italy (e-mail: andrea.campera@iet.unipi.it; g.iannaccone@iet.unipi.it).

F. Crupi is with Dipartimento di Elettronica, Informatica e Sistemistica, Università della Calabria, 87036 Arcavacata di Rende (CS), Italy (e-mail: crupi@unical.it).

Digital Object Identifier 10.1109/TED.2006.887202

TABLE I
GATE STACK STRUCTURES CONSIDERED

| | Structure *a* | Structure *b* | Structure *c* |
|---|---|---|---|
| high-*k* material | $HfO_2$ | $HfSi_XO_YN_Z$ | $HfSi_XO_YN_Z$ |
| $t_{high\text{-}k}$ | 4 nm | 2 nm | 1 nm |
| $t_{int}$ | 1nm ($SiO_2$) | 1 nm (SiON) | 1 nm (SiON) |
| EOT | 1.63 nm | 1.7 nm | 1.35 nm |

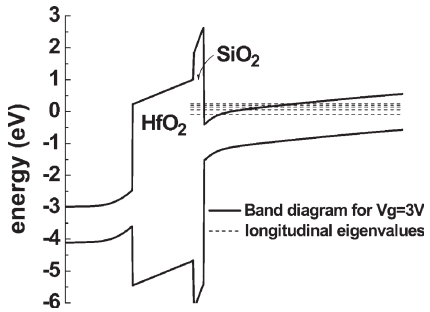


Fig. 1. Band diagram and two-dimensional subband energies obtained from the 1-D Poisson-Schrödinger solver for structure $a$ (4 nm of $HfO_2$ and 1 nm of $SiO_2$) with an applied gate voltage of 3 V.

IMEC-clean process. In all three cases, the substrate is p-doped with $N_A = 5 \cdot 10^{23}$ m$^{-3}$. Details on the layer structures are shown in Table I.

$C$–$V$ characteristics have been measured for capacitors of area 70 × 70 $\mu$m, and $I$–$V$ characteristics have been measured for n-MOSFETs with width of 10 $\mu$m and gate length of 5 $\mu$m.

## III. ONE-DIMENSIONAL (1-D) POISSON-SCHRÖDINGER SOLVER

In thin equivalent oxide thickness MOS structures, such as those we are considering, polysilicon depletion and finite density of states in the bulk must be taken into account. To simulate these structures, we have used a 1-D self-consistent Poisson-Schrödinger solver that takes into account quantum confinement at the emitting region (being it the polysilicon gate or the substrate, depending on bias), mass anisotropy in silicon conduction band, light and heavy holes, wave function penetration in the oxide. For simplicity, bands are parabolic. The band profile is computed with the quasi-equilibrium approximation, i.e., assuming that the tunneling current is so low that the dielectric separates in two regions in local equilibrium with two different Fermi energies.

From the band profile (e.g., the one shown in Fig. 1), we can compute the tunneling current per unit area, that is given by [10]

$$J = \frac{2qk_BT}{\pi\hbar^2} m_t \sum_i \nu_{\mathrm{ril}} T(E_{\mathrm{il}}) \ln\left\{\frac{1+\exp\left[(E_{\mathrm{Fl}}-E_{\mathrm{il}})/k_BT\right]}{1+\exp\left[(E_{\mathrm{Fr}}-E_{\mathrm{il}})/k_BT\right]}\right\} + \frac{4qk_BT}{\pi\hbar^2}\sqrt{m_t m_l} \times \sum_i \nu_{\mathrm{rit}} T(E_{\mathrm{it}}) \ln\left\{\frac{1+\exp\left[(E_{\mathrm{Fl}}-E_{\mathrm{it}})/k_BT\right]}{1+\exp\left[(E_{\mathrm{Fr}}-E_{\mathrm{it}})/k_BT\right]}\right\} \quad (1)$$

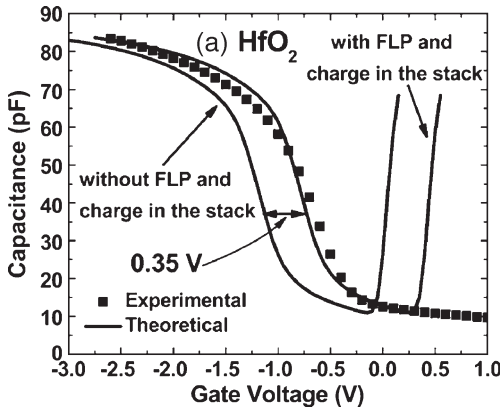


Fig. 2. Experimental and theoretical $C$–$V$ characteristics (with and without the $V_T$ shift) for structure $a$ (4 nm of $HfO_2$ and 1 nm of $SiO_2$).

where $q$ is the electron charge, $\hbar$ is the reduced Planck constant, $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, $m_t$ ($m_l$) is the transversal (longitudinal) electron effective mass, $T(E_{\mathrm{il}})[T(E_{\mathrm{it}})]$ are the transmission coefficients for the longitudinal (transversal) effective mass, $\upsilon_{\mathrm{ril}}(\upsilon_{\mathrm{rit}})$ are the attempt frequencies for the longitudinal (transversal) effective mass at the emitter computed by taking into account the time spent by the electrons in the classically forbidden regions for each eigenfunction [11], $E_{\mathrm{il}}(E_{\mathrm{it}})$ are the longitudinal (transversal) eigenvalues, and $E_{\mathrm{Fl}}(E_{\mathrm{Fr}})$ is the Fermi level of the left (right) electrode. The transmission coefficients are obtained by solving the Schrödinger equation for the barrier with open boundary conditions.

## IV. $C$–$V$ SIMULATIONS

It is a well-known fact that with respect to the ideal $SiO_2$ case, using an Hf-based gate stack, a threshold voltage shift $\Delta V_T$ is observed for both n-MOS and p-MOS transistors [6], [7], [12]. This threshold voltage shift is positive for $n^+$ poly-Si and negative for $p^+$ poly-Si gate and is caused by Fermi-level pinning (FLP) at the poly-Si/high-$k$ interface (that is likely due to defects located in the upper part of the bandgap [6]) and by fixed charge in the gate stack. $\Delta V_T$ is larger for p-MOS transistors with respect to n-MOS transistors.

In Fig. 2, we compare the experimental $C$–$V$ characteristics of structure $a$ with those obtained from quantum simulations. The FLP can be simply and effectively taken into account by assuming an effective electron affinity of the gate electrode, in general, different from that of the gate material. Interface charge and fixed charge in the high-$k$ layer contribute to the $V_T$ shift depending on the particular sample, whereas the FLP is an interfacial effect and does not depend on the thickness of the $HfO_2$ layer. For structure $a$, we have found a $\Delta V_T$ shift of 0.35 V. The FLP reported in [7] depends on the hafnium molar fraction and is between 0.2 and 0.3 V, which probably means that the FLP alone cannot be responsible for the entire $V_T$ shift. However, we cannot separate the effect of interfacial and volume charges (one possibility would be to have a sample with different dielectric thickness). Therefore, in the following simulations, we take into account all the $V_T$ shift with an effective electron affinity (extracted by shifting the theoretical

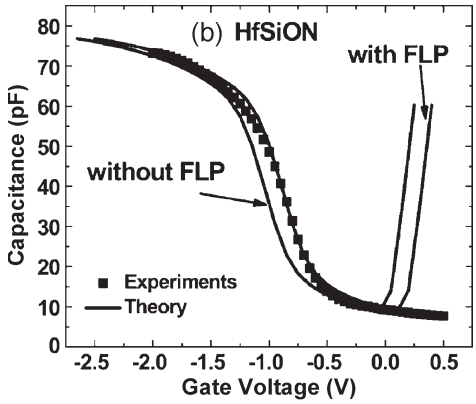


Fig. 3. Experimental and theoretical $C$–$V$ characteristics (with and without FLP) for structure $b$ (2 nm of $HfSi_XO_YN_Z$ and 1 nm of SiON).

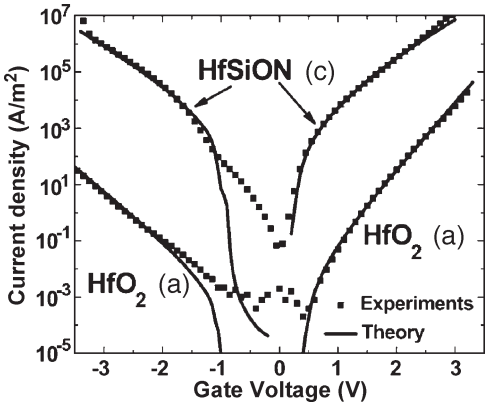


Fig. 4. Experimental and theoretical $I$–$V$ characteristics for structures $a$ (4 nm of $HfO_2$ and 1 nm of $SiO_2$) and $c$ (1 nm of $HfSi_XO_YN_Z$ and 1 nm of SiON).

$C$–$V$ curve along the voltage axis until it overlaps with the experimental one), which is strictly correct only if the shift is due to the interfacial charge. This amounts to a limited self-consistency. Indeed, the volume charge would cause not only a voltage shift but also a variation of the tunnel barrier profile, therefore modifying the shape of the $I$–$V$ characteristics. Later on, addressing TAT, we will make a similar and related approximation, neglecting the effect of the temporarily trapped electrons on the potential profile. It is important to note that in Figs. 2 and 3, we compare the experimental $C$–$V$ characteristics measured at high frequency with theoretical low-frequency $C$–$V$ characteristics: hence, the discrepancy at positive voltages. From the comparison between experimental and simulated $C$–$V$ characteristics, we can also extract the dielectric constant. We find a value of 25 for the relative dielectric constant of the hafnium oxide in good agreement with values reported in literature (for example [4]). In addition, from Fig. 2, we can observe a smoother experimental $C$–$V$ characteristic with respect to simulations, which means that the effect of interfacial traps is significant. We want to remark that we are assuming that the layer thicknesses are known with sufficient precision.

We can repeat the same procedure for the $HfSi_XO_YN_Z$ gate stack (structures $b$ and $c$) in order to extract the dielectric constant and information on the FLP and charge within the stack. In Fig. 3, we report the $C$–$V$ curves with and without the $V_T$ shift for structure $b$. The $\Delta V_T$ extracted from the comparison is of 0.13 V, and can be completely explained in terms of the FLP, since it agrees with values reported in literature [5], [6], [8]; the dielectric constant of the $HfSi_XO_YN_Z$ results to be 11 (very close to [8]). The very similar slope of the experimental and theoretical $C$–$V$ profiles in Fig. 3 also shows that $HfSi_XO_YN_Z$ has less interfacial traps.

## V. Current Density–Voltage Simulations

From the comparison between theoretical and experimental current density–voltage characteristics, we are able to extract the electronic affinity and the electron tunneling effective mass for $HfO_2$ and $HfSi_XO_YN_Z$, and to evaluate the presence of transport mechanisms additional to pure elastic tunneling. The electron affinity and the effective mass have a slightly different effect on the $J$–$V$ characteristics. Exploring the parameter space, we could only find a set of values that allows us to fit both the $J$–$V$ and the $C$–$V$ characteristics for positive and negative gate voltages. In Fig. 4, we plot the experimental and theoretical (pure tunneling) currents for $HfO_2$ and $HfSi_XO_YN_Z$ stacks, for negative and positive gate biases. The extracted electron affinity and electron effective mass, are, respectively, 1.75 eV and $0.08m_0$ for $HfO_2$, 1.97 eV and $0.24m_0$ for $HfSi_XO_YN_Z$ that have to be compared with values reported in literature [4], [5], [9], [13], [14].

TABLE II
Summary of Physical Parameters Extracted for $HfO_2$, HfSiON, and SiON

| | $HfO_2$ | HfSiON | SiON |
|---|---|---|---|
| *electron affinity* | 1.75 eV | 1.97 eV | 1.27 eV |
| *electron effective mass* | 0.08 $m_0$ | 0.24 $m_0$ | 0.45 $m_0$ |
| *relative dielectric constant* | 25 | 11 | 5 |
| *FLP* | 0.35 V | 0.13 V | - |

Hole tunneling is not significant: We have used a tunneling mass for holes of $0.5m_0$ (see for example [15]), although such value is somewhat arbitrary, since it cannot be verified in a straightforward way. For the electron tunneling effective mass in $SiO_2$, we have used $0.5m_0$. The situation is more complicated for the SiON layer for which the electron effective mass and all the other physical parameters, depend on the molar fraction of nitrogen embedded in the oxide: We have used a value of $0.45m_0$, an electron affinity of 1.27 eV, and a dielectric permittivity of 5. Such values allow us to fit the experiments, and are in good agreement with values reported in [16]. Extracted values for material parameters are summarized in Table II.

We want to stress the fact that from Fig. 4, it is clear that for the $HfSi_XO_YN_Z$ stack (structure $c$) and for the $HfO_2$ stack (structure a), the pure tunneling component is sufficient to fit the whole $J$–$V$ characteristics except for low negative gate bias between $-1$ and 0 V for structure $c$, and between $-2$ and 0 V for structure $a$. The higher measured current

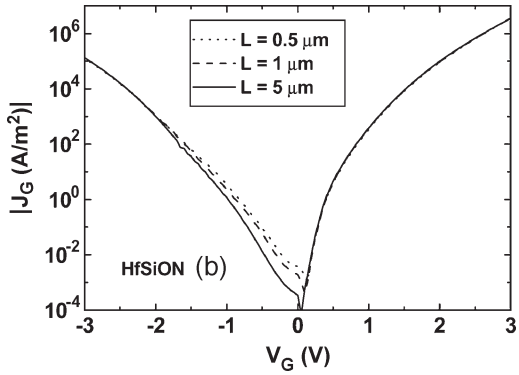


Fig. 5. $J$–$V$ comparison for different MOSFET channel lengths. At low negative voltage, the gate current density increases in shorter channel length MOSFET.

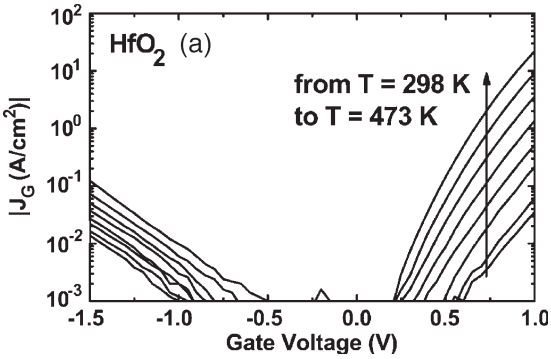


Fig. 6. Current density as a function of the gate voltage at different temperatures (from 298 to 473 K with a step of 25 K) for structure $a$ (4 nm of $HfO_2$ and 1 nm of $SiO_2$). Reproduced from Fig. 7 of [17].

density can be ascribed to two effects: an additional transport mechanism assisted by interface traps in the silicon gap [17], and a higher current density associated with the lateral source and drain $n^+$ extensions, not considered in the 1-D simulations. Consequently, a higher overall gate current density is measured in shorter channel length n-MOSFETs at low negative gate voltages, as shown in Fig. 5.

## VI. Temperature Dependence of Current–Voltage Characteristics

$HfO_2$ and $HfSi_XO_YN_Z$ show a different behavior as a function of temperature, as shown in Figs. 6 and 7, respectively. Current in $HfSi_XO_YN_Z$ stack is substantially independent of temperature, whereas in $HfO_2$, a larger temperature dependence is present for positive gate voltages, lower for negative gate voltages. We explain this behavior by introducing a temperature-dependent cross section in a microscopic model of TAT. Here, we briefly report the basic physics of the model, addressing the interested readers to the original work [19], and describe in some more detail the features that we have introduced to take into account the temperature dependence.

Let us consider the band profile sketched in Fig. 8, representing structure $a$ with a positive gate applied voltage of 0.5 V, an electron state $|\beta\rangle$ in one band of one electrode and a Khon Sham state $|\alpha\rangle$ representing a trap state in the dielectric stack. The probability per unit time that an electron tunnel from one

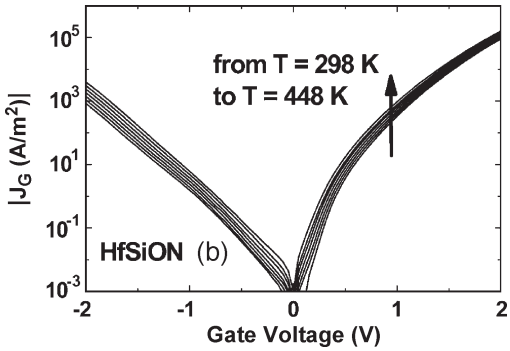


Fig. 7. Current density as a function of the gate voltage at different temperatures (from 298 to 448 K with a step of 25 K) for structure $b$ (2 nm of $HfSi_XO_YN_Z$ and 1 nm of SiON).

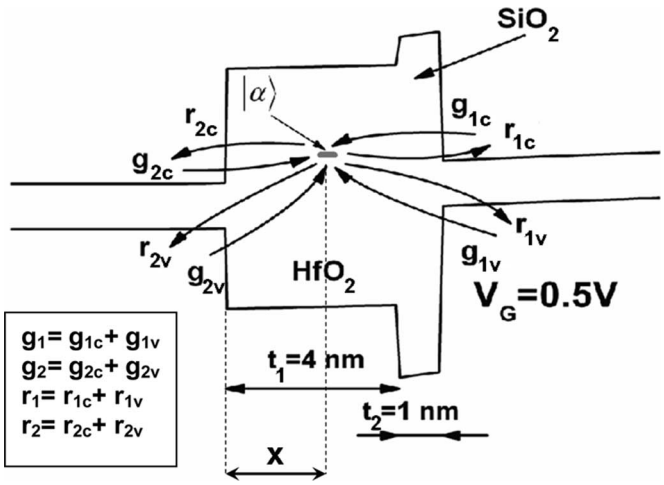


Fig. 8. Band profile of structure $a$ (4 nm of $HfO_2$ and 1 nm of $SiO_2$) with a positive gate applied voltage of 0.5 V. In the figure, it is also indicated the generation and recombination rates and a trap state $|\alpha\rangle$ in the hafnium oxide bulk.

band of one reservoir to the trap is given by the Fermi golden rule and is

$$\nu_{\beta\to\alpha} = \frac{2\pi}{\hbar}\left|M\left(\beta,\alpha\right)\right|^2 h_\Gamma\left(E_\beta - E_\alpha\right) \tag{2}$$

where

$$h_\Gamma\left(E_\beta - E_\alpha\right) = \frac{1}{\pi}\cdot\frac{\Gamma}{\left(E_\beta - E_\alpha\right)^2 + \Gamma^2} \tag{3}$$

and $E_\beta$, $E_\alpha$ are the energy of the state $|\beta\rangle$ and $|\alpha\rangle$, respectively. In (2), we take into account for inelastic transitions by using a Lorentzian function of finite half width $\Gamma$. We can rewrite (2) as

$$\nu_{\beta\to\alpha} = \sigma_{\beta,\alpha} J\left(\beta,x\right) = \sigma_{\beta,\alpha}\cdot T\left(E_l\right)\cdot f\left(E_l\right) \tag{4}$$

if we define the energy-dependent capture cross section as

$$\sigma_{\beta,\alpha} = \sigma_0\cdot h_\Gamma\left(E_\beta - E_\alpha\right). \tag{5}$$

$J(\beta,x)$ is the probability current density impinging on the plane positioned at the same depth $x$ of the trap, while $\sigma_0$, expressed as $\mathrm{m}^2\cdot\mathrm{J}$, is a compact parameter that contains all information on traps. We want to stress the fact that our definition of capture cross section is slightly different from the

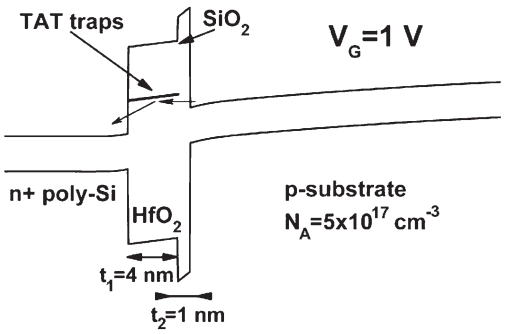


Fig. 9. Band profile of structure $a$ (4 nm of $HfO_2$ and 1 nm of $SiO_2$) with a positive gate applied voltage of 1 V as obtained by a Poisson-Schrödinger simulation. The thicker line indicates the trap level 1.6 eV below the hafnium oxide conduction band.

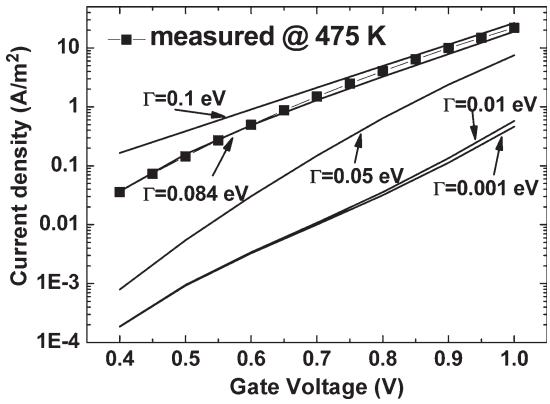


Fig. 10. Current density as a function of the gate voltage for various half width of the Lorentzian function. The best fit is reached for 0.081 eV of the half width.

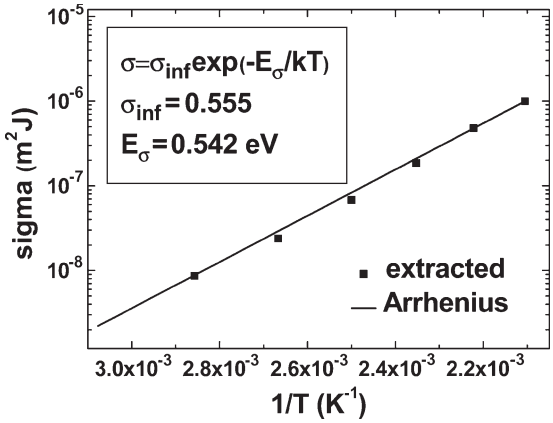


Fig. 11. Extracted capture cross section (logarithmic scale) as a function of the inverse of the temperature and Arrhenius fitting curve. In the figure are the activation energy and the capture cross section for $T \to \infty$.

conventional one, and allows us to introduce a dependence of the transition rate upon the energy difference between initial and final states.

Once we know the band profile, we can compute the capture and emission rates (which we will call in the rest of this paper generation and recombination rates, respectively), i.e., the probability per unit time that an electron tunnels from one band of one electrode to the trap and vice versa, and then the TAT current density.

$$g = 2 \int_{\beta} \nu_{\beta\to\alpha} \rho_{\beta} f_{\beta} d\beta \tag{6}$$

$$r = \int_{\beta} \nu_{\beta\to\alpha} \rho_{\beta} \left(1 - f_{\beta}\right) d\beta. \tag{7}$$

We can also write the TAT current density as [19]

$$J = q \cdot \frac{g_1 r_2 - g_2 r_1}{g_1 + g_2 + r_1 + r_2} \tag{8}$$

where the subscript 1 of the generation and recombination rates refers to states $\beta$ in the substrate and subscript 2 to states $\beta$ in the gate electrode.

The TAT current density temperature dependence can be included in an appropriate model for $\sigma_{\beta,\alpha}$ that includes its temperature dependence.

Traps in hafnium oxide have been recently investigated by Gavartin *et al.* [20] with *ab initio* calculations. From the simulations, we have observed that traps must be within the energy range 1/2 eV below the hafnium oxide conduction band in order to allow us to reproduce the shape of the $J$–$V$ characteristics at various temperatures. In [20], only one defect is in the energy range above, and it is specifically located 1.6 eV below the hafnium oxide conduction band ($O^0/O^-$ defects); hence, we assume them to be the dominant traps for the TAT current. In Fig. 9, we report the band profile for structure $a$ and the energetic position of the considered traps.

In order to simulate the TAT current, we need to know the half width of the Lorentzian function $\Gamma$ and the capture cross section. We can extract $\Gamma$ from the slope of the $J$–$V$ curve at 475 K (see Fig. 10). Indeed, we can reasonably assume, and this is confirmed by simulations, that at 475 K, the TAT current represents the entire current density because the pure tunneling current depends only slightly on the temperature.

It is important to note that $\Gamma$ strongly affects the slope of the $J$–$V$ characteristics on the semilog scale, whereas $\sigma_0$ appears as a multiplicative factor in $J$ (8) so that a variation of $\sigma_0$ only shifts vertically the $J$–$V$ characteristics on the semilog scale. On the other hand, from the experimental results shown in Fig. 6, we can see that the $J$–$V$ characteristics have a slope almost independent of temperature, and therefore, we can assume that in our case, $\Gamma$ is practically constant with temperature in the operating regimes we consider.

We now have to consider the temperature dependence of $\sigma_0$, which is typically given by an Arrhenius-like behavior [21]. We shall assume

$$\sigma_0 = \sigma_{\infty} \exp\left(-E_{\sigma}/k_B T\right) \tag{9}$$

where $\sigma_{\infty}$ is the capture cross section for $T \to \infty$, and $E_{\sigma}$ is the activation energy of the capture process.

For each temperature, we determine the value of $\sigma_0$ which provides the best fit between the theoretical and experimental $J$–$V$ characteristics. The extracted $\sigma_0$ is plotted in Fig. 11 as a function of temperature: As can be seen, it perfectly fits an Arrhenius function with an activation energy $E_{\sigma} = 0.542$ eV and $\sigma_{\infty} = 0.555$ m$^2 \cdot$ J. We should note that the activation

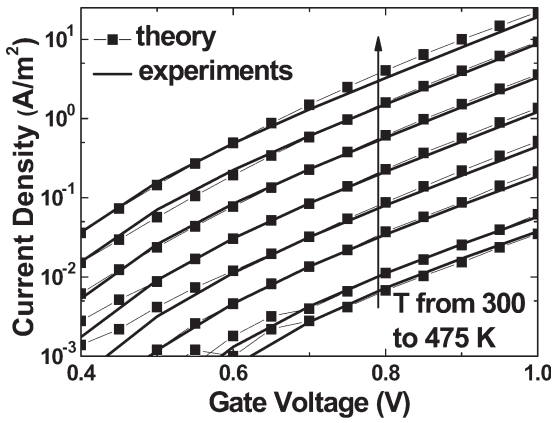


Fig. 12. Theoretical and experimental curves for positive gate applied voltage at various temperatures for structure $a$ (4 nm of $HfO_2$ and 1 nm of $SiO_2$).

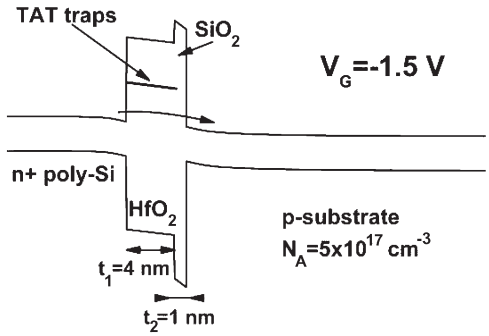


Fig. 13. Band profile of structure $a$ (4 nm of $HfO_2$ and 1 nm of $SiO_2$) with a negative gate applied voltage of $-1.5$ V. With a thicker line is represented the trap band 1.6 eV below the hafnium oxide conduction band.

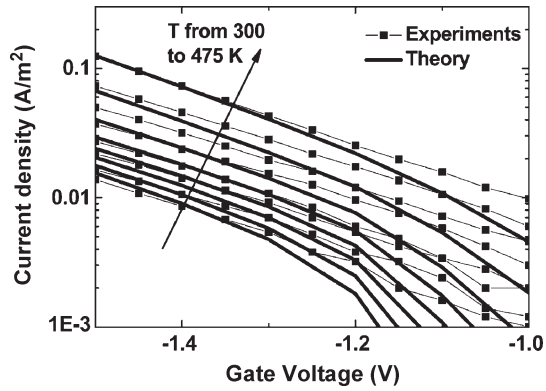


Fig. 14. Theoretical and experimental curves for negative gate applied voltage at various temperatures for structure $a$ (4 nm of $HfO_2$ and 1 nm of $SiO_2$).

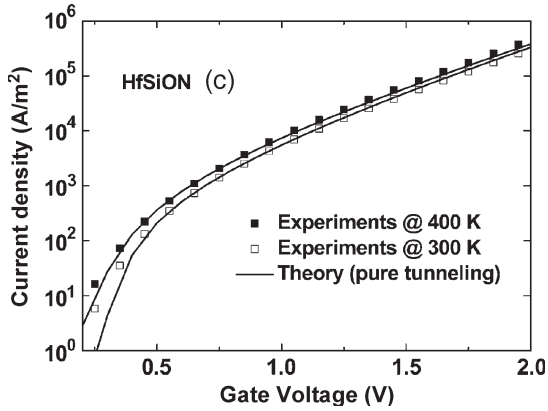


Fig. 15. Theoretical and experimental curves for positive gate applied voltage at various temperatures for structure $c$ (1 nm of $HfSi_XO_YN_Z$ and 1 nm of SiON) at 298 and 400 K.

energy of the capture cross section is rather high with respect to that typically found for $SiO_2$, which is lower than 0.3 eV [22], but to our knowledge, no other data are available for hafnium oxide, and we cannot exclude *a priori* this value. Indeed, some materials, such as $a$ Si:H, exhibit an activation energy even higher than that we have obtained (0.69 eV [23]).

With the extracted values of $\Gamma$ and $\sigma(T)$, the TAT current can be well reproduced for positive gate voltage, as sketched in Fig. 12. For negative gate applied voltage, TAT current is less relevant because the traps have a much higher energy with respect to the emitter Fermi level, as we can see in Fig. 13. In addition, we must remark that an additional transport mechanism, associated with the lateral source and drain $n^+$ extensions, is present for relatively "low" negative gate voltage $(-1 < V_G < 0)$, and this is not considered in our 1-D simulations (see Fig. 5). Then, we have to focus on higher negative gate voltages $(-1.6 < V_G < -1)$. The agreement for negative gate applied voltages between theoretical and experimental curves is reasonable, but not as good as for positive voltages mainly because the low absolute values for the current density lead to an increased relative error, as shown in Fig. 14. For the hafnium silicate nitride, experiments show a very small temperature dependence, which can be explained in terms of pure tunneling current. We cannot exclude that traps are present in the hafnium silicate nitride bulk, but we point out that they are not responsible for a significant TAT component. In Fig. 15, experiments and simulations at 298 and 400 K are reported for structure $c$: They are in good agreement without any additional fitting parameter.

The temperature-dependent TAT model allows us to reproduce experiments if we assume that traps in hafnium oxide are uniformly distributed in the layer. We have checked that if we assume that the traps are placed exclusively at one of the hafnium oxide interfaces, we are not able to obtain a good agreement with measurements. Indeed, in this latter case, the slope of the theoretical curves would depend on temperatures, while that of the experimental curves would not. Our assumption that traps are uniformly distributed in the hafnium oxide layer is also confirmed by some recent experiments [8].

## VII. Conclusion

We have shown that the temperature dependence of the leakage current in hafnium oxide can be explained in terms of a microscopic model for TAT with temperature-dependent capture cross section, where the relevant traps are uniformly distributed in the layer volume at 1.6 eV below the hafnium oxide conduction band. The cross section has an Arrhenius-like behavior with a rather high activation energy of 0.542 eV. For the samples of $HfSi_XO_YN_Z$ at hand, we observe a much smaller dependence of the leakage current on temperature, that can be simply explained by considering only the pure tunneling component.

## ACKNOWLEDGMENT

The authors would like to thank G. Groeseneken and IMEC for providing the samples used in this work.

## REFERENCES

[1] G. Groeseneken, L. Pantisano, L.-Å. Ragnarsson, R. Degraeve, M. Houssa, T. Kauerauf, P. Roussel, S. De Gendt, and M. Heyns, "Achievements and challenges for the electrical performance of MOSFET's with high-$k$ gate dielectrics," in *Proc. 11th IPFA*, Hsinchu, Taiwan, R.O.C., 2004, pp. 147–155.

[2] M. Takayanagi, T. Watanabe, R. Iijima, A. Kaneko, S. Inumiya, I. Hirano, K. Sekine, A. Nishiyama, K. Eguchi, and Y. Tsunashima, "HfSiON gate dielectrics for CMOS applications," in *Proc. IGWI*, Tokyo, Japan, 2003, pp. 128–132.

[3] M. Terai, K. Takahashi, K. Manabe, T. Hase, T. Ogura, M. Saitoh, T. Iwamoto, T. Tatsumi, and H. Watanabe, "Highly reliable HfSiON CMOSFET with phase controlled NiSi (NFET)and Ni3Si (PFET) FUSI gate electrode," in *VLSI Symp. Tech. Dig.*, 2005, pp. 68–69.

[4] J. Robertson, "Interfaces and defects of high-$k$ oxides on silicon," *Solid State Electron.*, vol. 49, no. 3, pp. 283–293, Mar. 2005.

[5] K. Torii, T. Aoyama, S. Kamiyama, Y. Tamura, S. Miyazaki, H. Kitajima, and T. Arikado, "Dielectric breakdown mechanism of HfSiON/$SiO_2$ gate dielectric," in *VLSI Symp. Tech. Dig.*, 2004, pp. 112–113.

[6] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor, J. M. Grant, L. G. Dip, D. H. Triyoso, R. I. Hedge, D. C. Gilmer, R. Garcia, D. Roan, M. L. Lovejoy, R. S. Rai, E. A. Hebert, H.-H. Tseng, S. G. H Anderson, B. E. White, and P. J. Tobin, "Fermi-level pinning at the Polysilicon/MetalOxide interface—Part I," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 971–977, Jun. 2004.

[7] ——, "Fermi-level pinning at the Polysilicon/MetalOxide interface—Part II," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 978–984, Jun. 2004.

[8] C. D. Young, G. Bersuker, G. A. Brown, C. Lim, P. Lysaght, P. Zeitzoff, R. W. Murto, and H. R. Huff, "Charge trapping in MOCVD hafnium-based field dielectric stack structures and its impact on device performance," in *Proc. IEEE Integr. Reliab. Workshop Final Report*, Oct. 2003, pp. 28–35.

[9] M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, A. Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takanayagi, and A. Nishiyama, "Effect of Nitrogen in HfSiON gate dielectric on the electrical and thermal characteristics," in *IEDM Tech. Dig.*, 2002, pp. 849–852.

[10] G. Iannaccone and S. Gennai, "Program, erase and retention times of thin-oxide Flash-EEPROMs," *VLSI DESIGN*, vol. 13, no. 1–4, pp. 431–434, 2001.

[11] G. Iannaccone and B. Pellegrini, "Compact formula for the density of states in a quantum well," *Phys. Rev. B*, vol. 53, no. 4, pp. 2020–2025, 1996.

[12] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Kohno, T. Chikyo, H. Kitajima, and T. Arikado, "Physics in Fermi Level Pinning at the Poly-Si/Hf-based High-$k$ Oxide interface," in *VLSI Symp. Tech. Dig.*, 2004, pp. 108–109.

[13] J. Zhang, E. Zhao, Q. Xiang, J. Chan, J. Jeon, J.-S. Goo, A. Marathe, B. Ogle, M.-R. Lin, and K. Taylor, "Polarity dependent reliability of advanced MOSFET using MOCVD Nitrided Hf-silicate high-$k$ gate dielectric," in *Proc. IEEE IRW Final Report*, 2002, pp. 92–95.

[14] W. J. Zhu, T.-P. Ma, T. Tamagawa, J. Kim, and Y. Di, "Current transport in metal/Hafnium Oxide/Silicon structure," *IEEE Electron Device Lett.*, vol. 23, no. 2, pp. 97–99, Feb. 2002.

[15] K.-N. Yang, H.-T. Huang, M.-C. Chang, C.-M. Chu, Y.-S. Chen, M.-J. Chen, Y.-M. Lin, M.-C. Yu, S. M. Jang, D. C. H. Yu, and M. S. Liang, "A physical model for hole direct tunneling current in p+ poly-gate pMOSFETs with ultrathin gate oxides," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2161–2166, Nov. 2000.

[16] M. Togo, K. Watanabe, T. Yamamoto, N. Ikarashi, T. Tatsumi, H. Ono, and T. Mogami, "Electrical properties of 1.5-nm SiON gate-dielectric using radical oxygen and radical nitrogen," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 1903–1909, Nov. 2002.

[17] F. Crupi, C. Ciofi, A. Germanò, G. Iannaccone, J. H. Stathis, and S. Lombardo, "On the role of interface states in low-voltage leakage currents of metal-oxide semiconductor structures," *Appl. Phys. Lett.*, vol. 80, no. 24, pp. 4597–4599, Jun. 17, 2002.

[18] F. Crupi, R. Degraeve, A. Kerber, D. H. Kwak, and G. Groeseneken, "Correlation between Stress-Induced Leakage Current (SILC) and the $HfO_2$ bulk trap density in a $SiO_2$/$HfO_2$ stack," in *Proc. IEEE Int. Reliab. Phys. Symp.*, Apr. 25–29, 2004, pp. 181–187.

[19] G. Iannaccone, F. Crupi, B. Neri, and S. Lombardo, "Theory and experiments of suppressed shot noise in stress-induced leakage currents," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1363–1369, May 2003.

[20] J. L. Gavartin, A. L. Shluger, A. S. Foster, and G. I. Bersuker, "The role of nitrogen-related defects in high-$k$ dielectric oxides: Density-functional studies," *J. Appl. Phys.*, vol. 97, no. 5, pp. 053704-1–053704-13, Mar. 2005.

[21] J.-U. Sachse, J. Weber, and H. Lemke, "Deep-level transient spectroscopy of Pd-H complexes in silicon," *Phys. Rev. B, Condens. Matter*, vol. 61, no. 3, pp. 1924–1934, Jan. 15, 2000.

[22] S. Özder, I. Atilgan, and B. Katircioğlu, "Temperature dependence of the capture cross section determined by DLTS on an MOS structure," *Semicond. Sci. Technol.*, vol. 10, no. 11, pp. 1510–1519, Nov. 1995.

[23] H. Okushi, T. Takahama, Y. Tokumaru, S. Yamasaki, H. Oheda, and K. Tanaka, "Temperature dependence of electron-capture cross section of localized states in a-Si:H," *Phys. Rev. B, Condens. Matter*, vol. 27, no. 8, pp. 5184–5187, Apr. 1983.

**Andrea Campera** was born in Livorno, Italy, in 1977. He received the "Laurea" degree (*cum laude*) in electrical engineering from Università di Pisa, Pisa, Italy, in 2004, where he is currently working toward the Ph.D. degree.

His main field of research is in the development of models and codes for the simulation of transport in semiconductor nanoscale devices.

**Giuseppe Iannaccone** (M'98) received the M.S.E.E. and Ph.D. degrees in electrical engineering from Università di Pisa, Pisa, Italy, in 1992 and 1996, respectively.

In 1996, he took a permanent position as a Researcher with the Italian National Research Council, and in the same year, he obtained a Faculty Position with the Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa, first as an Assistant Professor, then, since January 2001, as Associate Professor of electronics. His research interests include transport and noise modeling in nanoelectronic devices, development of TCAD tools, the investigation of limits to scaling down of CMOS technology, and the exploitation of nanoscale effects in alternative device structures. More recently, he is active in the design of extremely low-power systems for RFID and ambient intelligence scenarios. He has coordinated few European and national projects involving multiple partners, and has acted as the Principal Investigator in several research projects funded by public agencies at the European and national level, and by private organizations. He has authored of more than 100 papers published in journals with peer review and more than 60 papers in proceedings of international conferences.

Dr. Iannaccone is in the technical committee of few international conferences and serves as a referee for the leading journals in the fields of semiconductor physics, device electronics, and circuit design.

**Felice Crupi** received the M.Sc. degree in electronic engineering from University of Messina, Messina, Italy, in 1997 and the Ph.D. degree from University of Firenze, Firenze, Italy, in 2001.

In 2002, he joined with Università della Calabria, Arcavacata di Rende, Italy, where he is currently an Associate Professor of electronics. Since 1998, he has been a repeat Visiting Scientist with Interuniversity Micro-Electronics Center (IMEC), Leuven, Belgium. In 2000, he was a Visiting Scientist with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, and in 2006, he was a Visiting Scientist with Universitat Autonoma de Barcelona, Barcelona, Spain. His main research interests include reliability of VLSI CMOS devices, electrical characterization techniques for solid state electronic devices, and the design of ultralow noise electronic instrumentation. He has authored or coauthored of more than 70 publications in international scientific journals and in international conference proceedings.