Comparison of Modeling Approaches for the Capacitance–Voltage and Current–Voltage Characteristics of Advanced Gate Stacks

GP. Palestri
Dipartimento di Ingegneria Elettrica, Gestionale e Meccanica, Università di Udine
N. Barin
Advanced Research Center on Electronic Systems for Information and Communication Technologies, Università di Bologna
D. Brunel
Laboratoire de Physique de la Matiere, Centre National de la Recherche Scientifique Institut National des Sciences Appliquées de Lyon
C. Busseret
Laboratoire de Physique de la Matiere, Centre National de la Recherche Scientifique Institut National des Sciences Appliquées de Lyon
A. Campera
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
P. A. Childs
Emerging Device Technology Group, Department of Electronic, Electrical, and Computer Engineering, University of Birmingham
F. Driussi
Dipartimento di Ingegneria Elettrica, Gestionale e Meccanica, Università di Udine
C. Fiegna
Advanced Research Center on Electronic Systems for Information and Communication Technologies, Università di Bologna

GP. Palestri, N. Barin, D. Brunel, C. Busseret, A. Campera, P. A. Childs, F. Driussi, C. Fiegna, G. Fiori, R. Gusmeroli, G. Iannaccone, M. Karner, H. Kosina, A. Lacaita, E. Langer, B. Majkusiak, C. M. Compagnoni, A. Poncet, E. Sangiorgi, L. Selmi, A. S. Spinelli, J. Walczak, *Comparison of Modeling Approaches for the Capacitance–Voltage and Current–Voltage Characteristics of Advanced Gate Stacks*, IEEE Transactions on Electron Devices, **54**,1, pp.106-114 (2007).

Gianluca Fiori
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa

R.Gusmeroli
Dipartimento di Elettronica e Informazione, Politecnico di Milano

Giuseppe Iannaccone
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa

M. Karner
nstitute for Microelec- tronics, Technische Universität Wien

H. Kosina
nstitute for Microelec- tronics, Technische Universität Wien

A. L. Lacaita
Dipartimento di Elettronica e Informazione, Politecnico di Milano

E. Langer
nstitute for Microelec- tronics, Technische Universität Wien

B. Majkusiak
Institute of Microelectronics and Optoelectronics, Warsaw University of Technology

C. Monzio Compagnoni
Dipartimento di Elettronica e Informazione, Politecnico di Milano

A. Poncet
Laboratoire de Physique de la Matiere, Centre National de la Recherche Scientifique Institut National des Sciences Appliquées de Lyon

E. Sangiorgi
Advanced Research Center on Electronic Systems for Information and Communication Technologies, Università di Bologna

L. Selmi
Dipartimento di Ingegneria Elettrica, Gestionale e Meccanica, Università di Udine

A. S. Spinelli
Dipartimento di Elettronica e Informazione, Politecnico di Milano

J. Walczak
Institute of Microelectronics and Optoelectronics, Warsaw University of Technology

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***Abstract*—In this paper, we compare the capacitance–voltage and current–voltage characteristics of gate stacks calculated with different simulation models developed by seven different research groups, including open and closed boundaries approaches to solve the Schrödinger equation inside the stack. The comparison has been carried out on template device structures, including pure SiO_2 dielectrics and high-κ stacks, forcing the use of the same physical parameters in all models. Although the models are based on different modeling assumptions, the discrepancies among results in terms of capacitance and leakage current are small. These discrepancies have been carefully investigated by analyzing the individual modeling parameters and the internal quantities (e.g., tunneling probabilities and subband energies) contributing to current and capacitance.**

***Index Terms*—Gate leakage, gate stacks, high-κ dielectric materials, tunneling.**

I. Introduction

MOSFET scaling implies a continuous reduction of the equivalent thickness of the gate dielectric, which has nowadays reached values in the order of 1 nm [1]. At this length scale, quantum–mechanical tunneling through the gate dielectric causes a significant charge leakage from the quasi-bound states of the inversion or accumulation layer [2]. The resulting gate current raises numerous problems both at the device level and at the circuit level, namely 1) reliability of the dielectric ([3] and references therein), 2) static power dissipation [4], [5] and 3) discharging of isolated nodes in dynamic circuits [6]. Therefore, the predictive simulation and accurate modeling of the tunneling current through the gate dielectric is crucial for proper device and circuit design. As a result, gate leakage modeling has been a common research topic in past years [2], [7]–[16].

The tools for modeling gate leakage are also commonly used to extract from measurements some of the basic device parameters such as dielectric thickness, relative permittivity, and poly-Si doping by fitting the experimental capacitance–voltage (C–V) and gate current–voltage (I–V) curves [17]. In order to obtain meaningful results by this procedure, the underlying physical models and simulation tools should be properly validated. Because no standards can be defined (i.e., there is no higher level model to use as a benchmark) and the models are based on different approximations (e.g., the open and closed boundaries in the solution of the Schrödinger equation), their verification has to be implemented through mutual comparison. This is an essential prerequisite in order to make the other results achieved with these models also mutually comparable.

In this context, a comparison of the tools used to calculate the C–V curves in thin oxide devices has been presented in [18], whereas a limited comparison among different gate current models has been provided in [16] and [19].

In this paper, we report a comparison of capacitance per unit area (C) and gate current density (J_G) versus the gate voltage (V_G) characteristics of template MOS-Cap structures featuring pure SiO_2 or high-κ gate dielectrics, calculated according to the various models. A unique set of model parameters has been enforced to make the comparison more effective and efficient and to highlight the residual discrepancies due to different assumptions and model approximations. The results have been thoroughly analyzed in order to point out model similarities and limitations, and a good convergence of the results has been achieved.

This paper proceeds as follows. An overview of the simulation models employed is provided in Section II. The simulated template devices are described in Section III. Results are reported and discussed in Section IV. Conclusions are drawn

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P. Palestri, F. Driussi, and L. Selmi are with the Dipartimento di Ingegneria Elettrica, Gestionale e Meccanica (DIEGM), University of Udine, 33100 Udine, Italy.

N. Barin, C. Fiegna, and E. Sangiorgi are with the Advanced Research Center on Electronic Systems for Information and Communication Technologies (ARCES), University of Bologna, 40125 Bologna, Italy.

D. Brunel, C. Busseret, and A. Poncet are with the Laboratoire de Physique de la Matiere, Centre National de la Recherche Scientifique (UMR-CNRS 5511) Institut National des Sciences Appliquées de Lyon (INSA-Lyon), 69621 Villeurbanne, France.

A. Campera, G. Fiori, and G. Iannaccone are with the Dipartimento di Ingegneria dell'Informazione, Universitá di Pisa, 56126 Pisa, Italy.

P. A. Childs is with the Emerging Device Technology Group, Department of Electronic, Electrical, and Computer Engineering, University of Birmingham, Edgbaston, B15 2TT Birmingham, U.K.

R. Gusmeroli, A. L. Lacaita, C. Monzio Compagnoni, and A. S. Spinelli are with the Dipartimento di Elettronica e Informazione, Politecnico di Milano, 20133 Milano, Italy.

M. Karner, H. Kosina, and E. Langer are with the Institute for Microelectronics, Technische Universität Wien, 1040 Wien, Austria.

B. Majkusiak and J. Walczak are with the Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, 00-662 Warsaw, Poland.

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TABLE I
MAIN FEATURES OF THE SIMULATION MODELS USED IN THIS COMPARISON. PLEASE REFER TO THE TEXT FOR THE MEANING OF THE DIFFERENT ACRONYMS

	boundary conditions	tunnel probability	escape time	Refs
Model 1	open	n.a.	resonance peak	[28]
Model 2	periodical	TMM	n.a.	[32]
Model 3	closed	TMM	semiclassical	[33], [34] [35], [36]
Model 4	closed	WKB	n.a.	[37], [38] [31]
Model 5	open	n.a.	PML	[26], [27]
Model 6	closed	TMM	semiclassical	[19]
Model 7	closed	TMM	semiclassical	[39]

in Section V. A direct comparison with experimental data is provided in the Appendix.

II. DESCRIPTION OF THE SIMULATION APPROACHES

Seven modeling approaches have been considered in the comparison and they will be indicated as *Model 1*, . . . , *Model 7*. A detailed description of these models can be found in the references listed in Table I.

All of the models are based on the one-dimensional self-consistent solution of the Schrödinger and Poisson equations in a polysilicon/dielectric/silicon stack, where polysilicon is treated as crystalline silicon. The Schrödinger equation is solved under effective mass approximation applying closed, open, or periodic boundary conditions. All of the models assume thermal quasi-equilibrium in the semiconductor regions, i.e., the occupation of energy states in the conduction and valence bands are described by a unique Fermi level (zero split of the quasi-Fermi levels) [20].

In addition to the choice of the physical parameters, which is discussed in Section III, the calculations mainly differ in three aspects, namely 1) the boundary conditions for the solution of the Schrödinger equation, 2) the computation of the tunneling probability, and 3) the calculation of resonant tunneling from bound states [21]–[25]. The key features of the models with respect to these three aspects are summarized in Table I. Model 6 can evaluate the escape time of bound states, both with a semiclassical approach [9] and with an approach based on the half-width of the resonance peak [19]. In this comparison, only the former approach has been used. Model 7 can account for band gap-narrowing effects and incomplete ionization, but these features have been turned off in the present calculations in order to facilitate comparison with the other models.

A. Boundary Conditions

With regard to boundary conditions, in the closed boundaries case, quantum boxes are defined at the polysilicon/dielectric and dielectric/silicon interfaces, and the wave functions are assumed to vanish at both ends of the quantum boxes. Several differences exist between the models regarding the definition of the quantum boxes.

Model 3 forces the quantization of both electrons and holes in the boxes at the poly/dielectric and dielectric/silicon interfaces, so that only quantized carriers are present in the simulation domain. A fraction of the dielectric (i.e., 1 nm for $t_{OX} > 2$ nm or the whole dielectric otherwise) is included in the boxes in order to account for wave-function penetration.

Model 4 uses one box of variable width at the dielectric/silicon interface, where both electrons and holes are quantized. Here, the box was set to include 0.5 nm of oxide and 40 nm of silicon. Carriers in the poly gate are treated classically.

Model 6 uses, in inversion conditions, a quantum box at the dielectric/silicon interface for electron quantization and a quantum box at the poly/dielectric interface for holes. Electrons in the gate and holes in the substrate instead are treated classically. In accumulation, the holes in the substrate and the electrons in the poly are quantized. Carriers out of the potential wells are treated with a continuum of classical states.

Regarding Model 7, the quantum box includes the substrate and the whole dielectric. In accumulation, holes are quantized, whereas electrons are treated classically. In inversion, electrons are quantized, and holes are classical. Carriers in the poly are treated classically.

Open boundary conditions have been implemented in different ways, all of which incorporate wave-function penetration in the dielectric. Model 1 uses the transfer matrix method (TMM) to identify the subband energies as the resonant peaks of the energy dependence of the reflection coefficient as defined in [16]. Holes are treated classically. Model 5 is based on the perfectly matched layer (PML) method, which implements an absorbing boundary condition by introducing stretched coordinates [26], [27]. The holes are quantized in the bulk as well as in the poly gate.

Periodic boundary conditions are implemented in Model 2 in the following way: The quantum box includes the whole device, thus accounting for wave-function penetration in the dielectric. Both electrons and holes are quantized. The Schrödinger equation is solved two times, applying Dirichlet and then Neumann conditions on both sides. This is like simulating an infinite periodical structure, but only over one half-period. Due to these multiple boundary conditions, the continuum of states does not need to be treated in a special manner.

B. Gate Capacitance

Starting from the self-consistent solution of the Schrödinger and Poisson equations, in all model implementations, the gate capacitance is obtained by differentiating the total charge with respect to the gate voltage. The total charge is accounted for by the twofold and fourfold degenerate valleys of the silicon band structure, with unique values of the effective masses (see Table II). In some of the models (i.e., Model 6 and Model 7), the charge of a continuum of classical states is added to that of the bound states in order to account for electron states outside the potential wells.

C. Gate Current

In all the model implementations, the gate current is calculated by postprocessing the data obtained with the solution of the Schrödinger equation. The gate current density is the sum of

TABLE II
PHYSICAL PARAMETERS FOR SILICON, SILICON-DIOXIDE AND HAFNIUM-OXIDE USED IN THIS PAPER. PARAMETERS FOR HfO_2 ARE CONSISTENT WITH THOSE IN [40]

symbol	value	description
ϵ (SiO_2)	3.9	relative dielectric constant of SiO_2
m_{ox} (SiO_2, elec)	$0.5m_0$	effective mass of SiO_2
ϕ_B (SiO_2, elec)	3.1eV	conduction band offset at Si/SiO_2 interface
ϵ (HfO_2)	20	relative dielectric constant of HfO_2
m_{ox} (HfO_2, elec)	$0.2m_0$	effective mass of HfO_2
ϕ_B (HfO_2, elec)	1.55eV	conduction band offset at Si/HfO_2 interface
m_L (Si)	$0.916m_0$	longitudinal effective mass of Si
m_T (Si)	$0.19m_0$	transversal effective mass of Si
N_C (Si)	2.73×10^{19}cm^{-3}	effective DoS, conduction band
N_V (Si)	1.02×10^{19}cm^{-3}	effective DoS, valence band

the contribution from each subband (as shown in the references in Table I):

$$J_G = \frac{qK_BT_L}{\pi\hbar^2}\sum_i \frac{m_{\text{eff},i}n_i}{\tau_i}\ln\frac{1+\exp\left(\frac{E_{FL}-E_i}{K_BT_L}\right)}{1+\exp\left(\frac{E_{FR}-E_i}{K_BT_L}\right)}, \quad (1)$$

where q is the electron charge, K_B is the Boltzmann constant, T_L is the lattice's temperature, i is the subband index, E_i is the subband energy, n_i is the subband multiplicity, $m_{\text{eff},i}$ is the effective mass in the plane normal to the interface, τ_i is the escape time (life time) of the ith subband, and E_{FL} and E_{FR} are the Fermi levels at the left and right side of the simulation domain, respectively.

Disparities in the calculated current density can be traced back to the different methods used in the calculation of τ_i.

The models based on the solution of the Schrödinger equation with open boundaries provide τ_i in a natural way: in Model 1, it is given by $\tau_i = \hbar/\Delta E_i$, where ΔE_i is the half-width of the Lorentzian peak of the reflection coefficient [28], while in Model 5, the solution of the Schrödinger equation with the PML method provides complex eigenvalues, and τ_i is related to their imaginary part E_i^{im} as $\tau_i = \hbar/2E_i^{im}$.

On the other hand, the models based on the solution of the Schrödinger equation with closed boundaries (i.e., Models 3, 6, and 7) implement a definition of τ_i based on the semiclassical round-trip time [9]

$$\frac{1}{\tau_i} = \frac{T(E_i)}{\int_0^{x_i}\sqrt{2m_i/\left[E_i - E_C(x)\right]}dx} \quad (2)$$

where $T(E_i)$ is the tunnel probability corresponding to the subband energy E_i, x_i is the abscissa of the classical turning point, which is referred to the interface at $x = 0$, m_i is the effective mass in the quantization direction, and E_C is the conduction band edge. All of the groups using the semiclassical round-trip time compute the tunnel probability using the TMM [29]. In Model 3, the round trip time of each eigenfunction is computed with the full quantum approach described in [30, eq. 12], which enables one to properly include the time spent by the particle in the classically forbidden regions, which obviously is not considered in (2). The difference with respect to the semiclassical approach is quantitatively significant for ultrathin body devices and in heterostructures.

The contribution of the continuum of states to the gate current in Models 6 and 7 is given by the product of the incident flux and the corresponding tunnelling probability.

Model 4 is not based on the escape-time concept, but it calculates the incident flux by considering a free electron gas. The incident flux is then multiplied by the tunnelling probability obtained with a modified Wentzel–Kramers–Brillouin (WKB) method, where the conduction- and valence-band edges are increased by a quantity equal to the shift of the first quantized level in the inversion layer [31].

The tunnelling approach included in Model 2 calculates the gate current as [32]

$$J_G = \sum_\nu \frac{qm_\nu K_BT_L}{2\pi^2\hbar^3} \times \int_{-\infty}^{+\infty} T_\nu(E)\left(F_0(E_{FL}-E) - F_0(E_{FR}-E)\right)dE, \quad (3)$$

where F_0 is the zeroth-order Fermi function, and ν runs over six valleys, twofold and fourfold degenerated. m_ν is the effective mass in the plane normal to the interface. The tunnel probability $T_\nu(E)$ is evaluated with the TMM between the output contact and the turning point in the channel. In this way, the integral over E gives nonnegligible results only when E coincides with the subband energy.

In all of the models, image charge and momentum conservation effects have been neglected when computing the tunnel probability.

III. PARAMETERS OF THE TEMPLATE DEVICES

In order to compare the different models on the same basis, we have selected three different template devices. The first two, denoted as device A and device B, are the ones proposed in [18] and feature a pure SiO_2-gate oxide and a polysilicon gate. The oxide thickness is $t_{ox} = 1$ nm and 3 nm for devices A and B, respectively; the n-type poly doping is $N_P = 10^{20}$ cm^{-3} and $N_P = 5\times10^{19}$ cm^{-3}, respectively; the p-type substrate doping is $N_{SUB} = 10^{18}$ cm^{-3} and $N_{SUB} = 3\times10^{17}$ cm^{-3}, respectively. The third device, denoted as HK, features $N_P = 10^{20}$ cm^{-3} and $N_{SUB} = 3\times10^{17}$ cm^{-3}. The gate stack consists of a 4-nm HfO_2 layer and a 1-nm SiO_2 interfacial layer.

The physical parameters for SiO_2 and HfO_2 reported in Table II have been used in all of the models.

IV. RESULTS

In this section, we report the simulated C–V and I–V characteristics of the template devices. In order to understand

TABLE III
FLATBAND VOLTAGES OF THE SIMULATED DEVICES AS OBTAINED WITH THE DIFFERENT MODELS

	device A	device B	device HK
Model 1	-1.128	-1.070	-1.100
Model 2	-1.120	-1.060	-1.095
Model 3	-1.130	-1.065	-1.098
Model 4	-1.129	-1.064	-1.097
Model 5	-1.130	- 1.065	-1.098
Model 6	-1.131	-1.066	-1.099
Model 7	-1.130	-1.065	-1.098

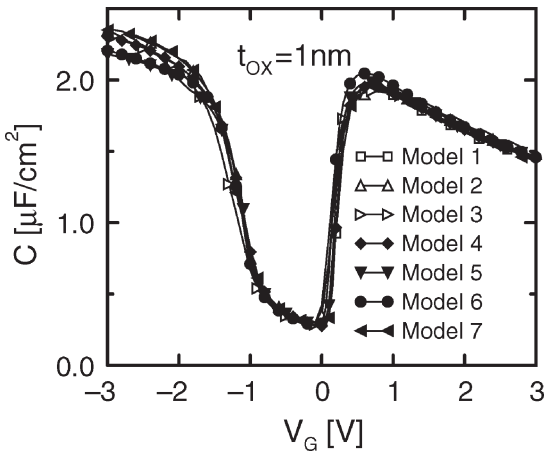

Fig. 1. Simulated C–V curves for device A.

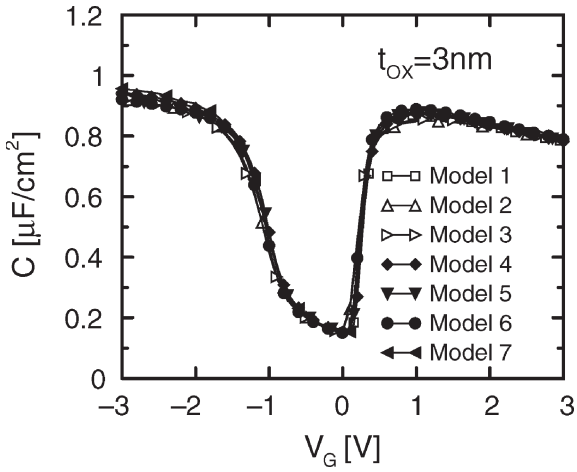

Fig. 2. Simulated C–V curves for device B.

the discrepancies between the different models, we will analyze in detail some of the "ingredients" of the capacitance and gate current calculations, such as the subband energies, the conduction band profile, the tunnel probability, and the escape time.

A uniform set of symbols has been adopted to identify the results from the different models, so that they are always shown with the same symbol: open squares: Model 1; open triangles up: Model 2; open triangles right: Model 3; filled diamonds: Model 4; filled triangle down: Model 5; filled circles: Model 6; filled triangles left: Model 7.

Table III reports the flatband voltages, calculated as the difference between the Fermi levels in the gate and in the bulk.

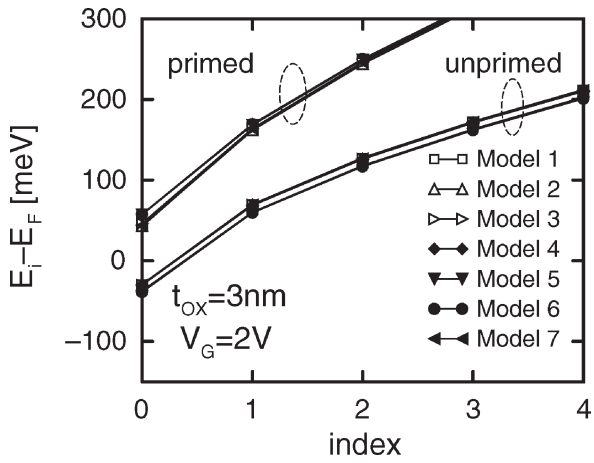

Fig. 3. Subband energies, which are referred to the Fermi level in the substrate, in the substrate of device B at $V_G = 2$ V.

A. Capacitance–Voltage Characteristics

The simulated C–V characteristic are reported in Figs. 1 and 2 for devices A and B, respectively. A detailed analysis of the results shows that small discrepancies emerge between the models for the 1-nm oxide device (i.e., device A) in the accumulation region (i.e., the data from Models 5 and 6 are slightly lower than other models' data) and at the gate voltage of the maximum inversion capacitance (i.e., $V_G \approx 0.5$ V), where a large spread appears between the limiting cases of Models 2 and 6. These differences are mainly due to the different models for quantization in polysilicon (as described in Section II, in some models carriers are treated classically in the poly). Most of these small effects are washed out further in the 3-nm oxide (i.e., device B), where a maximum discrepancy of less than 5% is registered among the model calculations. The small shift in the C–V of Model 3 with respect to the other models is due to the approach used in this model for polysilicon quantization near the flatband. When polysilicon quantization is switched off in Model 3, this shift disappears.

In order to better understand the origin of these residual differences, we have compared the conduction band profile and the eigenvalue energies predicted by the different models at two representative gate voltages, namely 1) -2 V and 2) $+2$ V.

In inversion (i.e., $V_G = 2$ V), all of the models exhibit very consistent results with very similar conduction band energy profiles, which are not shown. As a consequence, the subband energy of the first few unprimed and primed subbands, which is reported in Fig. 3, is similar for all models. In Fig. 3 and in the following, we use the standard notation to identify the subbands, that is, the term "unprimed" refers to the subbands having $m = 0.916\ m_0$ in the direction perpendicular to the Si/SiO_2 interface (i.e., two valleys), whereas the term "primed" refers to the ones having $m = 0.19\ m_0$ (i.e., four valleys).

Fig. 4 shows the conduction band profile in accumulation. The bottom of the conduction band has been forced to be the same at the far right end of the simulation domain (i.e., the quasi neutral substrate region) for all datasets in order to convert different definitions of E_C to a unique reference energy. A closer analysis of Fig. 4 shows that in accumulation, the different

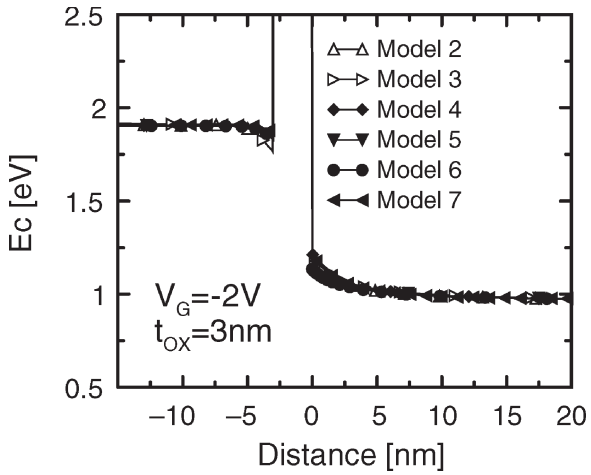

Fig. 4. Conduction band profile of device B for $V_G = -2$ V.

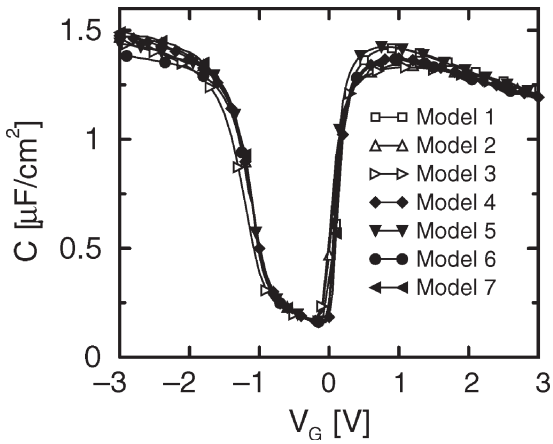

Fig. 5. Simulated C–V curves for the HK device.

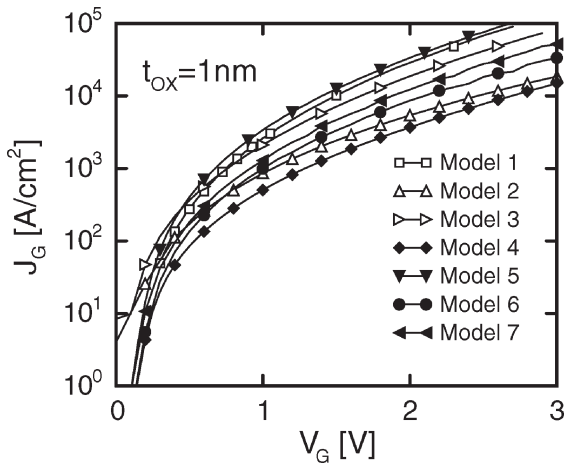

Fig. 6. Simulated I–V curves for device A.

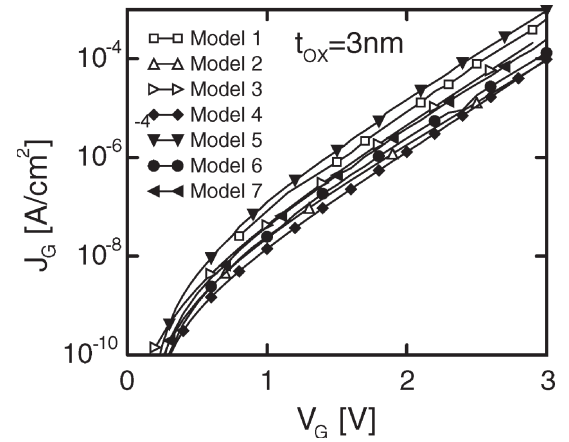

Fig. 7. Simulated I–V curves for device B. The PML method cannot work properly when the imaginary part of the eigenenergy, which is related to the life time of the bound state, is much lower than the real part. This issue is relevant in this device, especially at low V_{GS}. For this reason, the implementation of Model 5 for this device is based on the semiclassical escape time, and it is thus similar to the approach used in Models 3, 6, and 7.

treatment of the continuum of states results in a slightly larger spread than in inversion conditions.

The simulated C–V curves for the HK device are shown in Fig. 5. A good agreement between the different models is also found in this case, as with pure SiO_2 dielectrics (Figs. 1 and 2). The largest differences are in accumulation conditions and at $V_G \approx 0.5$ V (i.e., the gate voltage corresponding to maximum gate capacitance), as found in Figs. 1 and 2. A comparison of the individual ingredients leading to the result of Fig. 5 yielded essentially the same qualitative results found for the SiO_2 stacks.

B. I–V Curves

The simulated gate current in inversion conditions are reported in Figs. 6 and 7 for devices A and B, respectively. The shape of the curve is fairly similar for all models, and, also, the quantitative predictions of J_G are reasonably consistent for relatively thick oxides (i.e., within a factor of 5, as shown in Fig. 7). The spread in the current values marginally increases in thinner oxides, as shown in Fig. 6.

In the following, we analyze and compare the ingredients of the gate current computation. We have seen that, consistently with the gate current calculation in Fig. 7, all of the models provide practically the same conduction band profile for $V_G > 0$ and, in particular, the same oxide field and the same potential well in the substrate. Moreover, since the effective masses are the same, the subband energies are also practically the same (as shown in Fig. 3), at least for the models employing the same boundary conditions (i.e., open, closed, or periodical, see Table I). Therefore, the models employing semiclassical escape times based on the integration of the inverse of the classical velocity in between the classical turning points and that use the same approach to determine the transmission probabilities (e.g., TMM, as for Models 3, 6, and 7), should essentially determine the same gate current values. Discrepancies are traced back to the calculation of the tunneling probability and of the escape time. Remarkably, Model 1, employing a life-time calculation procedure based on the half-width of the Lorentzian peak of the reflection coefficient [28], features almost the same gate current (as shown in Figs. 6 and 7) as the other groups. Concerning Model 5, the PML method, as well as methods based on scanning the reflection coefficient, is more suitable for thin barriers and, therefore, some problems occur in the 3-nm device. For

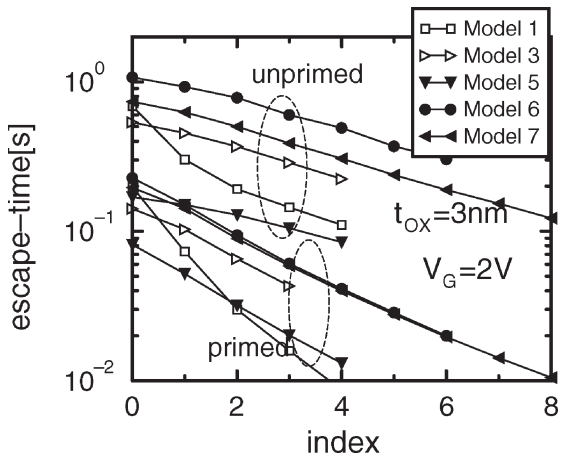

Fig. 8. Escape time as a function of the subband index for device B at $V_G = 2$ V. Consistently with Fig. 7, the data for Model 5 refers to the semiclassical escape time.

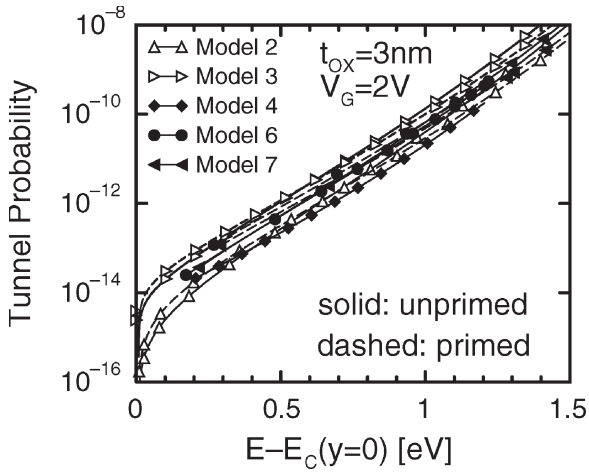

Fig. 9. Tunnel probability from substrate to gate as a function of the electron energy, which is referred to the conduction band edge at the dielectric/silicon interface, for device B at $V_G = 2$ V.

this reason, the gate current calculations for device B have been carried out using a semiclassical model for the escape time, which is similar to the approach taken in Models 3, 6, and 7. The large gate current, compared to the other models, may be due to the inconsistency between the calculation of the eigenvalues (using open boundaries) and calculation of the escape time using the semiclassical model. The slightly smaller gate current predicted by Model 4 is likely due to the single subband approximation taken when computing J_G.

In gate current calculations, an important role is played by the escape time of the bound states. Hence, we report in Fig. 8 the escape times obtained by some models for device B at $V_G = 2$ V. As for Models 3, 6, and 7, they have been calculated as the ratio of the particle round trip time along the path between the classical turning points of the eigenstate divided by the tunneling probability. Since Models 2 and 4 are not based on the escape time, contributions from these groups are not shown. The data obtained with Model 1 and based on the half-width of the Lorentzian peak [28], are slightly lower but essentially in agreement with those of Models 3, 6, and 7, based on the round trip time.

Another important ingredient for gate current calculation is the tunnel probability, which is plotted for device B in Fig. 9 for $V_G = 2$ V. The data from Models 1 and 5 are not shown, since these models do not separate the tunnel probability from the escape times, as shown in Section II. The spread in the tunnel probability is quite limited and essentially comparable with that found in the gate tunneling current. Note that the approaches based on the transfer matrix technique predict zero tunneling probability for $E - E_C = 0$, because the carrier velocity drops to zero in this limiting case. WKB-based calculations, instead, predict a non zero probability even at $E - E_C = 0$, because in this case the tunnel probability is simply given by the integral of the wave vector between the classical turning points.

Fig. 10 reports the gate current of the HK device for positive bias. A fairly good agreement is found as in the pure SiO_2 stacks (Figs. 6 and 7). Plots of the escape times and of the tunneling probabilities give results similar to the ones in Figs. 8 and 9.

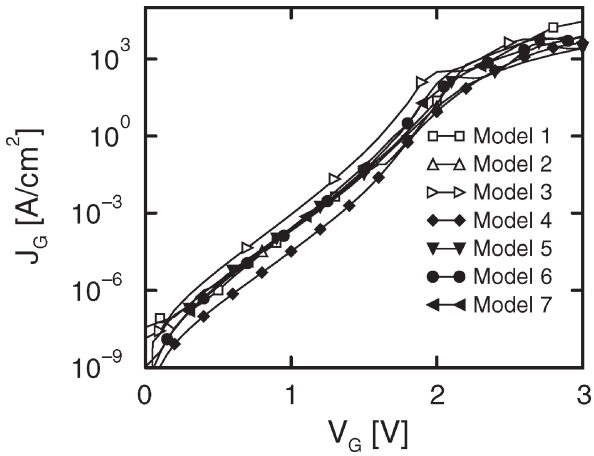

Fig. 10. Simulated I–V curves for device HK.

V. Conclusion

A detailed unprecedented comparison effort has been carried out by seven groups in order to validate available capacitance and gate current modeling approaches.

The template devices include two SiO_2 stacks, with different oxide thickness, and one high-κ stack ($HfO_2 + SiO_2$). Polysilicon gates have been assumed. All of the groups were forced to use the same model parameters, in order to make the comparison more efficient.

A good agreement between the results obtained using the different models has been found in the simulations of capacitance–voltage characteristics in SiO_2, as well as in the high-κ stacks. Regarding the gate current calculations, a satisfactory convergence of the results has been obtained in the case of positive gate voltages.

The differences in gate capacitance and gate current, which have been obtained from the models based on the solution of the Schrödinger equation with closed boundaries and the ones based on open boundaries, are small. Furthermore, the spreading between the models based on different boundary conditions is comparable with the one between the models based on the same approach. This suggests that the approach

based on closed boundaries, coupled with the evaluation of the semiclassical escape time of the bound states, provides a good trade-off between efficiency and precision, since it gives results comparable with the models based on open boundaries, but it is much faster.

The results yield an improved awareness of the individual groups, and of the modeling community as a whole, on the strengths and weaknesses of each approach. They also lead to the improved confidence of the device research community toward the capabilities of the modeling approaches for gate current calculation, since they show that different groups working in the topic of gate leakage have developed models that, even if based on different approximations, provide fairly consistent results.

APPENDIX
COMPARISON WITH EXPERIMENTAL DATA

In this section we compare the models with published experimental data on gate current.

In order to clarify the actual meaning of this comparison, it has to be noted first that it is very difficult to extract reliable data free of parasitic effects from measurements on real devices. Special care has to be taken in the design of the test structure [41] and in the characterization procedure. Moreover, the set of model parameters chosen in Table II is certainly realistic but not necessarily the most accurate possible in absolute terms. If we fix the device parameters (e.g., doping, oxide thickness, etc.) from the measurements and fit the tunneling masses and other uncertain physical model parameters, we can achieve a good fit with experiments with essentially all the models. On the other hand, if we fix the model parameters (e.g., those of Table II) and fit the experiments by playing with device parameters, we can only conclude that we do not exactly know t_{OX}, N_P and N_{SUB} of the measured samples. Such fittings have already been performed in many of the original papers describing the models considered in this comparison, and it is not worth repeating them here.

In this context, we have decided to simulate the I–V characteristics of some of the devices measured in [42] with the model parameters of Table II, and, trusting the accuracy of the device parameters given in [42], they are the following: polysilicon doping $N_P = 10^{20}$ cm^{-3}, p-type substrate doping $N_{SUB} = 5 \times 10^{17}$ cm^{-3}, pure SiO_2 dielectric with $\mathrm{t}_{OX} =$ 1.55 nm and 2 nm. Given the uncertainty on both the physical model parameters and the device parameters, it should be clear that this comparison does not imply that a given model always provides a better match to experiments or that it is more accurate than another model. It can only show if there is a systematic discrepancy or bias of all the models in one specific direction, possibly denoting the absence of one or more important physical ingredients.

Results are reported in Fig. 11 and compared with the experimental data. The agreement is acceptable, also considering that the set of model parameters might not be the most appropriate to reproduce experimental data with all the models. Given the uncertainty on the values of some physical parameters, among all, the tunneling mass, it is well possible that the error

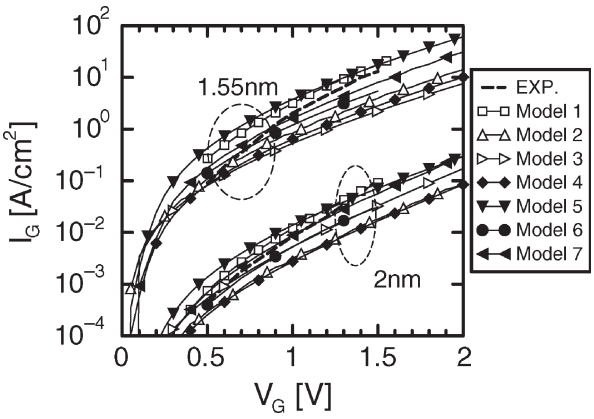

Fig. 11. I–V characteristic of pure SiO_2 gate stacks featuring $\mathrm{t}_{OX} =$ 1.55 nm and 2 nm. Comparison between the results of the different modeling approaches and the experimental data in [42] (dashed lines).

generated by one parameter is accidentally compensated by the approximations in one model and not in another one. Furthermore, in [42], the I–V and C–V characteristics, the latter used to extract t_{OX}, have been measured in different devices, so that doubts remain about the actual value of t_{OX}. Also, the disagreement between the experiments and models in terms of slope (dJ_G/dV_G) could come from doping profiles, which could be nonperfectly uniform near the Si/SiO_2 interface.

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