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F. Crupi, G. Giusi, G. Iannaccone, P. Magnone, C. Pace, E. Simoen, C. Claeys, *Analytical model for the 1/f noise in the tunneling current through metal-oxide-semiconductor structures*, Journal Applied Physics, **106**, pp.073710 (2009)

Analytical model for the 1/*f* noise in the tunneling current through metal-oxide-semiconductor structures

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(Received 10 July 2009; accepted 28 August 2009; published online 9 October 2009)

In this paper we propose an analytical model for the 1/*f* noise in the tunneling current through metal-oxide-semiconductor structures. The 1/*f* noise is ascribed to the superimposition of random telegraph signals due to elastic electron tunneling from the inversion layer to oxide traps and vice versa. The model is based on the observation that an electron trapped in the dielectric locally increases the potential barrier thus reducing the current density. The local reduction in the current density is described in terms of an effective blocking area where the current density is null when the electron is trapped. The radius of the blocking area depends smoothly on the trap spatial position and on the applied voltage, and it is roughly equal to half of the oxide thickness. Detrapping to the gate is not considered. Numerical simulations show that it is important only in a thin intermediate region inside the oxide and that the corresponding power contribution is negligible respect to that generated by traps closer to the substrate interface. The model allows us to extract an effective trap density inside the dielectric as a function of the Fermi energy from current 1/*f* noise measurements for different bias voltages. Trap densities in the order of 10^{20} cm^{-3} eV^{-1} are obtained from 1/*f* noise measurements carried on SiO_2/polysilicon gate n-metal-oxide-semiconductor-field-effect-transistors (nMOSFETs) which are in agreement with values already reported by previous works. Experiments have confirmed the area, frequency, and bias dependence of the gate current noise predicted by the proposed model. © *2009 American Institute of Physics*. [doi:10.1063/1.3236637]

I. INTRODUCTION

The study of 1/*f* noise has been widely recognized as an important source of information on defects in solid state materials and devices.[1–20] In the particular case of complementary-metal-oxide-semiconductor (CMOS) devices, a huge number of papers have been dedicated to the 1/*f* noise of the channel current.[4–13] These studies agree that such noise term is caused by the trapping/detrapping of channel charge carriers into/from oxide defects, whereas there is open debate on whether the responsible physical mechanism consists of charge number fluctuations or of mobility fluctuations. As far as noise of the gate current is concerned, research has been focused on the properties of shot noise in the presence of trap assisted tunneling[21–23] and as a source of information on the nature of traps. On the other hand, only a few works have been dedicated to the gate current 1/*f* noise.[14–20] Alers *et al.* proposed a qualitative model which ascribes the 1/*f* noise to fluctuations of a trap assisted tunneling current through the oxide that causes current noise but is not evident in the *I-V* characteristics.[14] They suggested that this type of noise may be a more sensitive probe of the degradation in thin oxides than other measurements. Lee *et al.* proposed an analytical model for the gate current excess noise based on the barrier height fluctuation and the inelastic trap assisted tunneling transport.[15] In their model the trap density is a fitting parameter which has to be numerically extracted from the gate noise data. In addition, they studied the correlation effects at low frequency between the drain noise and the gate noise.[16] Armand *et al.* proposed a numerical model for the gate current spectral density based on Green's function approach which allows us to extract the oxide trap density profile.[17] Recently we have reported that the gate current 1/*f* noise can be used as a sensitive probe for evaluating the impact of new materials on the quality of the gate stack in CMOS devices.[14–20] There are some advantages in using gate current 1/*f* noise measurements with respect to the other standard electrical techniques for dielectric quality characterization (low frequency–high frequency *C-V*, charge pumping, drain current 1/*f* noise measurements): (i) the large gate leakage of the modern CMOS devices with ultrathin gate dielectric degrades the accuracy of all the other methods, while it represents the source of information in the case of gate current 1/*f* noise; (ii) metal-oxide-semiconductor (MOS) capacitors can be used as test vehicles, whereas other methods such as the charge pumping and the one based on the drain current 1/*f* noise measurements require MOS-field-effect-transistor (MOSFET) devices; (iii) the proposed technique can be used also with very small devices with ultrathin dielectric, whereas the method based on *C-V* measurements requires large area samples or dedicated rf test structures.[24] Nevertheless, the applicability of this characterization technique is limited by the lack of simple analytical models able to relate the gate 1/*f* noise to physical quantities of the MOS structure. The development of this analytical model is the aim of the present work.

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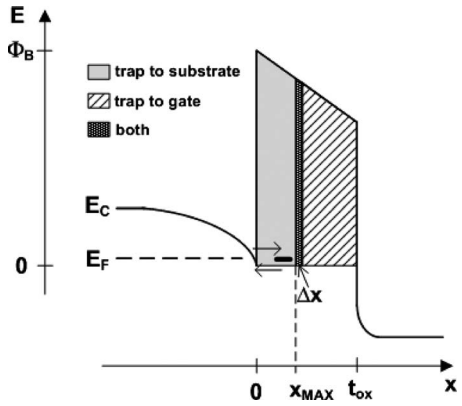

FIG. 1. Sketch of the conduction band of a MOS structure under inversion regime along with the indication of the elastic tunneling of electrons from the inversion layer conduction band to oxide traps and vice versa. In the proposed model we will consider the gate current noise originated by the traps which exchange electrons only with the substrate interface (gray region).

The remainder of this paper is organized as follows. In Sec. II we describe in detail the model for the gate current $1/f$ noise. In Sec. III we present a procedure for the estimation of the one-electron blocking area. In Sec. IV we present experiments validating the proposed model. Finally we draw our conclusion.

II. THE MODEL

In this section we derive a model for explaining the observed $1/f$ noise in the current trough a metal(gate)-insulator-semiconductor(substrate) structure biased in inversion regime, whose conduction band is sketched in Fig. 1. The model is based on the following assumptions.

(i) The physical source of the $1/f$ noise is the elastic tunneling of electrons from the substrate conduction band to oxide traps and vice versa (see Fig. 1). Thus we will consider only traps located between $0<x<x_{\max}$, where $x=0$ corresponds to the substrate interface and $x_{\max}$ is the maximum distance from the interface for which we can still discard the electron tunneling out of a trap to the gate. This assumption will be justified at the end of this section.

(ii) Each electron trapped in the oxide locally alters the oxide conduction band profile, thus causing a random telegraph signal (RTS) in the gate current. We define the one electron blocking area as $a \equiv \Delta I/J_G$, where ΔI is the gate current RTS amplitude and J_G is the gate current per unit surface when the trap is neutral. In other words, if the electron conduction through the gate oxide was completely switched off over an area a, we would observe the same RTS amplitude. Since the trapped electron does not fully block the current over an area a, but it decreases the current over a larger area, a is just an effective number. For simplicity a is assumed to be independent on trap location and gate bias. This assumption will be justified in the next section.

(iii) The gate current is due to direct tunneling of electrons, whereas we discard the trap assisted tunneling component. In other words we assume that trapping and detrapping of electrons in the oxide defects play a key role in the gate current noise while do not give a significant contribution to the overall gate current. This assumption is supported by the excellent agreement of the gate current values in ultrathin oxides obtained by measurements and by numerical simulations based only on direct tunneling.[25]

(iv) Fluctuations associated with each trap are assumed uncorrelated.

(v) The electron directly tunnels to oxide traps through a rectangular barrier of height ϕ_B.

(vi) The trap density in the dielectric per unit of volume and energy $N_T(E)$ is assumed uniform in space.

(vii) The considered frequency interval is $f_{\min} \ll f \ll f_{\max}$, where $f_{\min}$ and $f_{\max}$ correspond to oxide traps located at $x_{\max}$ and at $x=0$, respectively.

Each trap causes a RTS in the gate current with amplitude $\Delta I = aJ_G$, average time in the low state (filled trap) τ_{off} and average time in the high state (empty trap) τ_{on}. Thus the power spectral density (PSD) is given by[1]

$$S_{\text{RTS}} = \frac{4(aJ_G)^2 f_T(1-f_T)\tau_c}{1+(\omega\tau_c)^2}, \tag{1}$$

where $(\tau_c)^{-1} = (\tau_{\text{off}})^{-1} + (\tau_{\text{on}})^{-1}$ and the trap occupation probability $f_T = \tau_{\text{off}}/(\tau_{\text{on}} + \tau_{\text{off}})$. Because we do not consider the detrapping toward the gate, the balance of trapping-detrapping process imposes that the trap occupation probability coincides with the occupation probability of inversion layer charge carriers at the substrate interface, which is given by the Fermi–Dirac distribution,

$$f_T(E) = \frac{1}{1+e^{(E-E_F)/kT}}, \tag{2}$$

where E is the trap energy respect to the substrate conduction band E_C at the interface and E_F is the Fermi energy in the semiconductor. The RTS time constants are

$$\begin{cases} \dfrac{1}{\tau_{\text{on}}} = \dfrac{1}{\tau_0} T_C f_T \\ \dfrac{1}{\tau_{\text{off}}} = \dfrac{1}{\tau_0} T_C (1-f_T), \end{cases} \tag{3}$$

where τ_0 is a characteristic time constant and T_C is the transmission coefficient for electron tunneling between the silicon interface and the considered trap position at the considered trap energy. In the Wentzel–Kramers–Brillouin (WKB) approximation and by assuming a rectangular barrier of height ϕ_B, the transmission coefficient is given by[26]

$$T_C(x) = \exp(-\alpha x), \tag{4}$$

where x is the distance from the interface and

$$\alpha = \frac{4\pi}{h}\sqrt{2m^*\phi_B}, \tag{5}$$

where m^* is the tunneling effective mass of the electron in the oxide and h is Planck's constant. From Eqs. (3) and (4), it follows that

$$\tau_c = \tau_0 \exp(\alpha x). \tag{6}$$

The PSD given by all the traps, assumed uncorrelated, can be obtained by the superimposition,

$$S_{ig} = A \int_0^{x_{\max}} \int_0^{\phi_B} S_{\mathrm{RTS}}(x,E) N_T(E) dE dx, \tag{7}$$

where A is the device area and $E=0$ corresponds to the bottom of the conduction band E_C at the substrate interface. By assuming the one-electron blocking area independent of the trap position and from Eq. (2),

$$S_{ig} = \frac{4a^2 I_G^2}{A} \int_0^{x_{\max}} \int_0^{\phi_B} \frac{F_T(E)[1-f_T(E)]\tau_c(x,E)}{1+[\omega\tau_c(x,E)]^2} \times N_T(E) dE dx. \tag{8}$$

Since the function $f_T(1-f_T)$ is peaked around the Fermi level,

$$f_T(E)[1-f_T(E)] \approx kT\delta(E-E_F), \tag{9}$$

it follows that

$$S_{ig} = \frac{4a^2 I_G^2 kT N_T(E_F)}{A} \int_0^{x_{\max}} \frac{\tau_c(x,E_F)}{1+[\omega\tau_c(x,E_F)]^2} dx. \tag{10}$$

From Eq. (6) and changing variable to integrate over τ_c, we have

$$S_{ig} = \frac{4a^2 I_G^2 kT N_T(E_F)}{A\alpha} \int_{\tau_{\min}}^{\tau_{\max}} \frac{d\tau_c}{1+(\omega\tau_c)^2}, \tag{11}$$

with $\tau_{\min}=\tau_0$ and $\tau_{\max}=\tau_0 \exp(\alpha x_{\max})$. Solving the integral

$$S_{ig} = \frac{4a^2 I_G^2 kT N_T(E_F)}{A\alpha\omega} [\arctan(\omega\tau_{\max}) - \arctan(\omega\tau_{\min})] \tag{12}$$

by assuming $1/\tau_{\max} \ll \omega \ll 1/\tau_{\min}$, we have

$$S_{ig} = \frac{a^2 I_G^2 kT N_T(E_F)}{A\alpha f}. \tag{13}$$

Two important conclusions can be drawn: (i) the superimposition of the RTS noise sources due to all oxide traps originates the observed $1/f$ noise; (ii) the measurement of the $1/f$ noise for different gate voltages V_G gives us the trap density as a function of the Fermi energy,

$$N_T(E_F) = \frac{A\alpha f S_{ig}}{a^2 I_G^2 kT}. \tag{14}$$

At this point the only unknown parameter necessary to extract N_T is the one-electron blocking area. In Sec. III we will present a semianalytical model which allows to estimate this parameter.

Let us now discuss the assumption of neglecting the contribution of traps where electrons prevalently tunnel out to the gate. Each trap gives a significant contribution to the total power only at frequencies close to the corner frequency $f_c = 1/(2\pi\tau_c)$ of the associated RTS spectrum. This power contribution is proportional to the square of the RTS amplitude

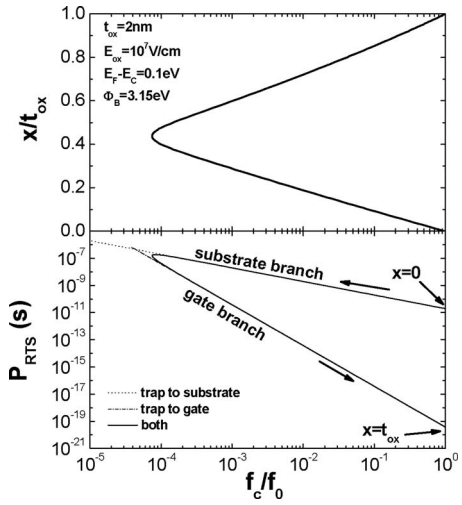

FIG. 2. The normalized trap position (a) and the Lorentzian power factor P_{RTS} (b) as a function of the RTS corner frequency normalized with respect to $f_0=1/(2\pi\tau_0)$. Two different trap positions correspond to each corner frequency, one where electrons prevalently tunnel out to the substrate (substrate branch) and the other where electrons prevalently tunnel out to the gate (gate branch). The power associated with the substrate branch is significantly higher than the one associated with the gate branch at the same corner frequency.

ΔI, which, as will be shown in Sec. III, smoothly depends on the trap spatial position, and is also proportional to the factor,

$$P_{\mathrm{RTS}} = \frac{\tau_c^2}{\tau_{\mathrm{on}} + \tau_{\mathrm{off}}} \tag{15}$$

so that we use P_{RTS} as an indicator of the power contribution of each trap to the total $1/f$ noise power. In order to investigate the dependence of f_c and P_{RTS} from the trap spatial position, we numerically evaluate τ_{on} and τ_{off} by including also the tunneling out of a trap to the gate and by using the WKB approximation for evaluating the transmission coefficient through the trapezoidal barriers. Results are reported in Fig. 2 for a MOS structure with 2 nm of SiO_2 and a p-type Si substrate. As shown in Fig. 2(a), two different trap positions correspond to each corner frequency, one where electrons prevalently tunnel out to the substrate and the other where electrons prevalently tunnel out to the gate. Figure 2(b) shows the RTS power factor P_{RTS} as a function of the corner frequency for three different cases: tunneling out only to the substrate and tunneling out only to the gate and both. Three different regions can be distinguished.

(i) $0<x<x_{\max}$, where the error in terms of RTS power due to neglecting the tunneling out to the gate is less than 10% (substrate branch).
(ii) $x_{\max}<x<x_{\max}+\Delta x$, where we have to take into account the tunneling to both interfaces.
(iii) $x_{\max}+\Delta x<x<t_{\mathrm{ox}}$, where the error in terms of RTS power due to neglecting the tunneling out to the substrate is less than 10% (gate branch).

In our example, we obtained $x_{\max}/t_{\mathrm{ox}}=0.44$ and $\Delta x=1.6$ Å. The most important message emerging from the Fig. 2(b) is that the power associated with the substrate branch is significantly higher than the one associated with the gate branch at

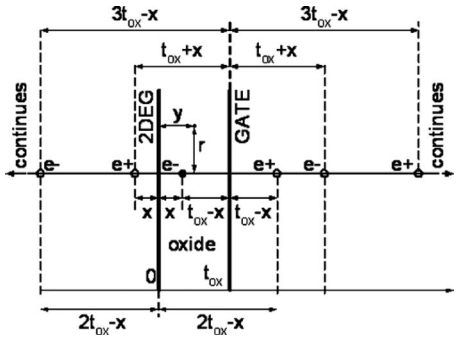

FIG. 3. Configuration of image charges that must be taken into account to write the electrostatic potential induced in the dielectric by a negatively charged trap at position x. The infinite series of image charges imposes equipotential surface on both the plane of the 2DEG and of the gate contact.

the same corner frequency. In other words, at least in the case of uniform trap density in the oxide, the contribution of traps close to the gate interface to the total power spectral density is negligible, unless in the thin intermediate region Δx where both contributions have to be considered. Note that this conclusion is not in contrast with our previous reports which show that in case of multilayer dielectric stacks and/or bad gate interface the traps close to the gate interface can strongly impact the gate current $1/f$ noise,[20] since in those cases the trap density is clearly not uniform.

III. THE ONE-ELECTRON BLOCKING AREA

The one-electron blocking area a is a crucial parameter in our model, since its estimation strongly influences the extraction of the trap density, as clear from Eq. (14). In this section we provide a semianalytical model for its evaluation. The potential in the oxide due to a single trap located in the oxide at a distance x from the inversion layer interface can be computed analytically, with the method of the image charges, assuming that we have perfect conductors at both the oxide-inversion layer and oxide-polysilicon interfaces. As is shown in Fig. 3, we have to take into account an infinite series of image charges at an ever increasing distance from the trap, in order to enforce equipotential surfaces on both the plane of the gate contact and of the two-dimensional electron gas (2DEG) inversion layer. By summing the contributions of the series of image charges, we can write the potential at depth y from the inversion layer and at a distance r from the trap axis as

$$\varphi(y,r) = \frac{q}{4\pi\varepsilon_0\varepsilon_{\mathrm{ox}}}\sum_{i=0}^{\infty} -[(y-2it_{\mathrm{ox}}-x)^2+r^2]^{-1/2} + [(y-2it_{\mathrm{ox}}-2t_{\mathrm{ox}}+x)^2+r^2]^{-1/2} + [(y+2it_{\mathrm{ox}}+x)^2 + r^2] - [(y+2it_{\mathrm{ox}}+2t_{\mathrm{ox}}-x)^2+r^2]^{-1/2}. \quad (16)$$

Once we have the potential profile along y at a distance r from the trap, we can compute the tunneling probability with the WKB approximation for an electron at the Fermi energy,[26]

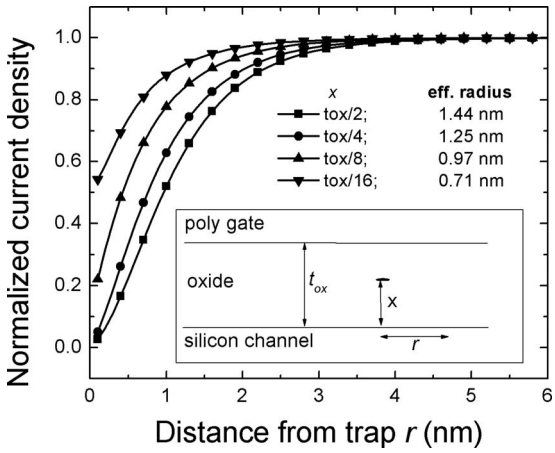

FIG. 4. Normalized current density (i.e., tunneling probability at the Fermi energy) as a function of the distance r from the trap position for different trap depths x in the oxide. The inset shows the estimated radius of the blocking area as a function of trap depth.

$$T(r) = \exp\left\{-\frac{4\pi}{h}\int_0^{t_{\mathrm{ox}}}\sqrt{2m^*[\phi_B - qE_{\mathrm{ox}}y + q\varphi(y,r)]}dy\right\}, \quad (17)$$

where E_{ox} is the electric field in the oxide and $T(r)$ is assumed to be proportional to the tunnel current density at a distance r from the trap position. If we call T_0 the tunneling probability when the trap is neutral, i.e.,

$$T_0 = \exp\left[-\frac{4\pi}{h}\int_0^{t_{\mathrm{ox}}}\sqrt{2m^*(\phi_B - qE_{\mathrm{ox}}y)}dy\right], \quad (18)$$

we can evaluate the effective area a blocked by the charged trap as

$$a = \int_0^{\infty} 2\pi r\left[1 - \frac{T(r)}{T_0}\right]dr. \quad (19)$$

In Fig. 4 we show how the normalized tunnel current density [i.e., $T(r)/T_0$] decreases as a function of the distance from the trap r for different values of the trap depth. In this calculation we have assumed an oxide thickness of 2 nm, and we have additionally assumed that the conducting planes are at an additional distance of 0.4 nm from the actual oxide interface due to polydepletion and the separation of the 2DEG from the substrate interface due to quantum confinement. Figure 5 shows the computed radius of the blocking area as a function of the trap relative position inside the dielectrics (0 corresponds to substrate interface and 1 to gate interface) for different values of the dielectric constant, oxide thickness, and gate bias. Note that in all different conditions the blocking radius value can be roughly approximated to 1 nm, which corresponds to half of the oxide thickness. As expected the radius decreases with the dielectric constant [see Fig. 5(a)], since the Coulomb potential $\varphi(y,r)$ is inversely proportional to the dielectric constant. Note that all the curves show a bell shape with a maximum in the middle of the oxide layer and the radius increases with the oxide thickness [see Fig. 5(b)]. These two observations can be easily explained since the radius increases if the metallic

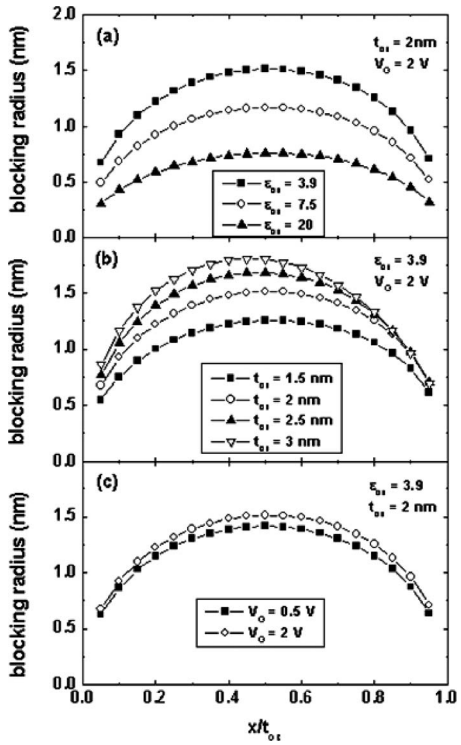

FIG. 5. The radius of the one-electron blocking area decreases with the dielectric constant (a), increases with the oxide thickness (b), and is almost independent on the gate voltage (c). In all cases the radius shows its maximum in the middle of the oxide layer.

planes—that screen the electrostatic potential—are located at a higher distance from the trap. As shown in Fig. 5(c), the blocking radius is almost independent of the applied gate voltage. These results indicate that the model assumption of the blocking area independence on trap position and gate bias is quite reasonable.

IV. EXPERIMENTS

In order to validate the proposed model, we measured the gate current noise in MOSFET devices by using a purposely designed measurement setup.[18] The low-frequency part of the measured gate current noise spectrum presents a flicker component or $1/f^{\gamma}$ component, with γ typically close to one. Figure 6 illustrates the cumulative distribution function of γ for two different sample areas, 10^{-6} and 2.8×10^{-8} cm^2. The higher dispersion of the γ value observed in smaller area devices is a consequence of the lower number of active traps. Figure 7 shows the average value of the normalized gate current noise spectra AS_{ig}/I_G^2 for the two areas. In both cases a value of γ very close to 1 is obtained, thus supporting the idea that the $1/f$ noise originates from the superposition of RTS noise sources. In addition, the two normalized spectra coincide as expected according to our model. An important implication is that the gate current $1/f$ noise can be evaluated also in small area samples but the results have to be averaged over a larger sample population.

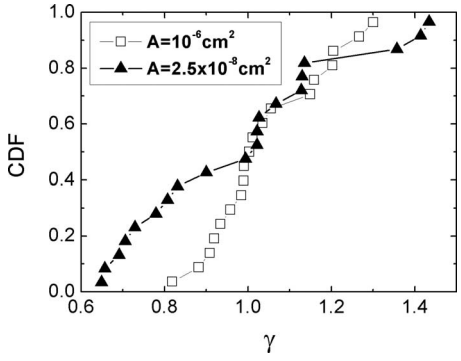

FIG. 6. Cumulative distribution function of the γ value of the gate current noise spectra measured in nMOSFETs with two different sample areas biased with V_G=1.5 V. The devices have a gate stack composed by 1 nm of SiON as interface layer, 2 nm of HfSiON and a polysilicon gate. A higher dispersion is observed for smaller area devices.

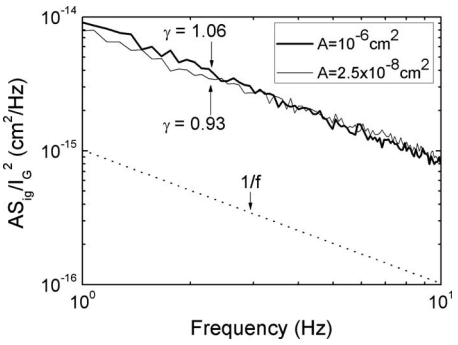

FIG. 7. Normalized gate current noise spectra averaged over about 20 samples for the same samples of Fig. 6. The two spectra are almost coincident with γ very close to 1.

In order to obtain an experimental estimation of the one-electron blocking area $a=\Delta I/J_G$, we measured the RTS amplitude ΔI and the average gate current density J_G. Although this approach seems very simple and straightforward, it presents some drawbacks. The reason is that in our model we have assumed uniform gate current density and identical blocking area for each defect. As a consequence, for a fixed bias point each trap should cause a RTS with the same amplitude $\Delta I=aJ_G$. In practice, the blocking area is only slightly dependent on trap position, but the current density is highly nonuniform for the following reasons: (i) oxide thickness nonuniformity, which is particularly important in the modern devices with oxide thickness of a few nanometers, (ii) high conductance paths, due to stress-induced leakage current or breakdown spots, (iii) in the case of metal gates and high-k cap layers, nonuniformities in the work function. If the trap stays in a region with a current density J_D higher than the average current density J_G, by evaluating the blocking area as $a=\Delta I/J_G$ instead of $a=\Delta I/J_D$, we obtain an overestimation of the a value. In general, we are able to detect only some dominant RTS traces with a higher amplitude, since the others with lower amplitude are hidden in the background $1/f$ noise. By taking into consideration only the dominant RTS traces, we should then largely overestimate the blocking area. The minimum RTS amplitude which can be detected depends on the device area, since in smaller area samples we have a lower number of active traps which gives a lower background $1/f$ noise. Thus in order to reduce the overestimation of the blocking area we evaluated the RTS amplitude in devices with an area of only 1.25×10^{-9} cm^2. Figure 8 shows the extracted radius of the blocking area. The measured values are between 8.8 and 37.8 nm (this high

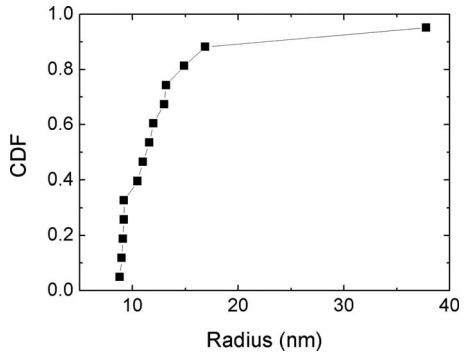

FIG. 8. Cumulative distribution function of the radius of the blocking area estimated by evaluating the amplitude of RTS in the gate current in nMOSFETs with SiON (equivalent oxide thickness of 1.6 nm) and polysilicon gate. Device area is 0.125 μm^2 ($W \times L = 0.25 \times 0.5$ μm^2).

value is due to an active trap placed close to a breakdown spot) with a median value of 11.3 nm, which, as expected, is much larger than the theoretical value.

Figure 9 reports the trap density in a Si/SiO_2(2 nm)/polysilicon structure extracted by applying the proposed model. According to the simulation results reported in Sec. III, we used a radius of the one-electron blocking area equal to 1 nm. A mean value of about 3×10^{20} cm^{-3} eV^{-1} has been obtained. Lower values in the order of 10^{18} cm^{-3} eV^{-1} are typically extracted from drain current $1/f$ noise measurements by applying the number fluctuations model,[20] while similar values have been obtained by Armand *et al.* by applying their numerical model of gate current noise.[17] Although the gate current $1/f$ noise and the drain current $1/f$ noise are two different effects of the same cause, which consists of electron trapping and detrapping in the dielectric defects, each analytical model for both types of noise is based on a different set of simplifying assumptions. As a consequence the extracted trap densities represent only effective numbers and they can be significantly different.

V. CONCLUSIONS

We have proposed an analytical model for the gate current $1/f$ noise in MOS devices which allows us to extract an effective trap density inside the dielectric as a function of the Fermi energy from gate current noise measurements as a function of the applied bias. The noise source consists of the elastic electron tunneling from the semiconductor inversion layer to oxide traps and vice versa. The model is based on the observation that an electron trapped in the dielectric locally increases the potential barrier, thus reducing the current density over an effective blocking area. The radius of the one-electron blocking area depends smoothly on the trap spatial position and on the applied voltage and is roughly equal to half of the oxide thickness. Numerical simulation proved that at least in the case of uniform trap density in the oxide, the contribution of traps close to the gate interface to the total power spectral density is negligible. Trap densities in the order of 10^{20} cm^{-3} eV^{-1} are obtained from $1/f$ noise measurements carried on SiO_2/polysilicon gate nMOSFETs which is in agreement with values already reported by previous works. Experiments have confirmed the area, frequency, and bias dependence of the gate current noise predicted by the proposed model.

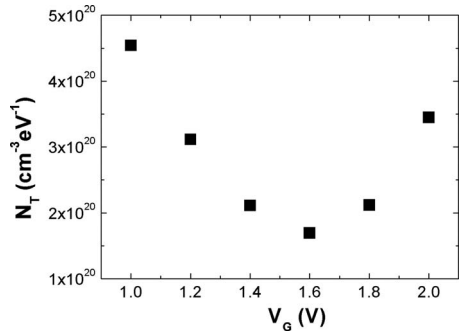

FIG. 9. Effective trap density extracted with the proposed method as a function of the applied bias in a nMOSFET with 2 nm of SiO_2 and polysilicon gate.

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