Università di Pisa

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Paolo Michetti
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
Martina Cheli
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
Giuseppe Iannaccone
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa

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Model of tunneling transistors based on graphene on SiC

Paolo Michetti,[a] Martina Cheli,[a] and Giuseppe Iannaccone[a]
Dipartimento di Ingegneria dell'Informazione Elettronica, Informatica, Telecomunicazioni, Università di Pisa, Via Caruso 16, 56122 Pisa, Italy

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Recent experiments shown that graphene epitaxially grown on Silicon carbide (SiC) can exhibit a energy gap of 0.26 eV, making it a promising material for electronics. With an accurate model, we explore the design parameter space for a fully ballistic graphene-on-SiC tunnel field-effect transistors, and assess the dc and high frequency figures of merit. The steep subthreshold behavior can enable I_{ON}/I_{OFF} ratios exceeding 10^4 even with a low supply voltage of 0.15 V, for devices with gatelength down to 30 nm. Intrinsic transistor delays smaller than 1 ps are obtained. These factors make the device an interesting candidate for low-power nanoelectronics beyond CMOS. © *2010 American Institute of Physics*. [doi:10.1063/1.3361657]

Carbon-based nanoelectronics is characterized by relatively small bandgaps and effective masses, with symmetric dispersion relations for electron and holes. This is the ideal situation for tunnel field-effect transistors (TFETs), whose carbon implementation therefore represents an extremely interesting option.[1]

Indeed, a TFET is a gated $p-i-n$ diode where the gate voltage modulates the position of energy bands in the intrinsic channel in order to control interband tunneling between the p-doped source and the n-doped drain. When the device is ON, current is dominated by interband tunneling, which instead is inhibited when the device is OFF. Small energy gaps and small effective masses can allow to achieve large ON current, comparable to that of mundane semiconductor field-effect transistors.

An impressive advantage of TFETs is the steep dependence of the current on the gate voltage, which can yield a Subthreshold Swing (SS) much smaller than 60 mV/decade, the minimum value achievable at room temperature with FETs. The very small SS also allows to implement adequate switches with very small supply voltages, and therefore to operate at extremely low power.

Finally, carbon channels very often have the same dispersion relations and mobility characteristics for electrons and holes, which is desirable for the optimization of complementary logic gates in terms of switching speed and power consumption.[2]

TFETs based on carbon nanotubes,[1] graphene nanoribbons,[3,4] and bilayer graphene[5,6] have been addressed theoretically, with simulations and analytical models. Carbon nanotubes and graphene nanoribbons are interesting in terms of the achievable performance, but device operation is extremely sensitive to the bandgap, which in turn strongly depends on the exact number of carbon atoms per ring or along the ribbon width, that is hardly controllable. Bilayer graphene is a two-dimensional (2D) channel which does not require very advanced lithography and provides a gap tunable with the vertical electric field, up to 0.15–0.2 eV. Satisfactory device operation is achieved with a supply voltage V_{DD} as small as 0.1 V.[5]

Very interestingly, epitaxial graphene grown on the Si-terminated face of a SiC substrate is a 2D material exhibiting a bandgap of 0.26 eV[7–9] and promising mobility.[10] Such semiconducting gap can be adequate to TFETs suitable for large-scale integrated circuits but is not sufficient for FETs.[11]

Here we consider the TFET illustrated in Fig. 1(a), in which the channel consists of a single graphene layer grown on a SiC substrate of overall thickness $t_{Sub}=100$ nm. The top gate is separated by a silicon oxide layer t_{ox} of 1 nm and is at voltage V_G. Following the evanescent mode approach,[12] we can estimate the natural variation length λ of the electrostatic potential in the channel as $\lambda=2/\pi(t_{ox}+t_{ch})$, where $t_{ch}=1.1$ nm is the effective distance between the graphene layer and the ideal interface of the top dielectric layer.[13] Here, we have assumed the evanescent part of the potential to be dominated by the vicinity of the top gate, neglecting the backgate, and, second, we have assumed the same effective dielectric constant for both oxide and graphene regions. Because the gate length $L_c<\lambda$, a long-channel behavior is expected. Therefore the electrostatic potential $\phi(x)$on the graphene channel is

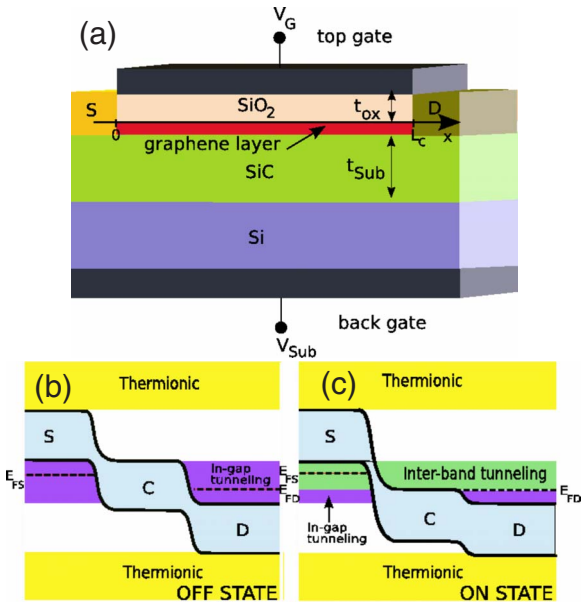

FIG. 1. (Color online) (a) Sketch of a TFET device based on graphene on SiC. (b) Band profile along the transport direction in the OFF state for a n-channel TFET, and (c) ON state of the TFET.

[a]Electronic addresses: pl.michetti@gmail.com, martina.cheli@iet.unipi.itmartina.cheli, and g.iannaccone@iet.unipi.it.

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$$q\phi(x) = qA_S e^{-x/\lambda} + qA_D e^{(x-L_c)/\lambda} + \phi_c, \quad (1)$$

where ϕ_c is the potential away from the contacts, q the absolute electron charge, $A_S \equiv E_c(0) - E_c(L_c/2)$ and $A_D \equiv E_c(L_c) - E_c(L_c/2)$, respectively, where $E_c(x)$ represents the conduction band edge in the longitudinal direction x.

For graphene on SiC we adopt the tight-binding Hamiltonian proposed in Ref. 7, which accounts for the energy dispersion curves

$$E^{(x)}_{\vec{k},\pm} = \pm\sqrt{m^2 + t^2|f(\vec{k})|^2} - q\phi(x) \quad (2)$$

of conduction (+) and valence (−) bands, whose edges, respectively, give $E_c(x)$ and $E_v(x)$, where $m=0.13$ eV is an effective parameter providing an energy gap of $2m$, $t=2.7$ eV is the nearest-neighbor hopping energy for graphene, and $f(\vec{k})$ is the well known off-diagonal element of the 2×2 graphene p_z-Hamiltonian. We assume the potential to be sufficiently smooth to rigidly shift graphene band edges. The band edge profiles for the device under investigation in the OFF state and in the ON state are shown in Figs. 1(b) and 1(c).

The device current I is the sum of three major contributions: thermionic, interband tunneling, and gap tunneling (due to tunneling through the channel in the gap spectral region). Thermionic and gap tunneling currents degrade transistor performance, dominating the current when the device is in the OFF state, and therefore must be minimized. The channel current per unit width is

$$I = \frac{q}{4\pi^2}\sum_{\pm}\int_{BZ} d\vec{k} T v_x [f(E^{(x_c)}_{\vec{k},\pm} - \mu_S) - f(E^{(x_c)}_{\vec{k},\pm} - \mu_D)], \quad (3)$$

where the integration runs over the Brillouin zone for conduction and valence bands $E^{(x_c)}_{\vec{k},\pm}$, calculated at the center of the channel (at $x=x_c=L_c/2$). f is the Fermi-Dirac distribution function and v_x is the component of the group velocity along the channel. The tunneling coefficient T is calculated via Wentzel–Kramers–Brillouin approximation in the tunneling regions at drain, at source or in the gap, as shown in Fig. 1(b). In tunneling regions, for a fixed energy E of the incoming particle, we solve the dispersion curve (2) for the complex wavevector describing the evanescent mode. The integration of the evanescent mode path through the barrier gives T, as described in more detail in Ref. 11.

In order to compute the channel potential we need to self-consistently solve the vertical electrostatics:

$$Q = -C_G(V_G - \Delta_G - \phi_c) - C_{\mathrm{Sub}}(V_{\mathrm{Sub}} - \Delta_{\mathrm{Sub}} - \phi_c),$$

$$Q = Q_h + Q_e, \quad (4)$$

where $C_G = \varepsilon_{ox}/t_{ox}$ and $C_{\mathrm{Sub}} = \varepsilon_{\mathrm{SiC}}/t_{\mathrm{Sub}}$ are the top gate and the backgate capacitance per unit area, respectively, whereas Δ_G and Δ_{Sub} are the flat band voltages of the top and backgates (set here to 0 V). The charge per unit area in the channel, due to holes and electrons (Q_h and Q_e), can be also obtained by summing over their steady-state distribution in conduction band

$$Q_e = -\frac{q}{4\pi^2}\int_{BZ} d\vec{k}[(2-T)f(E^{(x_c)}_{\vec{k},+} - \mu_S) + Tf(E^{(x_c)}_{\vec{k},+} - \mu_D)], \quad (5)$$

and valence band

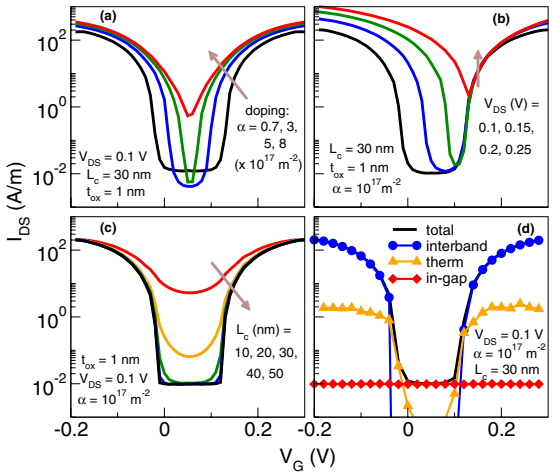

FIG. 2. (Color online) Transfer characteristics of a graphene-on-SiC TFET calculated for different parameters of the model. We analyzed the effects of a variation of doping concentration α in (a), of the supply voltage V_{DS} in (b), of the channel length L_c in (c). In (d) we show an example as the TFET total current is due to the summing up of interband tunneling, in-gap tunneling, and thermionic current contributions.

$$Q_h = \frac{q}{4\pi^2}\int_{BZ} d\vec{k}[Tf(\mu_S - E^{(x_c)}_{\vec{k},-}) + (2-T)f(\mu_D - E^{(x_c)}_{\vec{k},-})], \quad (6)$$

where we included the possible tunneling barrier at source or drain.

Let us assume the same doping density for source and drain. We can therefore define the energy difference between conduction(valence) edge and source(drain) Fermi energy at source(drain) $\delta = E_c(0) - \mu_S = -\mu_D - E_v(L_c)$. It is clear from Figs. 1(b) and 1(c) that it is possible to shut off the device only if the drain-to-source voltage satisfies $|V_{\mathrm{DS}}| < (E_{\mathrm{gap}} - 2\delta)/q$, which in the limit of weak doping becomes $|V_{\mathrm{DS}}| < 0.26$ V. Ideally, when the previous condition is satisfied, minimum device current is obtained when the channel is intrinsic at $L_c/2$. Accordingly the channel mid gap is $-q\phi_c = (\mu_S + \mu_D)/2$ and from Eq. (4) we find the OFF-state gate voltage $V_{\mathrm{OFF}} = V_{\mathrm{DS}}/2$. The OFF current I_{OFF} is defined as the current obtained with $V_{\mathrm{GS}} = V_{\mathrm{OFF}}$ and $V_{\mathrm{DS}} = V_{\mathrm{DD}}$. The ON current I_{ON} is the current obtained with $V_{\mathrm{GS}} = V_{\mathrm{OFF}} + V_{\mathrm{DD}}$ and $V_{\mathrm{DS}} = V_{\mathrm{DD}}$.

In Fig. 2, we show the TFET transfer characteristics calculated for different values of the main parameters of the model: the doping fraction α (which is a monotonous function of δ), V_{DS}, the channel length L_c. In Fig. 2(a), we show the effect of doping concentration $\alpha = 0.7$, 3, 5, and $8 \times 10^{17} \sim m^{-2}$, corresponding, respectively, to $\delta \approx 5$, 40, 65, 90 meV. As expected, the increase of δ leads to a thinning of the range of the OFF-state plateau, in which current is essentially reduced to the thermionic contribution. An initial increase of δ pushes down the source conduction band edge with respect to μ_S, and up the drain valence band with respect to μ_D, reducing the thermionic hole and electron currents, respectively. For larger α (and δ), one cannot fully shut the channel off because $|V_{\mathrm{DS}}| + 2\delta/q$ becomes larger than E_{gap}.

In Fig. 2(b), we analyze the operation of the TFET for different values of the source-drain voltage V_{DS}. The OFF-state plateau is reduced with increasing V_{DS}, I_{OFF} is constant because limited to the thermionic contribution, whereas

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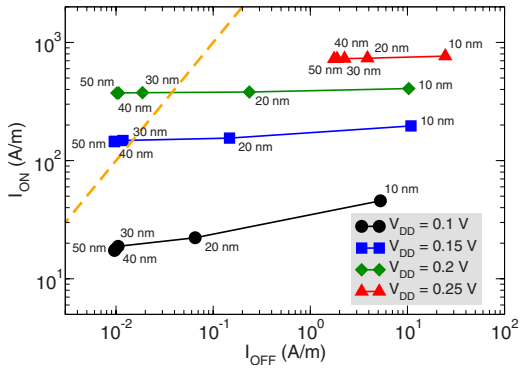

FIG. 3. (Color online) I_{ON} and I_{OFF} table for TFET devices with $V_{DD}=0.1,\ 0.15,\ 0.2,\ 0.25$ V, and L_c between 10 and 50 nm. We consider here $t_{ox}=1$ nm and $\alpha=3\times10^{16}$ m^{-2}. A dashed line marks the field where $I_{ON}/I_{OFF}\geq10^4$.

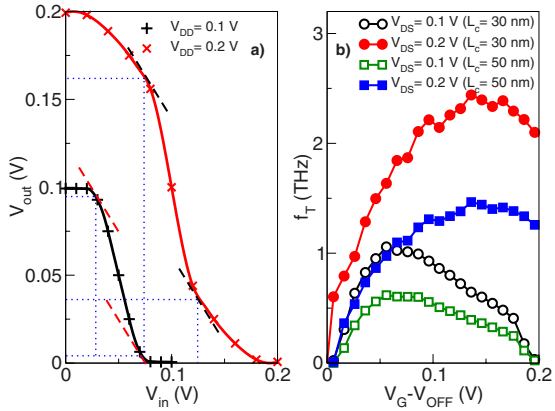

FIG. 4. (Color online) (a) Voltage transfer curve for a CMOS inverter based on the present device and operating at $V_{DS}=0.1$ and 0.2 V. Dashed lines highlight the points of the curve in which the slope is equal to unity. (b) Cutoff frequency calculated for TFETs with $V_{DS}=0.1$ and 0.2 V, for $L_c=30$ and 50 nm.

larger I_{ON} is obtained. For $V_{DS}\approx0.25$ V and above it is not possible to shut the TFET off anymore.

In view of transistor scaling we analyze the effect of a variation of the channel length L_c [Fig. 2(c)]. We show that for $L_c\geq30$ nm the OFF current does not depend on L_c and is determined by the thermionic current. However, a further reduction of L_c leads to an increase I_{OFF}, due to an increased transparency of the in-gap tunneling barrier. The oxide thickness affects tunneling through the contacts ($\lambda\propto t_{ox}$), with the main effect of exponentially reducing the tunneling log $T\propto -t_{ox}$. In Fig. 2(d), we show an example of the three current contributions occurring in the device. In ON state the tunneling current dominates the device, while it is suddenly suppressed going toward the OFF state, where thermionic current contributes to the subthreshold swing and eventually in-gap tunneling determines the OFF-state current plateau.

An important performance measure of a transistor is the obtainable I_{ON}/I_{OFF} ratio, therefore in Fig. 3 we plot I_{ON} against I_{OFF}. As noted also before, to shut the device off and have a sufficient I_{OFF} dynamics it is required $V_{DS}\leq0.2$ V, together with sufficiently long channel ($L_c\geq30$ nm) in order to limit in-gap tunneling. On the other hand the I_{ON} increases with V_{DD}. Therefore the best performance is obtained for $V_{DS}=V_{DD}=0.2$ V. Indeed we note that an I_{ON}/I_{OFF} ratio exceeding 10^4, considered adequate for low power operation,[14] can be obtained with a supply voltage of 0.15 and 0.2 V, and with a channel length L_c not smaller than 30 nm.

Now we analyze the performance of our device for digital applications. In Fig. 4(a), we plot the transfer characteristics of a CMOS inverter with identical n and p-type TFETs, with the channel of graphene on SiC with $L_c=30$ nm and $t_{ox}=1$ nm, for a supply voltage of 0.1 and 0.2 V. We extract the noise margins (NMs) for the CMOS inverter, which are a measure of logic gate robustness to disturbs and noise, as NM=22 mV and 37 mV, respectively, for $V_{DD}=0.1$ and 0.2 V. NMs are not extremely good but in line with what one could expect, given the low supply voltage.

We also performed an analysis of transistor intrinsic delay and transition frequency f_T of the considered TFET. We consider operating voltages of 0.1 and 0.2 V and a channel length of 30 and 50 nm. In particular in Fig. 4(b) we show the cutoff frequency as a function of the overdrive, calculated in the quasistatic approximation[15] $f_T=g_m/(2\pi C_G L_c)$, where $g_m\equiv\partial I_{DS}/\partial V_{GS}$ is the transconductance, and $C_G\equiv\partial Q/\partial V_{GS}$ evaluated for $V_{GS}=V_{DD}+V_{OFF}$, is the capacitance seen by the gate contact. The intrinsic delay time, which represents a figure of merit for digital application, is $\tau\equiv V_{DD}C_G/I_{ON}$. For a supply voltage of 0.1 V, we obtain $\tau=0.33$ ps and 0.54 ps, respectively, for a channel of length 30 and 50 nm. With a supply voltage of 0.2 V, $\tau=0.12$ ps for $L_c=30$ nm and $\tau=0.22$ ps for $L_c=50$ nm.

In conclusion, we examined the maximum achievable performance of a TFET based on epitaxial graphene on SiC substrates, analyzing the role of doping level, supply voltage, channel length, and oxide thickness. An I_{ON}/I_{OFF} exceeding 10^4 can be easily achieved by choosing adequate geometry and bias, with a channel length not smaller than 30 nm, for a supply voltage as small as 0.15 V. NMs of a minimum size inverter are reasonable but not impressive. Intrinsic delay times and transition frequency are very promising, and make the proposed TFET a strong candidate for extreme low-power carbon nanoelectronics.

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