Model and Performance Evaluation of Field-Effect Transistors Based on Epitaxial Graphene on SiC

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Model and Performance Evaluation of Field-Effect Transistors Based on Epitaxial Graphene on SiC

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***Abstract*—In view of the appreciable semiconducting gap of 0.26 eV observed in recent experiments, epitaxial graphene on a SiC substrate seems a promising channel material for FETs. Indeed, it is 2-D—and therefore does not require prohibitive lithography—and exhibits a wider gap than other alternative options, such as bilayer graphene. Here, we propose a model and assess the achievable performance of a nanoscale FET based on epitaxial graphene on SiC, conducting an exploration of the design parameter space. We show that the current can be modulated by four orders of magnitude; for digital applications, an $I_{\rm on}/I_{\rm off}$ ratio of 50 and a subthreshold slope of 145 mV/dec can be obtained with a supply voltage of 0.25 V. This represents a significant progress toward solid-state integration of graphene electronics, but not yet sufficient for digital applications.**

***Index Terms*—Compact models, epitaxial graphene, graphene transistors.**

I. Introduction

FROM the beginning [1], [2], graphene has attracted the attention of the scientific community due to its exceptional physical properties, such as an electron mobility exceeding more than ten times that of silicon wafers [3], and in view of its possible applications in transistors [4] and in sensors [5]. To induce a gap in graphene structures, several methods have been used: 1) lateral confinement in graphene ribbons [4], [6]; 2) carbon nanotubes [7]; 3) impurity doping [8]; or 4) a combination of single and bilayer graphene regions [9]–[11]. Unfortunately, they all face different problems.

Carbon nanotubes exhibit large intrinsic contact resistance and are difficult to pattern in a reproducible way; the inability to control tube chirality, and thus whether they are metallic or semiconducting, make solid-state integration still prohibitive. Graphene nanoribbons [4], [6] allow to obtain a very interesting device behavior [12], but require extremely narrow ribbons with single-atom precision, since a difference of only one dimer line in the width may yield a quasi-zero gap nanoribbon. Bilayer graphene exhibits a gap in the presence of a perpendicular electric field, but the range of the applicable bias can only induce a gap of 100–150 meV, not sufficient to obtain a satisfactory behavior in terms of $I_{\rm on}/I_{\rm off}$ ratio [10].

Graphene on SiC is a 2-D material, thus does not require extremely sophisticated lithography, and provides a higher energy gap; for the sake of comparison, a 0.26 eV energy gap would require an armchair nanoribbon of width smaller than 3 nm, or nanotubes with diameter smaller than 2 nm.

Epitaxially grown graphene on SiC provides potential for the large-scale integration of graphene electronics. The first challenge to the use of graphene as a channel material for FETs is to induce a reasonable gap for room-temperature operation. Recently, Zhou *et al.* [13] have experimentally demonstrated that a graphene layer, epitaxially grown on a SiC substrate, can exhibit a gap of about 0.26 eV, measured by angle-resolved photoemission spectroscopy. The gap is probably due to the symmetry breaking between the two sublattices forming the graphene crystalline structure, as also confirmed by the recent density functional calculations [14], [15]. According to Zhou *et al.* [13], this method of inducing a gap is very easy and reproducible; in addition, the thickness of graphite grown on SiC can be precisely controlled to be either single- or multiple-layered depending on the growth parameters [16]. From a manufacturability point of view, it is also extremely promising, since it would be highly convenient to prepare an entire substrate of graphene on an insulator and then obtain single device and integrated circuit through patterning [17].

In this paper, we present a semianalytical model of an FET with a channel of epitaxial graphene grown on a SiC substrate, where the band structure, the electrostatics, thermionic, and band-to-band tunneling currents are carefully accounted for. On the basis of our model, we assess the achievable device performance through an exploration of the device parameter space, and gain understanding of the main aspects affecting the device operation.

II. Model

We adopt the Tight Binding (TB) Hamiltonian for single-layer graphene on SiC that was proposed by Zhou *et al.* [13]. The empirical TB valence $(-)$ and conduction $(+)$ bands of a single epitaxial layer of graphene on SiC, read

$$E_{\pm}(k_x, k_y) = \pm\sqrt{m^2 + t^2\left|f(\mathbf{k})\right|^2} \tag{1}$$

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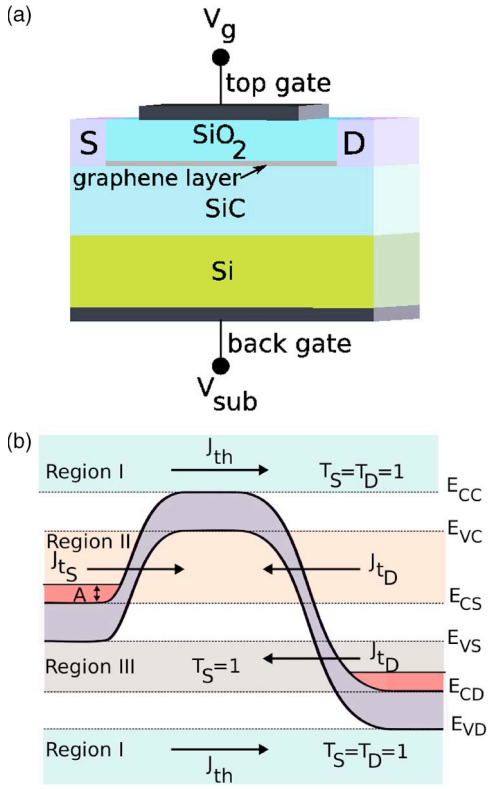

Fig. 1. (a) Schematic picture of a graphene on SiC transistor. The grey line between SiO_2 and SiC oxide represents the graphene plane acting as device channel. Source (S) and drain (D) contacts are also in graphene. (b) Profile band structure along the transport direction. The dashed lines mark the energy region in which it is possible to have thermionic current $(J_{\rm th})$, tunneling current from source to channel $(J_{\rm tD})$, and tunneling current from drain to channel $(J_{\rm tS})$.

where t is the in-plane hopping term (2.7 eV), $m = 0.13$ eV is an empirical potential energy shift between the two non equivalent graphene sublattices due to the interaction with the SiC substrate, and $f(\mathbf{k})$ is the off-diagonal element of the considered Hamiltonian [13]. In the six Dirac points of the graphene Brillouin zone, where $f(\mathbf{k})$ is zero, there is a finite energy gap $E_g = 2m$ corresponding to the channel conduction minimum $E_{\rm CC} = m - q\phi_{\rm ch}$ and the channel valence maximum $E_{\rm VC} = -m - q\phi_{\rm ch}$, where q is the electron charge and $\phi_{\rm ch}$ the self-consistent potential in the central region of the channel.

The device under consideration, depicted in Fig. 1(a), is a transistor with a channel of epitaxial graphene on a SiC substrate of thickness $t_{\rm sub} = 100$ nm, with a top gate separated by a SiO_2 layer of thickness $t_{\rm ox}$. In Fig. 1(b), we have sketched the band edge profiles along the transport direction $\hat{x}$, where $E_{\rm Ci}$ and $E_{\rm Vi}$, respectively, represent the conduction and valence band edges in the three different regions denoted by $i = S, D, C$ (Source, Drain, Channel). Source and drain contacts are n^+-doped, with molar fraction α_D, which translates into an energy difference A between the electrochemical potential μ_S (μ_D) and the conduction band edge $E_{\rm CS}$ $(E_{\rm CD})$ at the source (drain) contact. The analytical relation between α_D and A is given by: $\alpha_D = 1/D \int_{\rm BZ} f(E_{\rm CS} - A)\partial k_x \partial k_y$ where $D = 2/(\sqrt{3}a^2/2)$ is the atomic density per unit area, a is the graphene lattice constant and f is the Fermi–Dirac distribution function. The potential is set to zero at the source and to $V_{\rm ds}$ at the drain contact. In the center of the channel, $\phi_{\rm ch}$ is imposed by vertical electrostatics. We assume, as usual, complete phase randomization along the channel, which is particularly important because it allows us to neglect the effect of resonances in the presence of tunneling barriers.

Exploiting the Gauss theorem, we can write the surface charge density in the central part of the channel as

$$Q = -C_g(V_g - V_{\rm FBt} - \phi_{\rm ch}) - C_{\rm sub}(V_{\rm sub} - V_{\rm FBb} - \phi_{\rm ch}) \tag{2}$$

where $C_g = \epsilon_{\rm SiO_2}/t_{\rm ox}$ $(C_{\rm sub} = \epsilon_{\rm SiC}/t_{\rm sub})$ is the capacitance per unit area between the channel and the top gate (back gate), V_g $(V_{\rm sub})$ is the top gate (back gate) voltage, and $V_{\rm FBt}$ $(V_{\rm FBb})$ is the flatband voltage of the top gate (back gate), which we set to -0.4 eV.

The transit time of the device in the channel has been estimated as $\tau_t = Q_{\rm th}L_C/J_{\rm th} \approx 10^{-16}$ s where $Q_{\rm th}$ and $J_{\rm th}$ are the thermionic charge and current, respectively, $L_C = 20$ nm is the channel length.

In certain spectral regions, for example, in the valence band when the device is in the 'off' state, carriers are quasi-confined by tunneling barriers, and can dwell in the channel for a much longer time and be subject to some degrees of relaxation, even if transport in the conduction band is practically ballistic. It is indeed possible to include the treatment of energy relaxation in semianalytical models, through the virtual probe approach, as shown in [18] and [19]. And this approach has also been extended to consider carbon-related materials, where the interplay of energy relaxation and tunneling barriers has have been analyzed [20]. Here, we are not interested in developing a complete treatment of this problem, instead we employ a minimal model, in which a process, accounting for carrier thermalization with the contacts, has been included. Our only aim is to provide a slight correction to a canonical ballistic transport model. By increasing the effectiveness of this relaxation process with contacts, we can estimate the limit to the electrostatics imposed by a model with strict ballistic transport in all spectral regions.

In steady-state conditions, considering an infinitesimal element of area $dk_x dk_y$ in the wave-vectors space, charge distribution in the channel is obtained as a balance between two types of charge exchange processes with the contacts: one elastic, and one of thermalization.

We can write the electron charge in the channel as the sum of two contributions: N_+^e and N_-^e. $N_+^e = f_+^e L_C n_{\rm 2\text{-}D}$ $(N_-^e = f_-^e L_C n_{\rm 2\text{-}D})$ represents the density of forward (backward) going electrons, $f_\pm^e(k_x, k_y)$ denotes the occupation factors of forward $(+)$ and backward $(-)$ states in the channel, and $n_{\rm 2\text{-}D}(k_x, k_y)$ is the 2-D density of states in the k-space. For each contribution, we can write a rate equation in steady-state conditions

$$\begin{aligned}\frac{dN_+^e}{dt} &= J_S^+ - J_D^+ + (1 - T_S)f_-^e v_x \\ &\quad - (1 - T_D)f_+^e v_x + \frac{f_S^e - f_+^e}{\tau_S} L_C n_{\rm 2\text{-}D} = 0 \end{aligned} \tag{3}$$

$$\begin{aligned}\frac{dN_-^e}{dt} &= -J_S^- + J_D^- - (1 - T_S)f_-^e v_x \\ &\quad + (1 - T_D)f_+^e v_x + \frac{f_D^e - f_-^e}{\tau_D} L_C n_{\rm 2\text{-}D} = 0 \end{aligned} \tag{4}$$

where $f^e_{D,S} = \mathfrak{F}(E_+ - q\phi_{\rm ch} - \mu_{D,S})$ is the occupation factor at the drain (D) and source (S) contacts, and $\mathfrak{F}$ is the Fermi–Dirac distribution function.

Let us focus on (3) [similar considerations can be made for (4)]: $J^+_S = T_S f^e_S v_x$ is the tunneling current component injected from source, $J^+_D = T_D f^e_+ v_x$ is instead the drain tunneling current component ejected to the drain, $T_{S,D}$ are the transmission probabilities from source/drain contacts to channel, and v_x is the group velocity. $(1-T_S)f^e_- v_x$ and $(1-T_D)f^e_+ v_x$ are the reflected current components from source and drain barriers, respectively. Thermalization is introduced in the last terms of (3) and (4): the term in (3) [Eq. (4)] brings forward (backward) electrons in equilibrium with the source (drain) reservoirs, with characteristic time τ_S (τ_D). The steady-state f^e_+ and f^e_- can be obtained by solving (3) and (4)

$$f^e_+ = \frac{\left(T_D + \frac{1}{\tau_D \nu}\right)(1-T_S) f^e_D + \left(\frac{1}{\tau_D \nu} + 1\right)\left(T_S + \frac{1}{\tau_S \nu}\right) f^e_S}{\left(\frac{1}{\tau_S \nu} + 1\right)\left(\frac{1}{\tau_D \nu} + 1\right) - (1-T_S)(1-T_D)} \tag{5}$$

$$f^e_- = \frac{\left(T_S + \frac{1}{\tau_S \nu}\right)(1-T_D) f^e_S + \left(\frac{1}{\tau_S \nu} + 1\right)\left(T_D + \frac{1}{\tau_D \nu}\right) f^e_D}{\left(\frac{1}{\tau_S \nu} + 1\right)\left(\frac{1}{\tau_D \nu} + 1\right) - (1-T_S)(1-T_D)} \tag{6}$$

where $\nu = 2\pi^2 v_x / L_C$ is the inverse of the crossing time τ_t. For the sake of simplicity, in the following, we consider $\tau_S = \tau_D = \tau$.

The same reasoning can be applied to derive the hole occupation factors in the channel $f^h_\pm$.

The charge, to be self-consistently solved with (2) in order to obtain the channel potential $\phi_{\rm ch}$, is computed through the integration on the BZ

$$Q = -\frac{q}{4\pi^2} \iint_{\rm BZ} \left(f^e_+ + f^e_-\right) dk_x\, dk_y + \frac{q}{4\pi^2} \iint_{\rm BZ} \left(f^h_+ + f^h_-\right) dk_x\, dk_y \tag{7}$$

where the total current density is expressed as [21]

$$J_{\rm tot} = \frac{q}{4\pi^2} \left\{ \iint_{\rm BZ} v_x \left(f^e_+ - f^e_-\right) dk_x\, dk_y + \iint_{\rm BZ} v_x \left(f^h_+ - f^h_-\right) dk_x\, dk_y \right\}. \tag{8}$$

The transmission probability T_S (T_D) of the interband barrier at source (drain) is zero in the source (drain) band gap and one when there is no barrier between source (drain) and channel. When a barrier is present, T_S is computed analytically with the WKB approximation, assuming k_y conservation due to translational invariance along the y-direction

$$T_S(E, k_y) = \exp\left\{ -2 \int_{x_1}^{x_2} \left| {\rm Im}\left(k_x^{E,k_y}(x)\right) \right| dx \right\} \tag{9}$$

where x_1 and x_2 are the classical turning points, and E is the particle kinetic energy. The same approach is repeated for T_D.

The potential profile of the barrier connecting each contact and the central region of the channel is described by an exponential, with characteristic variation length λ, obtained from evanescent mode analysis [22] and assuming that in the barrier region mobile, charge has a negligible effect on the potential. Assuming $t_{\rm sub} \gg t_{\rm ox} > t_{\rm ch}$, we obtain

$$\lambda \approx \left(t_{\rm ox} + \frac{t_{\rm ch}}{2}\right) \frac{2}{\pi} \tag{10}$$

where $t_{\rm ch}$ is the effective separation between the interfaces of the SiO_2 and SiC layers, for which we assume $t_{\rm ch} = 1$ nm [4]. As long as $L_C \gg \lambda$, the effect of the source and drain contacts on the potential is vanishing in the middle of the channel, which is therefore dominated by the vertical electrostatics.

III. Electrostatics

From the analysis of the electrostatics, we can gain a better insight of the device performance limitations. In fact, gate voltage control upon the channel potential (of which the subthreshold slope S is a measure) is strictly limited by the quantum capacitance C_q of the channel. Device electrostatics can be schematized as in Fig. 2(a). The differential capacitance seen by the gate is

$$C_{\rm tg} = C_g \left(1 - \frac{\partial \phi_{\rm ch}}{\partial V_g}\right) \tag{11}$$

but, from Fig. 2(a), $C_{\rm tg}$ can also be expressed in terms of capacitances C_g, $C_{\rm sub}$, and C_q

$$C_{\rm tg} = \frac{C_g (C_{\rm sub} + C_q)}{C_g + C_{\rm sub} + C_q}. \tag{12}$$

From (11) and (12), we get the derivative of the channel potential with respect to the gate potential

$$\frac{\partial \phi_{\rm ch}}{\partial V_g} = \frac{C_g}{C_g + C_{\rm sub} + C_q}. \tag{13}$$

The expression of the subthreshold slope S then turns out to be

$$S = \left(1 + \frac{C_{\rm sub} + C_q}{C_g}\right) \frac{kT}{q} \ln(10) \tag{14}$$

from which it is clear that S is an increasing function of C_q, and therefore, a large quantum capacitance severely limits device performance.

Fig. 2(b) shows the capacitance–gate voltage characteristics for $V_{\rm ds} = 0, 0.1,$ and 0.25 V obtained by solving the

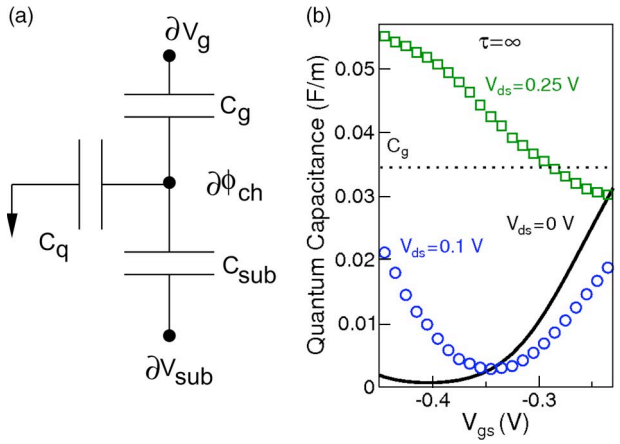

Fig. 2. (a) Equivalent circuit of device electrostatics. (b) Quantum capacitance–voltage characteristics for $V_{\rm ds} = 0, 0.1,\ 0.25$ V, $t_{\rm ox} = 1$ nm, $t_{\rm sub} = 100$ nm, and $\alpha_D = 2.4 \times 10^{-2}$ in case of fully ballistic transport.

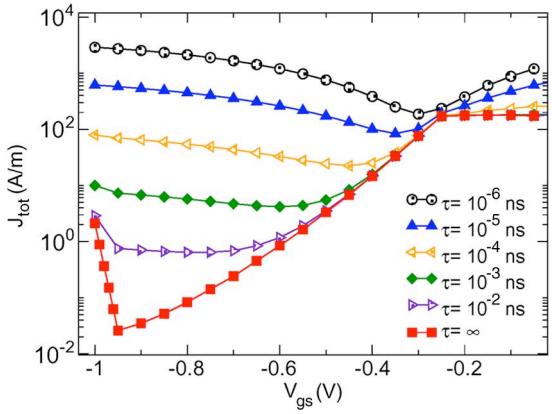

Fig. 3. Transfer characteristics for $\tau = 10^{-2}, 10^{-3}, 10^{-4}, 10^{-5}, 10^{-6}$ ns, for $V_{\rm ds} = 0.25$ V, $\alpha_D = 2.5 \times 10^{-3}$, and $t_{\rm ox} = 1$ nm.

Schrödinger equation self-consistently with Poisson equation. In the fully ballistic case, the quantum capacitance is low for small $V_{\rm ds}$, indicating a good control of the channel by the gate voltage, but, as soon as $V_{\rm ds}$ increases, hole accumulation in the channel occurs and C_q increases, rapidly degrading S [Fig. 2(b)]. When we include the thermalization process, hole accumulation is slightly suppressed by thermalization with the source contact. However, the overall effect on the quantum capacitance is practically negligible. We have observed that for τ larger than 10^{-4} ns, the quantum capacitance basically does not change with respect to Fig. 2(b); on the other hand, for $\tau < 10^{-4}$ ns C_q decreases with respect to the fully ballistic case, but the energy relaxation process becomes dominant, approaching a limit where (14) loses validity.

IV. Perspectives for Device Operation

In order to evaluate the possible performance of the SiC graphene FET, we have computed the transfer characteristics by varying three device parameters: 1) drain–source voltage $V_{\rm ds} = (\mu_S - \mu_D)/q$; 2) oxide thickness $t_{\rm ox}$, and 3) the donor molar fraction at the contacts α_D. We also account for the different possible values of energy relaxation time τ. First, in Fig. 3, we analyze the trend of the transfer characteristics

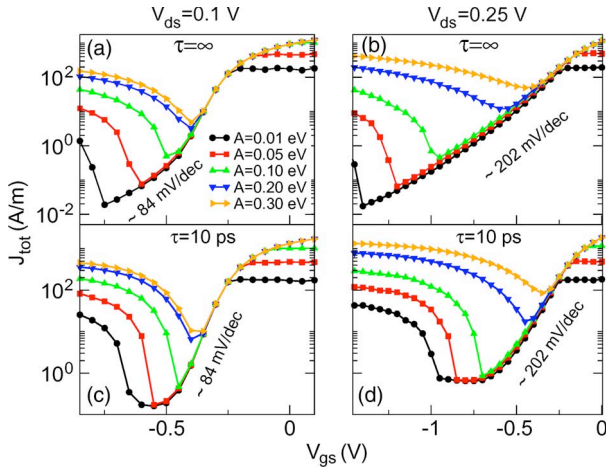

Fig. 4. Transfer characteristics for varying doping parameter $A = 0.01, 0.05, 0.1, 0.2, 0.3$ eV corresponding respectively to α_D of 2.5×10^{-3}, 9.8×10^{-3}, 2.4×10^{-2}, 6.8×10^{-2}, 1.3×10^{-1}, $t_{\rm ox} = 2$ nm with: (a) $V_{\rm ds} = 0.1$ V, $\tau = \infty$; (b) $V_{\rm ds} = 0.25$ V, $\tau = \infty$; (c) $V_{\rm ds} = 0.1$ V, $\tau = 10$ ps; and (d) $V_{\rm ds} = 0.25$ V, $\tau = 10$ ps.

for different τ for $V_{\rm ds} = 0.25$ V, $t_{\rm ox} = 1$ nm, and $\alpha_D = 2.5 \times 10^{-3}$ (corresponding to $A = 0.01$ eV). We observe that for $\tau \geq 1$ ns, the transfer characteristics are unaffected and identical to the ballistic case ($\tau \to \infty$). Reducing the relaxation time under 1 ns, the minimum current increases and the subthreshold slope remains almost constant since the quantum capacitance of the channel does not change. The introduction of the thermalization process with contacts has mainly two effects in the transfer characteristics: one is a gradual change of the current in the subthreshold region, the other is an increase of saturation current for $\tau < 10^{-4}$ ns or when not-ballistic current becomes relevant. In the most favorable case, a subthreshold slope of 140 mV/dec can be obtained.

In Fig. 4, we have highlighted the effect of $V_{\rm ds}$ and of the doping level of contacts. As expected, the main visible effect of increasing $V_{\rm ds}$ is a gradual degradation of the subthreshold slope, both in the fully ballistic case [Fig. 4(a) and (b)] and in the case of relaxation time $\tau = 10$ ps [Fig. 4(c) and (d)], from 84 mV/dec to 202 mV/dec. The reason is simply related to the increased accumulation of holes in the channel with increasing $V_{\rm ds}$, which implies a larger quantum capacitance of the channel and therefore a reduced control of the channel potential from the gate voltage.

Increasing the doping causes an increase of both the maximum current, due to an improved capacity of the source to inject electrons, and the minimum current. From Fig. 4, we draw the indication that by reducing doping at the contacts, we improve the current dynamics. As already noted, when the source–drain voltage exceeds the gap of the semiconducting channel ($V_{\rm ds} > 0.26$ V), the characteristics drastically degrade, since band-to-band tunneling current becomes comparable with the thermionic current, and hole accumulation in the channel inhibits channel control from the gate.

The increase of oxide thickness $t_{\rm ox}$ has mainly two effects, which can be associated to a reduction of the capacitive coupling between gate and channel; it increases the subthreshold slope S [as shown in Fig. 5(a)] and the opacity of the tunneling barriers (i.e., a larger λ). The former effect is more evident for

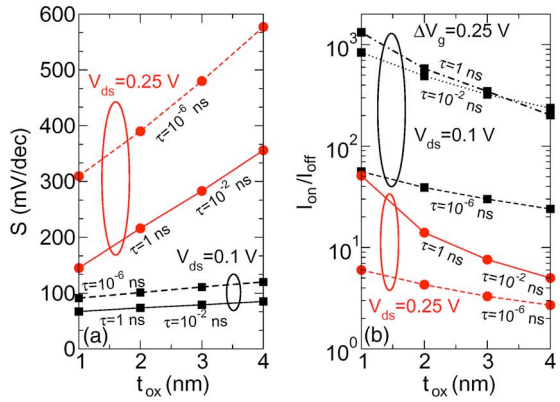

Fig. 5. (a) Subthreshold slope for $V_{\rm ds} = 0.1$ V and $V_{\rm ds} = 0.25$ V calculated with different relaxation time τ. (b) $I_{\rm on}/I_{\rm off}$ ratio for $V_{\rm ds} = 0.1$ V and $V_{\rm ds} = 0.25$ V calculated with different relaxation time τ.

$V_{\rm ds} = 0.25$ V, where the quantum capacitance is larger, instead, S is almost constant at about 75 mV/dec for $V_{\rm ds} = 0.1$ V and $\tau < 10^{-4}$ ns, instead for smaller τ, $S \sim 100$ mV/dec. Fig. 5(b) represents the $I_{\rm on}/I_{\rm off}$ ratio as a function of $t_{\rm ox}$ for $V_{\rm ds} = 0.1$ V and $V_{\rm ds} = 0.25$ V, calculated for a gate voltage range $\Delta V_g = 0.25$ V for different values of τ. Larger values of the $I_{\rm on}/I_{\rm off}$ ratio are observed for $\tau = 1$ ns.

From our analysis of the transfer characteristics, evaluated by varying three device parameters as $V_{\rm ds}$, α_D, and $t_{\rm ox}$, we stress the important result that for small $V_{\rm ds}$ and doping level [Fig. 4(a)] current is modulated by more than four orders of magnitude.

We have to stress also the main limitation of graphene on SiC: the energy gap of 0.26 eV coupled to a low effective mass results in a high band-to-band tunneling current $V_{\rm ds} >$ 0.26 V and so in an increase of the minimum current achievable. This limitation on $V_{\rm ds}$ affects the perspectives for digital circuit operation: in that case, we need $V_{\rm ds} = \Delta V_g$ and equal to the supply voltage. Even for optimized device parameters ($t_{\rm ox} = 1$ nm, $\alpha_D = 9.8 \times 10^{-3}$), and a supply voltage of 0.25 V, we obtain an $I_{\rm on}/I_{\rm off}$ ratio of 50, as can been seen from Fig. 5(b).

V. Conclusion

In this paper, we have investigated the performance of field-effect transistors based on epitaxial graphene on a SiC substrate with a semi-analytical model. We have shown that, for small $V_{\rm ds}$ and doping level, current is modulated by more than four orders of magnitude; this is a main improvement with respect to other graphene-based devices [10], [11], [23], [24]. Comparable results can be obtained only with carbon nanotubes or graphene nanoribbons, but only with the postselection of the devices after fabrication (for proper chirality and/or width). In the case of graphene on SiC, lithography and device patterning are certainly not prohibitive. A steep subthreshold behavior ($S = 67$ mV/dec) can be obtained for small $V_{\rm ds} = 0.1$ V, when the accumulation of holes in the channel is inhibited, and a larger current ratio, in excess of 10^3, can be obtained for a gate voltage window of 0.25 V. For digital applications, the limiting factor is represented by the small voltage drop applicable to the channel, being limited by the energy gap (0.26 eV) of the semiconducting material. With optimized device parameters we have obtained a subthreshold slope of ≈140 mV/dec and an $I_{\rm on}/I_{\rm off}$ equal to 50, with a supply voltage of 0.25 V and $\tau = 1$ ns. This falls short of the requirements of the International Technology Roadmap for Semiconductors (ITRS), which requires $I_{\rm on}/I_{\rm off} \approx 10^4$ [25]. The ITRS requirements are instead respected by the graphene-on-SiC Tunnel Field-Effect Transistors [26], with $I_{\rm on}/I_{\rm off}$ ratios exceeding 10^4 even with a low supply voltage of 0.15 V for devices with gate length down to 30 nm.

Finally, we believe that graphene on SiC is very promising as a channel material for FETs, and much attention has to be put on the mechanisms capable to suppress hole injection also at larger $V_{\rm ds}$, that would allow to improve the subthreshold swing and obtain a good $I_{\rm on}/I_{\rm off}$ also with a small applied voltage, and on its use in tunnel FETs, where its low gap and low effective mass can be turned into an advantage.

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