

Barrier Lowering and Backscattering Extraction in Short-Channel MOSFETs

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Abstract—In this paper, we propose a fully experimental method to extract the barrier lowering in short-channel saturated MOSFETs using the Lundstrom backscattering transport model in one-subband approximation and carrier degeneracy. The knowledge of barrier lowering at the operative bias point in the inversion regime is of fundamental importance in device scaling. At the same time, we also obtain an estimate of the backscattering ratio and the saturation inversion charge. With respect to previously reported works on extraction of transport parameters based on the Lundstrom model, our extraction method is fully consistent with it, whereas other methods make a number of approximations in the calculation of the saturation inversion charge, which are inconsistent with the model. The proposed experimental extraction method has been validated and applied to results from device simulation and measurements on short-channel poly-Si/SiON gate nMOSFETs with gate lengths down to 70 nm. Moreover, we propose an extension of the backscattering model to the case of 2-D geometries (e.g., bulk MOSFETs). We found that, in this case, backscattering is governed by the carrier transport in a few nanometers close to the silicon/oxide interface and that the value of the backscattering ratio obtained with a 1-D approach can be significantly different from the real 2-D value.

Index Terms—Backscattering, barrier lowering, C - V measurements, device simulation.

I. INTRODUCTION

DUE TO THE continuous downscaling of MOSFET geometry, improved physical models are needed to accurately study the charge transport in the channel [1]–[8]. One of the simplest and most successful models was proposed by Lundstrom [2] on the basis of Natori's theory for ballistic MOSFETs [1]. In his *backscattering* model, charge transport in the channel is regulated by the injection of the near-equilibrium thermal carriers at the top of the source–channel potential barrier (the virtual source). Only a fraction of the injected carriers reaches the drain side due to scattering in the channel. The ratio of the backscattered current to the total current injected by the virtual source is the backscattering coefficient.

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The backscattering coefficient plays a pivotal role in understanding the scalability of a given technology (material and/or architecture). Since a wide range of technology options are currently under study to meet performance targets as scaling continues, the backscattering coefficient is gaining more and more popularity, and experimental procedures for its accurate estimation are strongly required [9]–[12].

Most of the measurements of the backscattering ratio have been done by using the method proposed by Chen *et al.* [9], where backscattering is extracted by measuring the saturation drain current at different temperatures [13]–[17]. However, as it has been discussed by Zilli *et al.* [18], the method accounts for a number of assumptions that strongly affect the value of the extracted backscattering. A more reliable method has been proposed by Lochtefeld *et al.* [10], [11], where the saturation inversion charge is obtained from the measurement of the gate-to-channel capacitance corrected for drain-induced barrier lowering (DIBL). However, because no experimental method exists to extract the DIBL at the specified bias point in the inversion regime, the charge is calculated by using a DIBL extracted in the subthreshold regime where it is easily calculated as a simple shift of the gate voltage for a constant drain current. Because the DIBL is generally a function of bias point, the extracted value of backscattering can be sensibly affected.

Differently, in this paper, we propose a fully experimental method that uses the correct DIBL, and it allows the extraction of barrier lowering directly in the inversion regime, which is of fundamental importance for device scaling, obtaining at the same time an estimation of the backscattering ratio and of the saturation inversion charge. Secondary transport parameters like injection velocity and mean free path can be evaluated as a direct consequence.

The remainder of this paper is divided as follows. In Section II, the Lundstrom backscattering model is discussed. In this section, we also extend the model to the case of a 2-D geometry. In Section III, the method proposed by Lochtefeld *et al.* for the backscattering ratio extraction is discussed. In Section IV, the proposed method is presented, and in Section V, it is exemplified through application to 2-D quantum-corrected device simulations and to measurements on short-channel poly-Si/SiON gate nMOSFETs.

II. BACKSCATTERING MODEL

Saturation backscattering coefficient (r_{sat}) is defined as the ratio of the negative-directed current (I^-) at the virtual

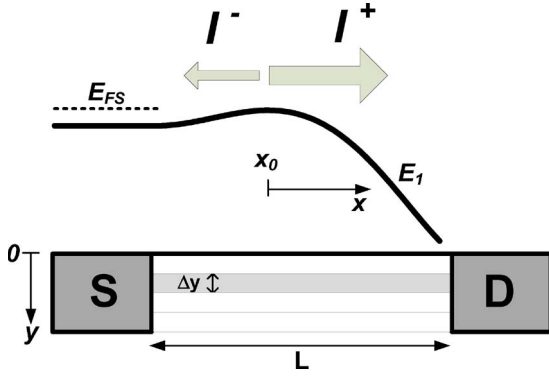


Fig. 1. (Top) Subband energy profile in saturation along the channel direction x . Backscattering is defined as the ratio of the negative-directed current (I^-) to the positive-directed current (I^+) evaluated at the virtual source (x_0), which is the x position corresponding to the maximum of energy. (Bottom) Backscattering in a 2-D geometry is evaluated by dividing the channel along the vertical y -direction into thin slice Δy . The 1-D model is used to calculate the local values for r_{sat} , I^- , and I^+ into each slice, and the total 2-D backscattering is evaluated through (7).

source (x_0) to the positive-directed current (I^+) at the virtual source (Fig. 1)

$$r_{\text{sat}} = \frac{I^-}{I^+} \quad (1)$$

$$I_{D,\text{sat}} = I^+ - I^- \quad (2)$$

where $I_{D,\text{sat}}$ is the drain current in saturation. The Lundstrom backscattering model in saturation is governed by the following equations [3]:

$$I_{D,\text{sat}} = qWN_{2D}v_{\text{th}}\mathfrak{S}_{1/2}(\eta_{\text{sat}})\frac{1-r_{\text{sat}}}{2} \quad (3)$$

$$Q_{\text{sat}} = qN_{2D}\frac{1+r_{\text{sat}}}{2}\mathfrak{S}_0(\eta_{\text{sat}}) \quad (4)$$

where q is the electron charge; W is the device width; $N_{2D} = kT(gm_{\text{DOS}}/\pi\hbar^2)$ is the 2-D effective density of states, with k being the Boltzmann constant, T being the absolute temperature, g being the subband degeneracy, \hbar being the reduced Planck constant, and m_{DOS} being the effective electron mass for the density of states of the considered subband; $v_{\text{th}} = \sqrt{2kTm_C/(\pi m_{\text{DOS}}^2)}$ is the average 1-D thermal velocity, with m_C being the conduction effective electron mass for the considered subband; Q_{sat} is the inversion charge per unit area at the virtual source; $\mathfrak{S}_{1/2}$ (\mathfrak{S}_0) is the Fermi–Dirac integral on the order of one-half (zero); and $\eta_{\text{sat}} = (E_{\text{FS}} - E_1)/kT$ is the energy distance (in units of kT) of the populated subband (E_1) with respect to the source quasi Fermi level (E_{FS}). The model is intrinsically 1-D (along the channel direction), and for this reason, the theory has been developed mainly for thin double-gate (DG) devices. Moreover, the Lundstrom model assumes that only one subband (E_1) is populated. This approximation is good, specifically for high transverse fields. An empirical approach to take into account multiband occupation has been proposed by Barral *et al.* [12] in the case of DG/SOI devices. In this paper, to validate the proposed method, also in the case of bulk devices, we use a 2-D approach for calculating the backscattering ratio.

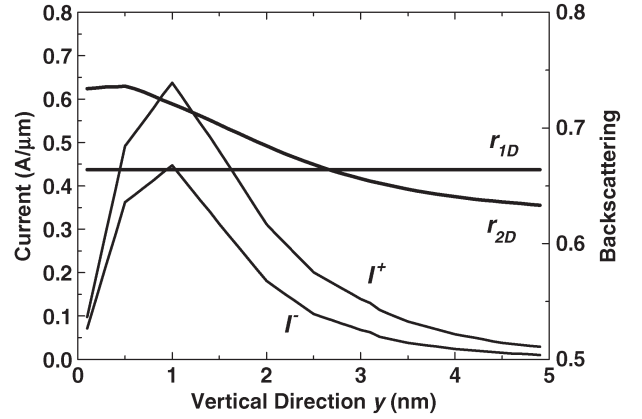


Fig. 2. I^- , I^+ , r_{1D} , and r_{2D} calculated as a function of vertical depth y (Fig. 1). The currents I^+ and I^- have a maximum close to the interface and decrease rapidly going far from it. r_{2D} is the cumulative 2-D backscattering coefficient evaluated through (7) as a function of vertical depth y . As expected, r_{2D} is significantly affected by the charge transport in a region of few nanometers close to the interface. r_{1D} is the backscattering value obtained using (3) and (4), with Q_{sat} being evaluated as the sum of charges in each slice [Fig. 1 and (5)].

A. Extension to a 2-D Geometry

As stated earlier, the backscattering model is 1-D and based on a subband description while we need to calculate r_{sat} in a 2-D geometry and a quantum-corrected semiclassical simulation. To serve this purpose, we propose a straightforward extension of the Lundstrom backscattering model for a 2-D semiclassical device. Indeed, in a 2-D semiclassical device, the position of the virtual source along the longitudinal direction (x) depends on the position of the plane along the vertical (y) axis. We divide the channel, along the y -direction, into thin slices of length L (the channel length) and thickness Δy (see Fig. 1). For each slice, we find the position of the virtual source $x_0(y)$, and we calculate the local charge density and the local current as

$$Q(y) = q \int_y^{y+\Delta y} n(x_0, y') dy' \quad (5)$$

$$I_D(y)/W = \int_y^{y+\Delta y} J_D(x_0, y') dy' \quad (6)$$

where n is the electron concentration and J_D is the current density. Now, the 1-D model [(3) and (4)] can be used within the slice, getting the local values for $Q(y)$, $I_D(y)$, and $r(y)$. By solving (1) and (2) within the slice, we can also calculate the local values for $I^+(y)$ and $I^-(y)$. Now, the 2-D backscattering ratio can be calculated as

$$r_{2D} = \frac{\sum_{y'} I^-(y')}{\sum_{y'} I^+(y')} \quad (7)$$

Fig. 2 shows the results of device simulation performed on short-channel silicon devices ($L = 70$ nm, $t_{\text{ox}} = 1.2$ nm) biased in saturation. As expected, the currents I^+ and I^- have

a maximum close to the interface (~ 1 nm), where the charge also has a maximum, and decrease rapidly going far from it. r_{2D} is the cumulative 2-D backscattering coefficient evaluated through (7) as a function of integration depth along the vertical direction y . As expected, it can be observed from Fig. 2 that r_{2D} is significantly affected by the charge transport in a region of few nanometers close to the interface, while it becomes constant far from it. It is difficult to do a fair comparison between r_{2D} with the value of the backscattering calculated using a 1-D assumption (r_{1D}) because a question arises about the correct definition of Q_{sat} in a 2-D geometry. However, if we evaluate Q_{sat} as the sum of the charges at $x_0(y)$ in each slice [(5)], we can calculate r_{1D} through (3) and (4). Fig. 2 shows that the value of the backscattering ratio obtained with a 1-D method (r_{1D}) can be significantly different from the real 2-D value (r_{2D}).

III. LOCHTEFELD METHOD FOR BACKSCATTERING EXTRACTION

In the Lochtefeld method [10], [11], to extract the backscattering coefficient in a short-channel device, the saturation inversion charge is estimated by integration of the gate-to-channel capacitance (C_{GC})

$$Q_{\text{sat}} = \int_{-\infty}^{V_G + \Delta V_G} C_{GC}(V) dV \quad (8)$$

where V_G is the gate voltage of the specified bias point and ΔV_G is a correction term. Because it is difficult to measure C_{GC} in a short-channel device due to parasitic capacitances (overlap and instrumentation), C_{GC} is measured in a longer reference device so that ΔV_G includes corrections for the threshold-voltage (V_T) roll-off and for the DIBL. As stated in the Introduction, the DIBL is evaluated in the subthreshold regime where it is easily calculated as a simple shift of the gate voltage for a constant drain current. Fig. 3 shows the barrier lowering simulated (expected DIBL) as a function of gate bias point. This number has been calculated by taking the difference of the potentials at the virtual source and at the maximum of the charge (~ 1 nm far from the interface) for cases $V_D = 1$ V and $V_D = 50$ mV, where V_D is the drain-to-source voltage. It is apparent that the DIBL is a strong function of bias point, and in particular, it is totally different in subthreshold with respect to the inversion regime affecting the calculated inversion charge. This is due to the bias dependence of the capacitive channel-drain coupling, which is a component of the bulk capacitance. In fact, the shape of the DIBL as a function of gate voltage resembles the shape of the gate capacitance as a function of gate voltage. However, some authors have reported that a DIBL in the subthreshold regime is sometimes sufficient to reproduce device characteristics [21]. Once that Q_{sat} is estimated, η_{sat} is calculated from

$$Q_{\text{sat}} = qN_{2D}\mathfrak{S}_0(\eta_{\text{sat}}). \quad (9)$$

From the knowledge of η_{sat} and measuring the saturation drain current, backscattering is extracted by (3). Let us note that

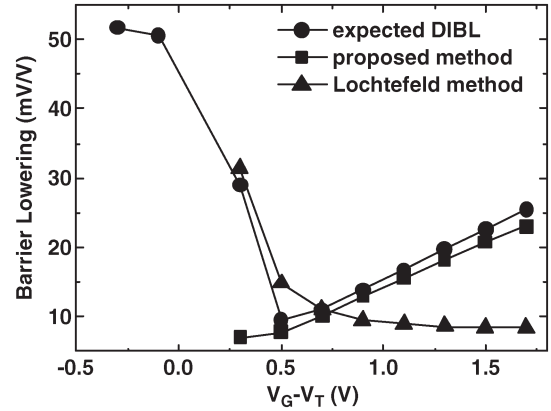


Fig. 3. Barrier lowering simulated as a function of gate bias with the proposed method, the Lochtefeld method, and the one expected, calculated by taking the difference of the potentials at the virtual source and at the maximum of the charge (~ 1 nm far from the interface) for cases $V_D = 1$ V and $V_D = 50$ mV. The simulated devices are silicon n-MOSFETs with poly-Si gate, bulk doping of 10^{18} cm $^{-3}$, oxide thickness $t_{\text{ox}} = 1.2$ nm, and gate length $L = 70$ nm. The expected DIBL is a strong function of bias point. The DIBL calculated with our method matches very well with the expected DIBL, while the value calculated with the Lochtefeld procedure underestimates strongly the expected value showing a strong inconsistency with the subthreshold expected DIBL used to calculate the inversion charge.

(9) contains the relationship between charge and potential when $V_D = 0$, while the correct equation that should be used is (4). In fact, (4) reduces to (9) when $r_{\text{sat}} = 1$.

IV. PROPOSED METHOD FOR BARRIER LOWERING AND BACKSCATTERING EXTRACTION

The proposed method is based on directly using (3) and (4), which define the backscattering model. In addition, the term Q_{sat} is estimated as

$$Q_{\text{sat}} = Q_0 + \int_{V_G}^{V_G + \frac{kT}{q}\Delta\eta} C_{GC}(V) dV \quad (10)$$

where $\Delta\eta = \eta_{\text{sat}} - \eta_0$, η_0 is the value of η at equilibrium ($V_D = 0$) extracted from $Q_0 = qN_{2D}F_0(\eta_0)$. Q_0 is the equilibrium charge extracted from CV measurement corrected for the V_T roll-off. Substituting (10) into (4), one obtains an equation in the two unknowns $\Delta\eta$ and r_{sat}

$$Q_0 + \int_{V_G}^{V_G + \frac{kT}{q}\Delta\eta} C_{GC}(V) dV = qN_{2D} \frac{1 + r_{\text{sat}}}{2} \mathfrak{S}_0(\eta_0 + \Delta\eta). \quad (11)$$

By solving the nonlinear system [(3) and (11)], one obtains both r_{sat} and $\Delta\eta$. The DIBL is simply represented by $kT/q \cdot \Delta\eta$. Let us note that the proposed method is fully consistent with the backscattering model because (3) and (4) are used. Two main differences can be found with respect to the Lochtefeld method: 1) the DIBL correction in the charge calculation is done directly using the correct barrier lowering at the specified bias point in the inversion regime and not in the subthreshold regime, and 2) scattering is included in the charge calculation [the term $(1 + r_{\text{sat}})/2$ in (11)].

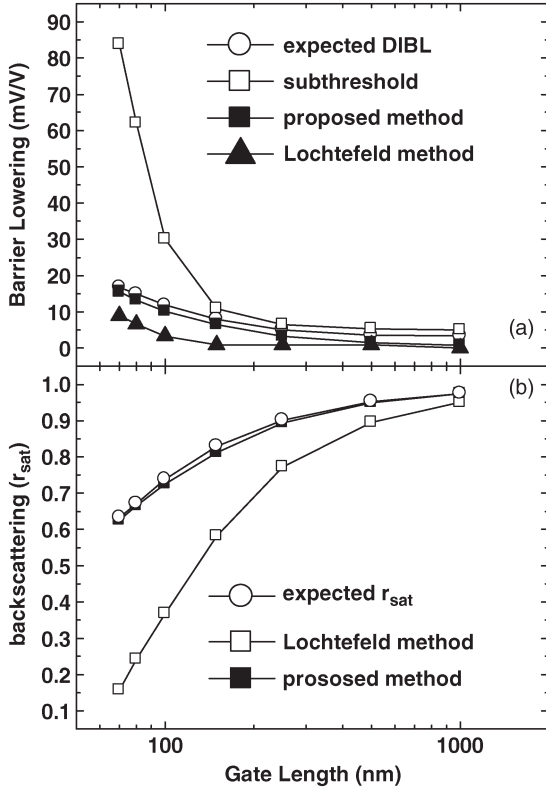


Fig. 4. (a) Simulated barrier lowering and (b) backscattering in 2-D short-channel poly-Si gate nMOSFETs with $t_{\text{ox}} = 1.2$ nm at biases $V_G - V_{T,\text{LONG}} = 1$ V and $V_D = 1$ V, where V_G is fixed and $V_{T,\text{LONG}}$ is the V_T of the long reference device. It is apparent that the values extracted with the proposed method match very well with the expected values directly obtained from the simulation using the procedure discussed in Section II-A, whereas the Lochtefeld method overestimates the barrier lowering. Moreover, the DIBL extracted with the Lochtefeld method is inconsistent with the subthreshold expected DIBL used to calculate the inversion charge.

V. VALIDATION BY NUMERICAL SIMULATION AND MEASUREMENTS

A comparison of the accuracy of the Lochtefeld method and of the proposed method is made through 2-D density gradient device simulation using Medici device simulator [19]. To serve this purpose, in Fig. 4(a) and (b), we compare, for different gate lengths, the expected values of barrier lowering (calculated as discussed in Section III) and of backscattering [calculated by (7)] obtained directly from simulation with the ones extracted by applying the Lochtefeld method and the proposed method on the simulated I - V and C - V characteristics. Moreover, the DIBL calculated in the subthreshold regime is plotted. The simulated devices are silicon n-MOSFETs with poly-Si gate, bulk doping of 10^{18} cm^{-3} , and oxide thickness $t_{\text{ox}} = 1.2$ nm. Equilibrium Schrodinger-Poisson simulations show that 80% of the charge is confined in the first subband of the unprimed ladder $\Delta_2^{(1)}$ (see the inset in Fig. 6), thus justifying in part the one-subband approximation. N_{2D} and v_{th} [(3) and (4)] are calculated, for the considered subband, with $m_{\text{DOS}} = m_C = m_t = 0.19m_0$ and $g = 2$, where m_t is the transversal effective mass and m_0 is the electron free mass. Let us note the excellent agreement between the values of the expected DIBL and the DIBL extracted with our proposed method. The excellent agreement in barrier lowering extraction

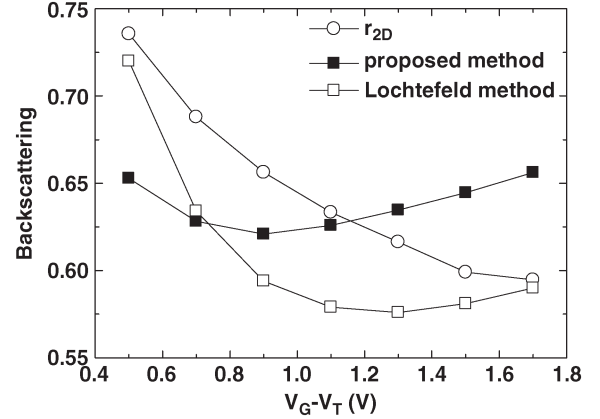


Fig. 5. Simulated backscattering with the Lochtefeld method, the proposed method and the expected value (r_{2D}) as discussed in Section II-A as a function of the gate overdrive.

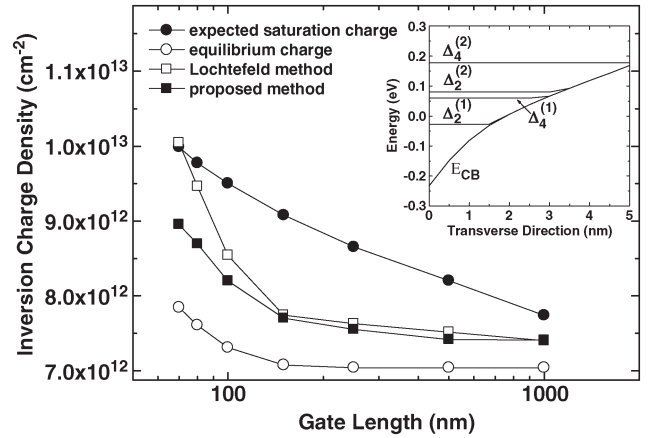


Fig. 6. Simulated inversion charge extracted with the Lochtefeld method, the proposed method, and the expected value as discussed in Section II-A. The Lochtefeld method gives a value closer to the expected value with respect to the charge obtained with the proposed method. This apparent advantage is due to the sum of two inconsistencies: the wrong DIBL correction and the assumption of $r_{\text{sat}} = 1$ in the charge calculation (9). In the inset, the results of Schrodinger-Poisson simulations show that 80% of the charge is confined in the first subband of the unprimed ladder ($\Delta_2^{(1)}$).

is maintained also by changing the gate voltage (Fig. 3). The inconsistency of the Lochtefeld method is apparent when one compares the DIBL used to calculate the charge (expected DIBL in the subthreshold range) and the DIBL calculated as $kT/q \cdot \Delta\eta$ (Lochtefeld method in Fig. 3), which is, in any case, much smaller with respect to the expected value. A comparison between the backscattering extracted with the proposed method and the one extracted with the Lochtefeld method is difficult to do because both methods are intrinsically 1-D while the expected backscattering is 2-D as discussed in Section II-A (see the difference between 2-D and 1-D backscattering as function of the gate voltage in Fig. 5). We repeat that the comparison is not totally fair, but we are confident that the value extracted with our method is more consistent because it has been extracted by directly using the Lundstrom backscattering equations (3) and (4). Fig. 6 shows the same type of comparison for the inversion charge. The expected saturation charge has been calculated as discussed in Section II-A. The charge obtained from the Lochtefeld method gives a value closer to the expected

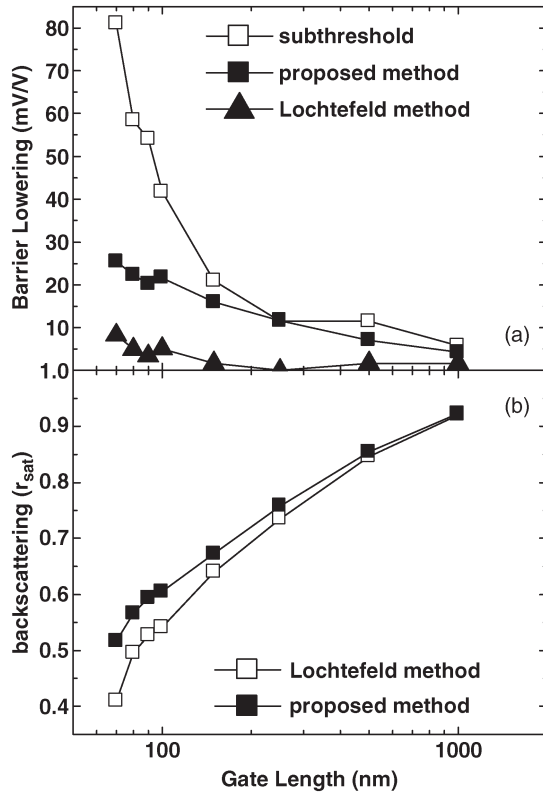


Fig. 7. (a) Barrier lowering and (b) backscattering extracted from measurements in short-channel poly-Si gate nMOSFETs with $t_{\text{ox}} = 1.2$ nm at biases $V_G - V_{T,\text{LONG}} = 1$ V and $V_D = 1$ V, where V_G is fixed and $V_{T,\text{LONG}}$ is the V_T of the long reference device. The observed trends are in agreement with device simulations (Fig. 4).

value with respect to the charge obtained with the proposed method. This apparent advantage is due to the sum of the two inconsistencies, as mentioned in Section IV. First, the charge is calculated with a DIBL that is higher with respect to the expected DIBL, i.e., with a DIBL in the subthreshold regime instead of a DIBL in the inversion regime. This error should produce a charge that is higher with respect to the expected charge. Second, (9) is used in the Lochtefeld method instead of (4), i.e., the increase in the charge from equilibrium to saturation is considered as due only to an electrostatic effect, and scattering is neglected [the term $(1 + r_{\text{sat}})/2$ in (4)]. Because scattering lowers the charge [$(1 + r_{\text{sat}})/2 < 1$], the value obtained with the Lochtefeld method appears lower with respect to the expected value. In any case, both methods are not able to reproduce well the expected inversion charge because 2-D electrostatics is neglected in the Lundstrom model and because of the one-subband approximation. Experimental measurements have been performed on short-channel nMOSFETs with electrical parameters similar to those used in device simulation. The behavior of the DIBL and of the backscattering ratio extracted from experiments in Fig. 7(a) and (b) is in good agreement with that of the same parameters obtained from the simulations reported in Fig. 4(a) and (b), so that we do not spend any further comment here. The gate lengths reported in Fig. 7 are the mask lengths. The V_T roll-off used to calculate Q_0 is calculated by using the maximum transconductance method for threshold-voltage extraction [20]. Moreover, the term ΔV_G

in (10) includes an additional correction term ($-R_S I_{D,\text{sat}}$) due to the series resistance R_S [10], which is extracted by a common linear extrapolation technique [20].

VI. CONCLUSION

Standard methods to extract backscattering need the inversion charge at the virtual source, which is difficult to estimate in saturated short-channel devices. This charge is usually measured in a longer reference device by a CV and after it is corrected for V_T roll-off and DIBL. DIBL correction is usually done in the subthreshold regime with the well-known method of gate voltage shift for a constant drain current. Because backscattering is calculated in inversion, the DIBL should be calculated in inversion and not in subthreshold as is usually done. In this paper, we have shown that using the DIBL in subthreshold may lead to severe errors in barrier lowering extraction and, hence, in backscattering and saturation inversion charge extraction. Moreover, standard methods neglect the influence of scattering in the calculation of the saturation inversion charge. We have proposed a fully experimental method to extract the DIBL and, hence, the backscattering and saturation inversion charge in short-channel MOSFETs, which is completely consistent with the backscattering model, as it must be. The proposed experimental extraction method has been validated and applied to results from device simulation and measurements on short-channel poly-Si/SiON gate nMOSFETs with gate lengths down to 70 nm. Moreover, we have proposed an extension of the backscattering model to the case of 2-D geometries. We found that backscattering is governed by the carrier transport in a few nanometers at the silicon/oxide interface and that the value of the real 2-D backscattering ratio can be sensibly affected by a 1-D method when bulk MOSFETs are investigated.

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REFERENCES

- [1] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *J. Appl. Phys.*, vol. 76, no. 8, pp. 4879–4890, Oct. 1994.
- [2] M. S. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Lett.*, vol. 18, no. 7, pp. 361–363, Jul. 1997.
- [3] A. Rahman and M. S. Lundstrom, "A compact scattering model for the nanoscale double-gate MOSFET," *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 481–489, Mar. 2002.
- [4] E. Fuchs, P. Dollfus, G. Le Carval, S. Barraud, D. Villanueva, F. Salvetti, H. Jaouen, and T. Skotnicki, "A new backscattering model giving a description of the quasi-ballistic transport in nano-MOSFET," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2280–2289, Oct. 2005.
- [5] G. Mugnaini and G. Iannaccone, "Physic-based compact model of nanoscale MOSFETs—Part I: Transition from drift-diffusion to ballistic transport," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1795–1801, Aug. 2005.
- [6] G. Mugnaini and G. Iannaccone, "Physic-based compact model of nanoscale MOSFETs—Part II: Effects of degeneracy on transport," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1802–1806, Aug. 2005.
- [7] M. J. Chen and L. F. Lu, "A parabolic potential barrier-oriented compact model for the $k_B T$ layer's width in nano-MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 5, pp. 1265–1268, May 2008.

- [8] G. Giusi, G. Iannaccone, M. Mohamed, and U. Ravaioli, "Study of warm electron injection in double gate SONOS by full band Monte Carlo simulation," *IEEE Electron Device Lett.*, vol. 29, no. 11, pp. 1242–1244, Nov. 2008.
- [9] M. J. Chen, H.-T. Huang, K.-C. Huang, P.-N. Chen, C.-S. Chang, and C. H. Diaz, "Temperature dependent channel backscattering coefficients in nanoscale MOSFETs," in *IEDM Tech. Dig.*, Dec. 2002, pp. 39–42.
- [10] A. Lochtefeld and D. A. Antoniadis, "On experimental determination of carrier velocity in deeply scaled nMOS: How close to the thermal limit?" *IEEE Electron Device Lett.*, vol. 22, no. 2, pp. 95–97, Feb. 2001.
- [11] A. Dobbie, B. De Jaeger, M. Meuris, T. E. Whall, E. H. C. Parker, and D. R. Leadley, "Channel backscattering characteristics of high performance germanium pMOSFETs," in *Proc. 9th Int. Conf. Ultimate Integr. Silicon*, 2008, pp. 7–10.
- [12] V. Barral, T. Poiroux, J. Saint-Martin, D. Munteanu, J. L. Autran, and S. Deleonibus, "Experimental investigation on the quasi-ballistic transport: Part I—Determination of a new backscattering coefficient extraction methodology," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 408–419, Mar. 2009.
- [13] H.-N. Lin, H.-W. Chen, C.-H. Ko, C.-H. Ge, H.-C. Lin, T.-Y. Huang, and W.-C. Lee, "Channel backscattering characteristics of uniaxially strained nanoscale CMOSFETs," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 676–678, Sep. 2005.
- [14] H.-N. Lin, H.-W. Chen, C.-H. Ko, C.-H. Ge, H.-C. Lin, T.-Y. Huang, and W.-C. Lee, "Channel backscattering characteristics of strained PMOSFETs with embedded SiGe source/drain," in *IEDM Tech. Dig.*, 2005, pp. 141–144.
- [15] T.-Y. Liow, K.-M. Tan, H.-C. Chin, R. T. P. Lee, C.-H. Tung, G. S. Samudra, N. Balasubramanian, and Y.-C. Yeo, "Carrier transport characteristics of sub-30 nm strained N-channel FinFETs featuring silicon-carbon source/drain regions and methods for further performance enhancement," in *IEDM Tech. Dig.*, 2006, pp. 1–4.
- [16] V. Barral, T. Poiroux, M. Vinet, J. Widiez, B. Previtali, P. Grosgeorges, G. Le Carval, S. Barraud, J. L. Autran, D. Munteanu, and S. Deleonibus, "Experimental determination of the channel backscattering coefficient on 10–70 nm metal gate double gate transistors," *Solid State Electron.*, vol. 51, no. 4, pp. 537–542, Apr. 2007.
- [17] Y. J. Tsai, S. S. Chung, P. W. Liu, C. H. Tsai, Y. H. Lin, C. T. Tsai, G. H. Ma, S. C. Chien, and S. W. Sun, "The channel backscattering characteristics of sub-100 nm CMOS devices with different channel/substrate orientations," in *Proc. Int. Symp. VLSI-TSA*, 2007, pp. 1–2.
- [18] M. Zilli, P. Palestri, D. Esseni, and L. Selmi, "On the experimental determination of channel back-scattering in nanoMOSFETs," in *IEDM Tech. Dig.*, 2007, pp. 105–108.
- [19] [Online]. Available: <http://www.synopsys.com/Tools/TCAD/DeviceSimulation/Pages/TaurusMedici.aspx>
- [20] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. New York: Wiley-Interscience, 2006.
- [21] A. Khakifirooz, O. M. Nayfeh, and D. Antoniadis, "A simple semiempirical short-channel MOSFET current–voltage model continuous across all regions of operation and employing only physical parameters," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1674–1680, Aug. 2009.



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