An Approach Based on Sensitivity Analysis for the Evaluation of Process Variability in Nanoscale MOSFETs

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***Abstract*—We propose an approach to evaluate the effect on the threshold-voltage dispersion of nanoscale metal–oxide–semiconductor field-effect transistors (MOSFETs) of line-edge roughness, surface roughness, and random dopant distribution. The methodology is fully based on parameter sensitivity analysis, performed by means of a limited number of technology computer-aided design simulations or analytical modeling. We apply it to different nanoscale transistor structures, i.e., bulk 45-nm n-channel, 32-nm ultrathin-body silicon-on-insulator, and 22-nm double-gate MOSFETs. In all cases, our approach is capable of reproducing with very good accuracy the results obtained through 3-D atomistic statistical simulations at a small computational cost. We believe that the proposed approach can be a powerful tool to understand the role of the main variability sources and to explore the device design parameter space.**

***Index Terms*—Metal–oxide–semiconductor field-effect transistor (MOSFET), mismatch, parameter fluctuations, variability.**

I. Introduction

Intrinsic process variability is broadly considered as one of the main factors limiting complementary metal–oxide–semiconductor (CMOS) technology scaling [1]. The increased variability of device electrical parameters is already slowing down the adoption of the latest technology nodes by analog and mixed-signal designers. For this reason, the statistical dispersion of transistor characteristics is one of the main factors to consider in the development of current and next CMOS technology nodes. Indeed, one of the main reasons why ultrathin-body (UTB) MOS field-effect transistors (MOSFETs) with undoped channel and metal gate are considered for the next CMOS technology nodes is the suppression of random dopant distribution (RDD) as a source of threshold-voltage variability. The metal gate enables threshold-voltage adjustment in the absence of dopants in the channel. Alternative device structures such as UTB silicon-on-insulator (SOI) and multiple-gate MOSFETs have been also precisely considered because they seem more promising for managing the statistical dispersion of transistor characteristics.

Methodology and proper modeling tools to quantitatively evaluate the variability of device electrical parameters as a function of device structure are therefore essential to guide the device design and optimization.

In time, analytical models have been proposed to evaluate the impact of threshold-voltage dispersion due to RDD [2], [3] and line-edge roughness (LER) [4]. Analytical models are fundamental for understanding the main relevant physical mechanisms but are typically limited to simplified and idealized structures. Statistical simulations are very powerful for a quantitative assessment of the dispersion of electrical parameters of realistic devices [5]–[8] and also enable the use of doping profiles and geometry carefully calibrated with experiments. On the other hand, statistical simulations are very demanding from the computational point of view and may sometimes represent a "brute force" approach to an issue more easily accessible with other means [9], [10].

We believe that a complete analytical or quasi-analytical approach can provide important insights on the main sources of variability and the ways to minimize their effect and can enable a thorough exploration of the device design space, which would be prohibitive with a statistical simulation approach. In this paper, we propose an approach to evaluate the effect on the threshold-voltage variability due to RDD, LER, and surface roughness (SR) fully based on a limited number of 2-D technology computer-aided design (TCAD) simulations to perform parameter sensitivity analysis.

We apply our proposed approach to three template devices, i.e., 32-nm UTB SOI and 22-nm double-gate MOSFETs adopted within the EC Pulling the limits of nanoCMOS electronics (PULLNANO) project as template devices, and one bulk 45-nm n-channel MOSFET with a polysilicon gate length of 42 nm, an oxide thickness of 1.7 nm, and a width of 45 nm. The 32- and 22-nm templates are shown in Fig. 1 (details can be found in [11]), whereas the 45-nm template is illustrated in [12]. The choice of the template devices is due to the availability of data from statistical atomistic simulations on the very same templates [8], [12], which enables us to compare results obtained with our proposed approach.

II. Methodology

The approach we propose requires the identification of the relevant quantities that translate process variability into the

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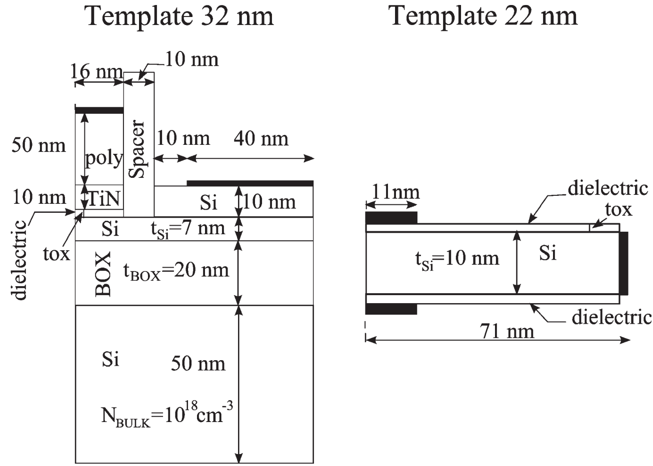


Fig. 1. Template structures for the (left) 32-nm UTB SOI and (right) 22-nm double-gate MOSFETs. The device is symmetrical. Doping profiles for source and drain are described in [11]. The effective oxide thickness t_{ox} is 1.2 nm for the 32-nm template and 1.1 nm for the 22-nm template.

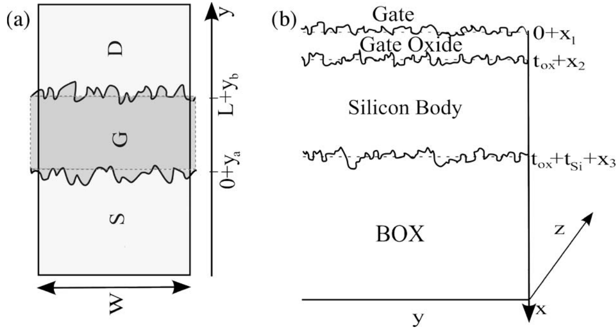


Fig. 2. (a) Top view of the active area highlighting the gate LER. (b) Layered structure highlighting the interface roughness between adjacent layers in the 32-nm template. The y-axis runs along the channel length direction, the x-axis is perpendicular to the device plane, and the z-axis runs along the channel width.

dispersion of electrical parameters. It involves the following three steps:

First, we need to express all process and geometry variability sources in terms of a set of synthetic parameters.

Then, we need to identify the *independent* parameters.

Finally, we use sensitivity analysis to evaluate the contribution to the dispersion of electrical parameters (e.g., the threshold voltage V_{th}) of each independent source. This step is based on the assumption that the effect of each source is sufficiently small that first-order linearization is applicable. In the literature, nonlinear and cross terms have been explicitly evaluated, for example, through statistical simulations on 35-nm MOSFETs [13]; the variance of the threshold voltage due to combined effect has been shown to be equal to the sum of the variances due to individual effects, giving us confidence in the linear approximation.

A. Variability Due to LER and SR

As an example, let us consider the 32-nm device shown in Fig. 2, where the y-axis runs along the channel length direction, the x-axis is perpendicular to the device plane, and the z-axis runs along the channel width.

We can translate LER in terms of the dispersion of the average position of both gate edges along the y-axis ($y = 0 + y_1$ and $y = L + y_2$), as illustrated in Fig. 2(a). This, in turn, translates into gate length dispersion. In practice, the two rough edges are not completely independent, but here, for simplicity, we can assume that they are. SR is translated into the dispersion of the average position of the interface between adjacent layers; the offsets are x_1, x_2, and x_3 in Fig. 2(b).

We assume that parameters y_1, y_2, x_1, x_2, and x_3 are only affected by LER and SR and are physically independent. We start by considering the effect of the offset of the position between two adjacent Si-SiO_2 layers ($x_i, i = 1, 2, 3$). The first step is to evaluate variance $\sigma^2_{x_i}$ of x_i. In the case of the UTB SOI MOSFET, we should consider the fluctuations present in the bottom interface of the buried oxide, but these are practically irrelevant for our calculation.

Interface roughness leads to deviation from the nominal position of the interface between two layers that we can statistically describe as a random function $f(y, z)$ with zero-mean value and exponential autocorrelation $r(y_1, z_1, y_2, z_2) \equiv \langle f(y_1, z_1) f(y_2, z_2)\rangle$, characterized by mean square amplitude Δ_S and correlation length Λ_S, i.e.,

$$r(y_1, z_1, y_2, z_2) = \Delta_S^2 \exp\left(-\frac{\sqrt{(y_1 - y_2)^2 + (z_1 - z_2)^2}}{\Lambda_S}\right). \tag{1}$$

The average position of interface $\overline{f}$ for a given occurrence of a rough interface is

$$\overline{f} = \frac{1}{LW} \int_0^L dy \int_0^W dz f(y, z). \tag{2}$$

$\overline{f}$ has zero-mean value and variance given by

$$\sigma_f^2 =< \overline{f}^2 >= \frac{1}{L^2W^2} \int_0^L dy_1 \int_0^W dz_1 \times \int_0^L dy_2 \int_0^W dz_2 < f(y_1, z_1) f(y_2, z_2) > \tag{3}$$

which, using (1), can be written as

$$\sigma^2_{x_1} = \sigma^2_{x_2} = \sigma^2_{x_3} = \sigma^2_{\mathrm{SR}} = \frac{2\pi\Delta_S^2}{LW}\left[\Lambda_S^2 - e^{-\frac{\sqrt{L^2+W^2}}{\Lambda_S}} \Lambda_S \left(\Lambda_S + \sqrt{L^2 + W^2}\right)\right]. \tag{4}$$

where x_1, x_2, and x_3 in (4) are the average position of interfaces between adjacent layers, as indicated in Fig. 2.

In the common case $L, W \gg \Lambda_S$, (4) reduces to

$$\sigma^2_{\mathrm{SR}} = \frac{2\pi\Lambda_S^2\Delta_S^2}{LW}. \tag{5}$$

If, instead, we consider a Gaussian autocorrelation, as in [8] and [12], expressed as

$$r(x_1, y_1, x_2, y_2) = \Delta_S^2 \exp\left(-\frac{(x_2 - x_1)^2 + (y_2 - y_1)^2}{2\Lambda_S^2}\right). \tag{6}$$

Replacing (6) in (3), we find

$$\sigma_{\rm SR}^2 = \frac{2\pi\Lambda_S^2\Delta_S^2}{L^2W^2}\left[L\cdot erf\left(\frac{L}{\sqrt{2}\Lambda_S}\right)+\sqrt{\frac{2}{\pi}}\Lambda_S\left(e^{-\frac{L^2}{2\Lambda_S^2}}-1\right)\right] \cdot\left[Werf\left(\frac{W}{\sqrt{2}\Lambda_S}\right)+\sqrt{\frac{2}{\pi}}\Lambda_S\left(e^{-\frac{W^2}{2\Lambda_S^2}}-1\right)\right] \quad (7)$$

which again reduces to (5) if $L, W \gg \Lambda_S$.

We can express the variation of the threshold voltage in terms of thickness variations of different layers and then consider as independent physical quantities only x_1, x_2, and x_3, i.e.,

$$dV_{\rm th} = \frac{\partial V_{\rm th}}{\partial t_{\rm ox}}dt_{\rm ox} + \frac{\partial V_{\rm th}}{\partial t_{\rm Si}}dt_{\rm Si} + \frac{\partial V_{\rm th}}{\partial t_{\rm BOX}}dt_{\rm BOX}$$

$$dV_{\rm th} = \frac{\partial V_{\rm th}}{\partial t_{\rm ox}}(dx_2 - dx_1) + \frac{\partial V_{\rm th}}{\partial t_{\rm Si}}(dx_3 - dx_2) - \frac{\partial V_{\rm th}}{\partial t_{\rm BOX}}(-dx_3). \quad (8)$$

Then, using linearization and the hypothesis of the independence of the different parameters, we can write

$$\sigma_{V_{\rm th}\rm SR}^2 = \left(\frac{\partial V_{\rm th}}{\partial x_1}\right)^2\sigma_{x1}^2 + \left(\frac{\partial V_{\rm th}}{\partial x_2}\right)^2\sigma_{x2}^2 + \left(\frac{\partial V_{\rm th}}{\partial x_3}\right)^2\sigma_{x3}^2. \quad (9)$$

The partial derivatives can be expressed as

$$\frac{\partial V_{\rm th}}{\partial x_1} = -\frac{\partial V_{\rm th}}{\partial t_{\rm ox}}$$

$$\frac{\partial V_{\rm th}}{\partial x_2} = \frac{\partial V_{\rm th}}{\partial t_{\rm ox}} - \frac{\partial V_{\rm th}}{\partial t_{\rm Si}}$$

$$\frac{\partial V_{\rm th}}{\partial x_3} = \frac{\partial V_{\rm th}}{\partial t_{\rm Si}} - \frac{\partial V_{\rm th}}{\partial t_{\rm BOX}}. \quad (10)$$

As far as LER is concerned, we assume that the average edge position is a random function $g(z)$ with zero-mean value and an exponential autocorrelation function $r(d) \equiv \langle g(z)g(z+d)\rangle$ characterized by the correlation length Λ_L and the mean square amplitude Δ_L, i.e.,

$$r(d) = \Delta_L^2 e^{-|d|/\Lambda_L} \quad (11)$$

from which we can write

$$\sigma_f^2 =< \bar{g}^2 >=< \frac{1}{W^2}\int_0^W g(z_1)\,dz_1 \cdot \int_0^W g(z_2)\,dz_2 > . \quad (12)$$

Therefore, we find

$$\sigma_{y_a}^2 = \sigma_{y_b}^2 = \sigma_{\rm LER}^2 = \frac{2\Lambda_L\Delta_L^2}{W}\left\{1 - \frac{\Lambda_L}{W}\left[1-\exp\left(-W/\Lambda_L\right)\right]\right\}. \quad (13)$$

where y_a and y_b are the average gate edges indicated in Fig. 2.

If, instead, we consider the function Gaussian autocorrelation, then

$$r(d) = \Delta_L^2 e^{-\frac{d^2}{2\Lambda_L^2}}. \quad (14)$$

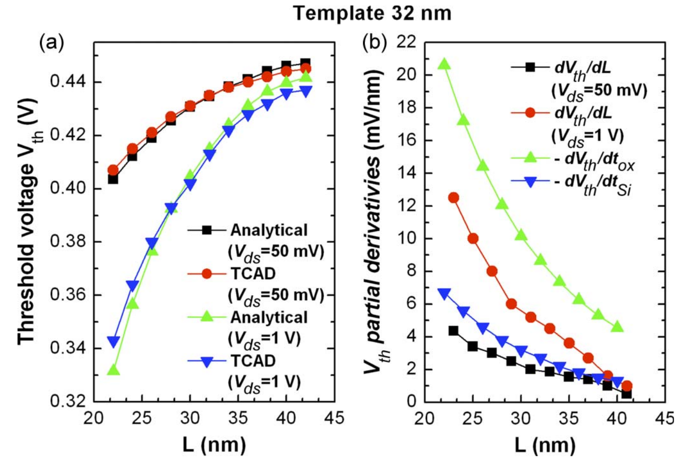


Fig. 3. Threshold voltage as a function of L from (a) analytical model and TCAD and (b) analytical partial derivatives of $V_{\rm th}$ of the 32-nm-template MOSFET.

Solving integral (12), we find

$$\sigma_{\rm LER}^2 = \frac{2\Delta_L^2\Lambda_L}{W^2}\left[\Lambda_L\left(e^{-\frac{W^2}{2\Lambda_L^2}}-1\right)+\sqrt{\frac{\pi}{2}}Werf\left(\frac{W}{\sqrt{2}\Lambda_L}\right)\right]. \quad (15)$$

The variance of $V_{\rm th}$ due to LER is

$$\sigma_{V_{\rm th}\rm LER}^2 = \left(\frac{\partial V_{\rm th}}{\partial y_1}\right)^2\sigma_{y_1}^2 + \left(\frac{\partial V_{\rm th}}{\partial y_2}\right)^2\sigma_{y_2}^2 = 2\left(\frac{\partial V_{\rm th}}{\partial L}\right)^2\sigma_{\rm LER}^2. \quad (16)$$

All required derivatives can be computed with TCAD simulations or—if the device structure is simple enough—with an appropriate analytical model.

As shown, if proper independent parameters are identified, the evaluation of the dispersion of the threshold voltage only requires the computation of a limited number of derivatives, each of which obtainable from a single-device simulation. Even using derivatives obtained from the TCAD, the computational cost of the procedure is extremely reduced with respect to a statistical simulation. The price to pay is the initial analysis of variability sources and the consequent assumptions.

The threshold voltage of the 32-nm-template MOSFET as a function of gate length is plotted in Fig. 3, where it is compared with results from the analytical model presented in the Appendix. $V_{\rm th}$ is defined as V_{GS} corresponding to the current of 10^{-5} A/μm as in [8]. The agreement is very good. In Fig. 4, we show the same comparison for the 22-nm-template device. The dependence on the gate length of the threshold voltage of the 45-nm MOSFET is shown in Fig. 5 for $V_{DS} = 50$ mV and 1.1 V. In the latter case, there is no analytical model because the doping profiles for different lengths are directly obtained from process simulations and cannot be described by a simple expression.

Now, we can use (9) and (16) to compute the variance of $V_{\rm th}$ due to LER and SR and to compare our results with those obtained with atomistic statistical simulations in [8] and [12].

For the sake of comparison, we assume, as in [8], for all rough interfaces a Gaussian autocorrelation function with the mean square amplitude $\Delta_S = 0.15$ nm and the correlation length $\Lambda_S = 1.8$ nm, which are close to values observed

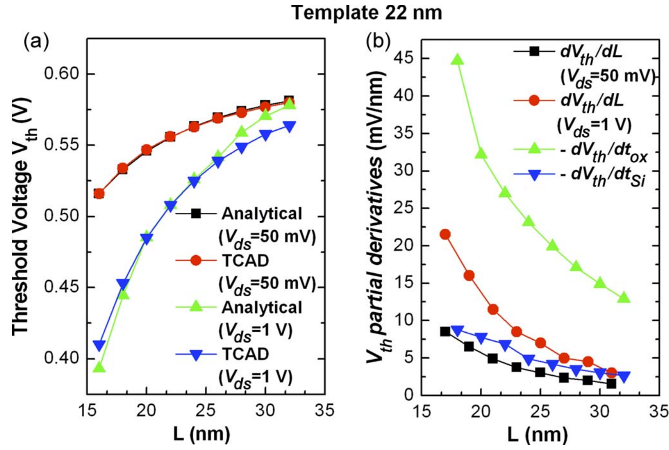


Fig. 4. Threshold voltage as a function of L from (a) analytical model and TCAD and (b) analytical partial derivatives of V_{th} for the 22-nm-template MOSFET.

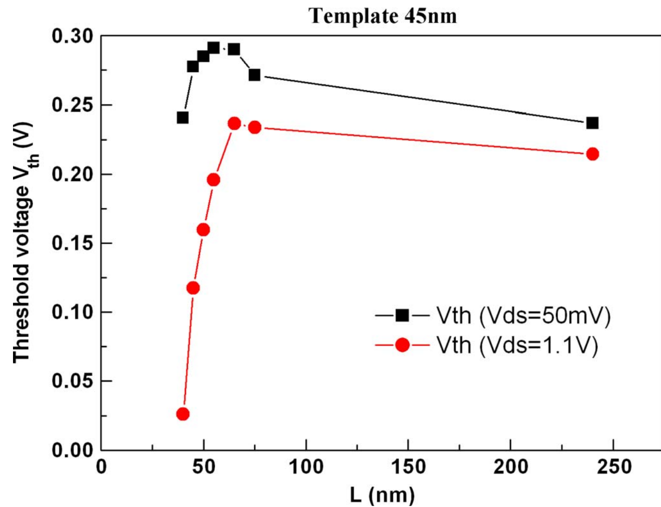


Fig. 5. Threshold voltage as a function of L for the 45-nm-template MOSFET, for two different values of V_{DS}.

from transmission electron microscopy measurements [14]. For LER, we assume a Gaussian autocorrelation function with $\Delta_L = 1.3$ nm and $\Lambda_L = 25$ nm for 32- and 22-nm templates, and as in [12], we assume a Gaussian autocorrelation function with $\Delta_L = 1.3$ nm and $\Lambda_L = 30$ nm.

Results are shown in Table I. The columns *An* and *TCAD* indicate results from our approach where the partial derivatives of V_{th} are analytically computed (as described in the Appendix) or with TCAD [15], respectively. The column *Stat.Sim* indicates results reported in [8] and [12]. As shown, the agreement for the LER data is always extremely good. Very good agreement is obtained between columns *An* and *TCAD*, for the effect of SR, for which data from [8] are not available.

B. Effect of RDD

In the case of RDD, the source of the threshold-voltage dispersion is the fluctuation of the dopant distribution in the active area. What matters is not only the total number of dopants in the active area but also their position. In any case, it is pretty intuitive that we do not need to know with atomistic precision the effect of dopant distribution on the threshold voltage.

TABLE I
STANDARD DEVIATION OF THE THRESHOLD VOLTAGE DUE TO LER AND SR FOR THE 32-AND 22-nm TEMPLATE MOSFETs AND TO LER FOR THE 45-nm MOSFET, OBTAINED WITH DIFFERENT METHODS

	Vds = 50 mV	Approach		
		An.	*TCAD*	*Stat.Sim. [8,12]*
32 nm	σ_{Vth} LER (mV)	*3.36*	*3.45*	*3.3*
	σ_{Vth} SR (mV)	*0.32*	*0.38*	*N/A*
22 nm	σ_{Vth} LER (mV)	*6.7*	*6.2*	*5.8*
	σ_{Vth} SR (mV)	*2.07*	*2.03*	*N/A*
45 nm	σ_{Vth} LER (mV)	-	*7.4*	*20*
	Vds = 1V (32nm; 22nm), 1.1V (45nm)	*Approach*		
		An.	*TCAD*	*Stat.Sim. [8,12]*
32 nm	σ_{Vth} LER (mV)	*9.25*	*9.47*	*8.6*
	σ_{Vth} SR (mV)	*0.94*	*0.85*	*N/A*
22 nm	σ_{Vth} LER (mV)	*15.8*	*15*	*13*
	σ_{Vth} SR (mV)	*6.1*	*6.26*	*N/A*
45 nm	σ_{Vth} LER (mV)	-	*22*	*33*

First, we can acknowledge that the mechanism is mainly governed by electrostatics; therefore, the impurity position along the width direction is of minor relevance. This allows us to simplify our analysis, considering only 2-D device structures. Indeed, statistical simulations with random dopants typically yield a family of parallel transfer characteristics, corresponding to a threshold-voltage dispersion independent of the inversion level in the channel. This means that percolation is hardly effective since it should strongly depend on the Debye length and, therefore, on the mobile charge density in the channel. An *ex post* verification of this assumption will be provided by comparing our results with 3-D statistical simulations.

Furthermore, we can assume that the effects of fluctuations of the number of dopants in different regions are small enough to linearly add up. For a given variation of dopant distribution $\Delta N_A(x, y, z)$ with respect to the nominal value, we can write the following expression for the variation of V_{th}:

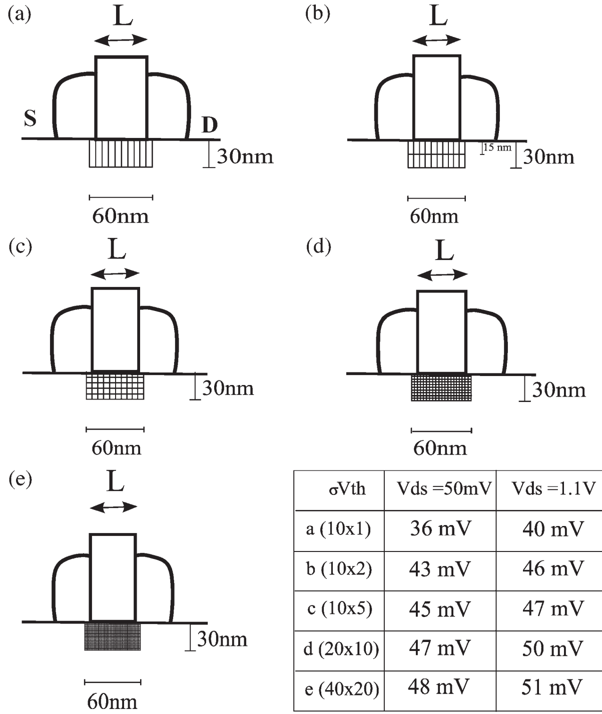
$$\Delta V_{\mathrm{th}} = \int K(x, y)\Delta N_A(x, y, z)dxdydz \tag{17}$$

where $K(x, y)$ has the role of a propagator or Green's function [16]. The expression requires the linearity assumption to hold. Let us notice that we are neglecting the dependence of K on z according to the aforementioned hypothesis.

To conveniently compute propagator K, we can assume that K is a smooth function of x and y and move from the continuum to a discrete space, partitioning the active area in small rectangular boxes, as shown in Fig. 6(a). Now, we can write

$$\Delta V_{\mathrm{th}} = \sum_i \Delta V_{\mathrm{th}_i} = \sum_i K_i \Delta N_i. \tag{18}$$

The sum runs over all boxes, ΔN_i is the variation of the number of dopants in box i, and ΔV_{th_i} is the threshold-voltage variation if only dopants in box i are varied.



σVth	Vds =50mV	Vds =1.1V
a (10x1)	36 mV	40 mV
b (10x2)	43 mV	46 mV
c (10x5)	45 mV	47 mV
d (20x10)	47 mV	50 mV
e (40x20)	48 mV	51 mV

Fig. 6. Different partitions used to evaluate the variance of the threshold voltage for the 45-nm MOSFET: (a) 10×1, (b) 10×2, (c) 10×5, (d) 20×10, and (e) 40×20 boxes. (Inset) Table with results of $\sigma_{V_{\mathrm{th}}}$ due to RDD for the 45-nm template and comparison with atomistic simulations.

In practice, we multiply doping in box i by factor $(1+\alpha)$ and compute ΔV_{th_i} with TCAD simulations. Therefore, we have

$$\Delta N_i = \alpha N_i$$
$$\Delta V_{\mathrm{th}_i} = \alpha K_i N_i \tag{19}$$

so that (18) becomes

$$\Delta V_{\mathrm{th}} = \sum_i \left(\frac{\Delta V_{\mathrm{th}_i}}{\alpha}\right)\alpha = \sum_i \left(\frac{\Delta V_{\mathrm{th}_i}}{\alpha}\right)\frac{\Delta N_i}{N_i}. \tag{20}$$

We now need another reasonable assumption, i.e., doping variations in different boxes are independent Poisson processes. Therefore, from (20), we can write

$$\sigma^2_{V_{\mathrm{th}}\mathrm{RDD}} = \sum_i \left(\frac{\Delta V_{\mathrm{th}_i}}{\alpha}\right)^2 \frac{\sigma^2_{N_i}}{N_i^2} = \sum_i \sigma^2_{V_{\mathrm{th}}\mathrm{RDD}}{}^{[i]}. \tag{21}$$

Since N_i is a Poisson process, i.e., $N_i = \sigma_{N_i}$, we finally have

$$\sigma^2_{V_{\mathrm{th}}\mathrm{RDD}} = \sum_i \left(\frac{\Delta V_{\mathrm{th}_i}}{\alpha}\right)^2 \frac{1}{N_i} = \sum_i \sigma^2_{V_{\mathrm{th}}\mathrm{RDD}}{}^{[i]}. \tag{22}$$

The threshold-voltage dispersion due to RDD only requires a single TCAD simulation for each box and an integral of the doping profile in each box. Box partitioning is shown in Fig. 6(a) and covers a region smaller than the whole active area because one can easily check that, far from the channel, the impact of doping fluctuations on V_{th} rapidly goes to zero.

To evaluate the granularity of partition required to obtain reasonably accurate results, we have used different partitions for the 45-nm MOSFET, as shown in Fig. 6, i.e., 10×1 (a), 10×2 (b), 10×5 (c), 20×10 (d), and 40×20 (e). The table in the inset of Fig. 6 shows the standard deviation of the threshold voltage obtained for $V_{DS} = 50$ mV and 1.1 V. If the device is symmetric with respect to a source–drain swap, for low V_{DS}, we can reduce to half the number of simulations required since the propagator is also symmetric.

TABLE II
STANDARD DEVIATION OF THE THRESHOLD VOLTAGE DUE TO RDD FOR THE 45-, 32-, AND 22-nm-TEMPLATE MOSFETs

	45 nm	*Our approach*	*Stat. Sim. [12]*
50 mV	σ_{Vth} RDD (mV)	*47*	*50*
1.1 V	σ_{Vth} RDD (mV)	*50*	*52*
	22nm	*Our approach*	*Stat. Sim. [8]*
50 mV	σ_{Vth} RDD (mV)	*6.6*	*6.4*
1 V	σ_{Vth} RDD (mV)	*7.9*	*8.1*
	32 nm	*Our approach*	*Stat. Sim. [8]*
50 mV	σ_{Vth} RDD (mV)	*7.4*	*5.3*
1 V	σ_{Vth} RDD (mV)	*11*	*6.1*

Results show that only few simulations (in the case of Fig. 6(b), 20 for high V_{DS} or 10 for low V_{DS}) are sufficient to obtain reasonably accurate results. Very accurate results can be obtained in the case of Fig. 6(d) with a factor of ten more simulations. In Table II, results for the three template devices are compared with results from statistical simulations [12] for two different values of V_{DS}, i.e., 50 mV, which corresponds to quasi-equilibrium, and 1.1 V, which corresponds to far-from-equilibrium transport. In all cases, except the 32-nm device that posed convergence problems upon the application of the method, the agreement is rather good.

The partial contributions to the variance of the threshold voltage indicated with $\sigma^{2[i]}_{V_{\mathrm{th}}\mathrm{RDD}}$ are plotted as a function of positions in the color maps in Fig. 7 for the three template devices. In Fig. 7(a), the effect of the acceptor doping of the 45-nm MOSFET is shown, whereas in Fig. 7(b) and (c), the effect of the donor doping of the contacts of the 32- and 22-nm templates are shown, respectively. In all cases, it is pretty clear that a limited part of the active area has a practical impact on the threshold-voltage dispersion.

The total variance of the threshold voltage is computed by summing the variances due to all independent physical effects, i.e.,

$$\sigma^2_{V_{\mathrm{th}}\mathrm{TOT}} = \sigma^2_{V_{\mathrm{th}}\mathrm{RDD}} + \sigma^2_{V_{\mathrm{th}}\mathrm{LER}} + \sigma^2_{V_{\mathrm{th}}\mathrm{SR}}. \tag{23}$$

As mentioned previously, the cross terms are negligible even when they are considered. An *ex post* evaluation of results obtained with 3-D atomistic statistical simulations of separate and combined variability sources (for example, [8]) confirms such assumption.

III. CONCLUSION

We have proposed a methodology for the quantitative evaluation of the effect of LER, SR, and RDD, which is based on the careful analysis of the main independent physical parameters

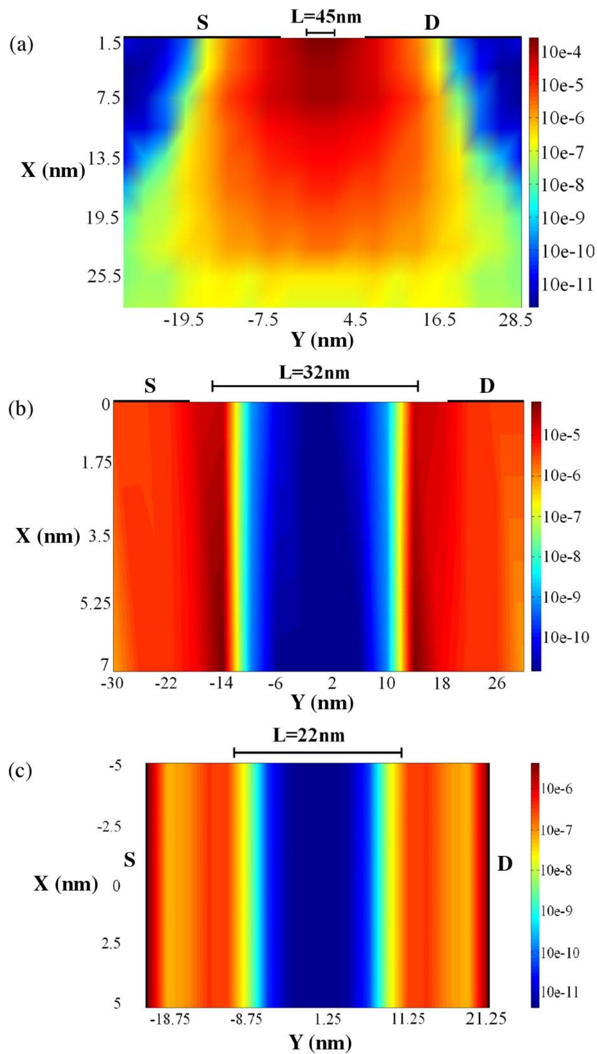


Fig. 7. Color maps of the partial contributions to the variance of the threshold voltage indicated with $\sigma^{2[i]}_{V_{\rm th}\rm RDD}$ as a function of position. Effect of (a) the acceptor doping of the 45-nm MOSFET and the donor doping of the (b) 32- and (c) 22-nm MOSFETs.

affecting threshold-voltage variability. The approach requires the calculation of partial derivatives of $V_{\rm th}$ with respect to device structure parameters that can be obtained with a limited number of 2-D TCAD simulations or—for simple doping profiles—with analytical models. We have shown that, in all cases, we are able to obtain results in very good agreement with 3-D atomistic statistical simulations [8], [12].

Let us stress the fact that one of the main tenets of our approach is that 3-D properties have no specific effect on the threshold voltage of MOSFETs for logic. Device width, as we have seen, only has an effect in determining the variance of the average doping, gate edge, or interface position. Such approximation is based on the assumption that the MOSFET behavior is mainly governed by electrostatics. The best validation of our approximation is the very good agreement between results from statistical simulations (based on 3-D modeling) and our sensitivity approach (based on 2-D modeling) for all device structures considered. We have qualified this statement to the threshold voltage of MOSFETs for logic because, when

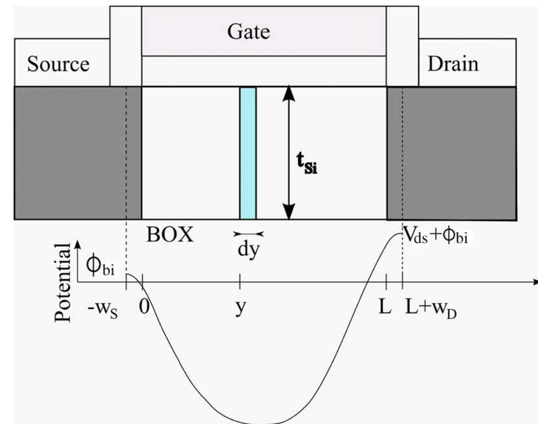


Fig. 8. Illustration of the method derived from [16] to obtain an analytical expression of the surface potential profile.

quantities are associated to deep subthreshold bias, for example, in the case of the threshold voltage of nonvolatile memory devices or the off-current of MOSFETs, peculiar 3-D effects such as percolation might play a significant role. In addition, our approach in the present form cannot provide information on the far tails of the distribution, which might be particularly important for evaluating device/circuit yield, and would require extension to higher order terms.

We believe that our approach has multiple advantages over statistical modeling, obviously not only in terms of computational requirements (by several orders of magnitude) but also in terms of providing a good framework for understanding the physical relevant effects affecting device variability and in the possibility of providing a quick way to evaluate $V_{\rm th}$ variability of candidate devices.

The main advantages of statistical simulation, on the other hand, are that it does not require preliminary device analysis and assumptions and that it would work even when the linear approximation does not hold, for example, in the presence of very large and critical variability. We firmly believe that the method presented here is a powerful tool to quickly evaluate the variability of device parameters in the context of technology developments, using simulations tools already available and routinely used by CMOS technology developers. It also provides a better understanding of the effect of single physical parameters on the overall device behavior and can therefore be a useful guide for device design.

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Appendix
Analytical Model for the Dependence of Threshold Voltage on Gate Length

The analytical model for the threshold voltage of the UTB SOI and double-gate MOSFETs is obtained from a simple derivation of surface potential profile $\phi_S(y)$ at the interface between the silicon body and the gate dielectric. We devise a

simple extension of the approach of Liu *et al.* [17] along the lines proposed in [18]. Let us consider, for example, Fig. 8, in which a UTB SOI MOSFET is considered. We assume that the channel can be divided into three regions, i.e., the central undoped region under the gate and the two external highly doped source and drain regions where the influence of the gate voltage is negligible. In the external regions ($y < 0$ and $y > L$), we assume complete depletion, and therefore, a parabolic potential profile is given by

$$\frac{d^2\phi_S}{dy^2} = -\frac{qN_D}{\varepsilon_{\text{Si}}} \tag{24}$$

where q is the electron charge, N_D is the average doping in the source and drain regions, and ε_{Si} is silicon dielectric permittivity. In the central region ($0 < y < L$), we use Gauss' theorem to write that the electric-field flux through the surface of a slice of thickness dy (shown in Fig. 8) is zero [11], [15]. This allows us to write

$$\frac{t_{\text{Si}}}{\eta}\frac{dE_S(y)}{dy} + \frac{\varepsilon_{\text{ox}}}{\varepsilon_{\text{Si}}}\frac{V_{GS} - V_{\text{FB}} - \phi_S(y)}{t_{\text{ox}}} = 0 \tag{25}$$

where $E_S(y)$ is the lateral surface electric field, $\phi_S(y)$ is the channel potential at the SiO_2 interface, ε_{ox} is the oxide electric permittivity, V_{FB} is the flatband voltage, and V_{GS} is the gate-to-source voltage. η is a fitting parameter that takes into account the fact that the electric field is not constant along x and that it is not zero in the buried oxide in the case of single-gate MOSFETs [18]. Its value usually varies between 1.0 and 1.3 [20].

The first term in (25) is the flux entering the Gaussian box along the y-direction; the second term is the electric flux entering the top surface of the Gaussian box. Since we adopt the guess that the electric field is constant along the x-direction, we can write $E_S(y) = -\{[d\phi_S(y)]/dy\}$.

Therefore, (25) becomes

$$\frac{d^2\phi_S(y)}{dy^2} - \frac{\eta}{\varepsilon_{\text{Si}}t_{\text{Si}}}\frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}}\phi_S(y) = \frac{\eta}{\varepsilon_{\text{Si}}t_{\text{Si}}}\frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}}(V_{\text{FB}} - V_{GS}). \tag{26}$$

Solving (26), we have

$$\phi_S(y) = \phi_P + C\frac{\sinh(y/\Lambda)}{\sinh(L/\Lambda)} + D\frac{\sinh[(L-y)/\Lambda]}{\sinh(L/\Lambda)} \tag{27}$$

where ϕ_P is the particular solution of the equation and is equal to $\phi_P = V_{GS} - V_{\text{FB}}$ and λ is the characteristic length defined as $\lambda = \sqrt{\varepsilon_{\text{Si}}t_{\text{Si}}t_{\text{ox}}/\eta\varepsilon_{\text{ox}}}$. Unknown terms w_S, w_D, C, and D are obtained by enforcing the continuity of ϕ_S and its derivative and by the boundary conditions, i.e.,

$$\begin{cases} \phi_S(-w_S) = \phi_{bi} \\ \frac{d\phi_S}{dy}(-w_S) = 0 \end{cases} \qquad \begin{cases} \phi_S(L + w_D) = V_{DS} + \phi_{bi} \\ \frac{d\phi_S}{dy}(L + w_D) = 0. \end{cases} \tag{28}$$

Once $\phi_S(y)$ is known, we can extract its minimum value in channel $\phi_{\text{SMIN}}(V_{GS}, V_{DS})$ and obtain the threshold voltage as the gate voltage required to have $\phi_{\text{SMIN}} = \phi^*$, corresponding to the drain current used in the definition of V_{th}.

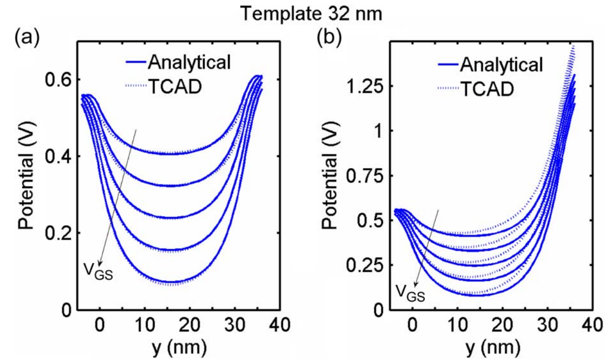

Fig. 9. Surface potential profile of the 32-nm-template MOSFET as a function of y for different V_{GS} values (0–0.5 V in steps of 0.1 V) for $V_{DS} =$ (a) 50 mV or (b) 1 V. Comparison between analytical model and TCAD simulations. (Arrow) Increase in V_{GS}.

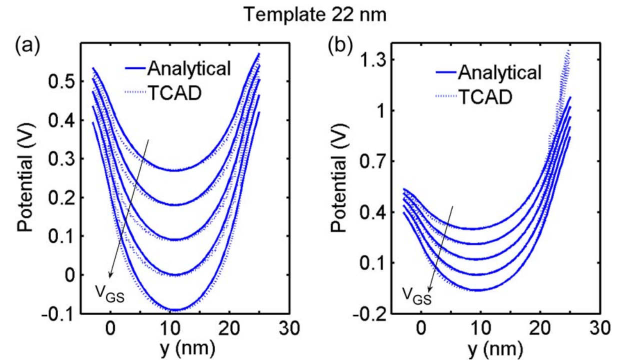

Fig. 10. Surface potential profile of the 22-nm-template MOSFET as a function of y for different V_{GS} values (0–0.5 V in steps of 0.1 V) for $V_{DS} =$ (a) 50 mV or (b) 1 V. Comparison between analytical model and TCAD simulations. (Arrow) Increase in V_{GS}.

The minimum potential along the longitudinal direction can be obtained from

$$\left.\frac{d\phi_S(y)}{dy}\right|_{y_{\min}} = 0. \tag{29}$$

At a low drain–source voltage value, we can be assume that $y_{\min} = (L/2)$.

First, we want to validate our analytical model for the surface potential and the threshold voltage by comparison with TCAD results [15] on the template devices with the full doping profiles. In Fig. 9, the surface potential profiles for the 32-nm-template MOSFET are compared for $V_{DS} = 50$ mV and 1 V and for different values of V_{GS}. We use a single fitting parameter ($\eta = 1.2$) with the same value for the 32- and 22-nm templates at the price of a suboptimal fitting. Nevertheless, agreement is very good. Very good agreement is also obtained for the 22-nm-template MOSFET (see Fig. 10).

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