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# *Detailed calculation of the vertical electric field in thin oxide MOSFETs*

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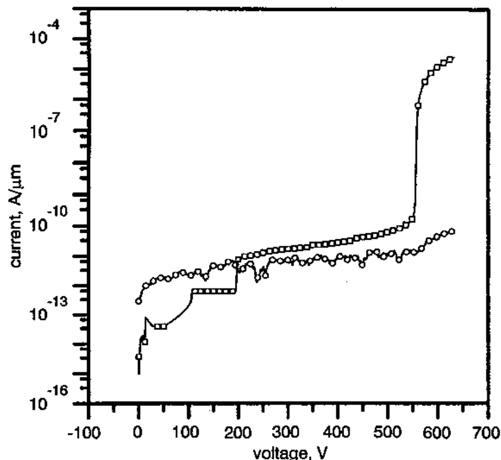


**Fig. 3** *Contours of flowlines and potentials across switch at drain bias of 450 V*

○ drain current
□ source current

lations show a blocking capability of only ~210V. Using a simplified model [6], the voltage without a buffer is estimated to be ~190V. Therefore, a significant improvement is achieved by introducing the *n*-buffer layer under the source.

Table 1 shows the relationship between the breakdown voltages and drift lengths. The breakdown voltage increases with drift length. Above 60μm drift length, the blocking capability does not improve with further increases in the drift length.

**Table 1:** Relationship between breakdown voltage and drift length

| | 20μm | 30μm | 40μm | 50μm | 60μm |
|---|---|---|---|---|---|
| BV | 238V | 336V | 420V | 491V | 550V |

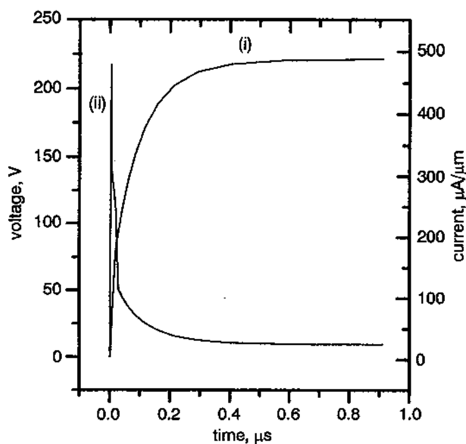


**Fig. 4** *Effect of current component on blocking capability*

Gate bias, $P^+$ isolation are 0 V
(i) source voltage
(ii) source current

By fixing the drain to a high potential and connecting the source to a resistor of 9MΩ and a small capacitor of $6.6 \times 10^{-2}$pF, the transient turn on performance is obtained and is shown in Fig. 4. In all the simulations, the models of Auger, SRH and impact ionisation were enabled. A 2μs carrier lifetime was specified for the silicon material. To produce a better convergence, a ramping time of 20ns was incorporated in the gate pulse. The device has a turn on time of 0.22μs for the source voltage, while the waveform of the source current has a quicker response. A sharp current spike is obvious in the Figure, which comprises a displacement component and the discharge of the attached capacitor. Considering the 0.59μs time constant of the load resistance and capacitance, the fast response of the source voltage and current proves the quick transient speed of the device.

In conclusion, a lateral power MOSFET suitable for application as a high side switch has been successfully designed using a modified 600V CMOS process. The device has a blocking capability in excess of 550V, and a turn on time of 0.22μs. The superior blocking capability comes from the incorporation of an *n*-buffer layer prior to the formation of the *p*-well.

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## Detailed calculation of vertical electric field in thin oxide MOSFETs

S. Gennai and G. Iannaccone

The authors have performed a detailed calculation of the vertical electric field in a MOSFET, taking into account polysilicon gate depletion, quantum-confinement effects in the channel, and the anisotropy of the effective mass. It is shown that thin oxides do not exhibit higher actual breakdown fields than thick oxides.

The process of scaling down the dimensions of MOSFETs requires the use of ever thinner gate oxides: it is expected that oxide thicknesses in the range 2–3nm will be required for channel lengths of 100nm, to be delivered to the market in about the year 2003 [1, 2]. The very high electric fields present in such thin oxides even at small gate voltages may pose severe reliability problems that need to be thoroughly investigated.

Recently, 1.5nm-thick gate oxides have been fabricated with very promising characteristics in terms of uniformity and reliability [3]. A breakdown voltage of ~3.4V was measured, suggesting that very thin gate oxides could have breakdown fields in excess of 20 MV/cm, considerably higher than those of thicker oxides.

However, quantum confinement in the channel and depletion of the polysilicon gate reduce the voltage drop in the oxide, and hence the electric field. It is therefore important to establish what is the actual vertical electric field in an MOS structure, as a function of device parameters and operating conditions.

In this Letter we present results from a detailed simulation of charge accumulation in the inversion layer. The charge density and the conduction band profile in the MOS structure are computed by solving self-consistently the Schrödinger and Poisson equations with a purposely developed code. The anisotropy of the silicon effective mass is taken into account, as well as the different

orientations of the six conduction band minima. In the case considered of the (100) substrate the Schrödinger equation has to be solved with effective mass $m_t = 0.19m_0$ for four minima (transverse mass $(m_t \times m_l)^{0.5}$), and with effective mass $m_l = 0.96m_0$ for the other two minima (transverse mass $m_t$), where $m_0$ is the electron mass.

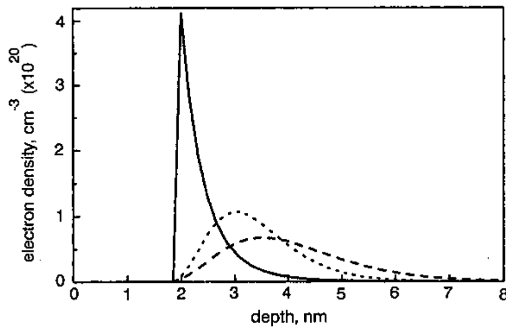


**Fig. 1** *Computed electron density in MOS structure with gate voltage of 3V, $t_{ox}$ = 2nm, $N_A = 5 \times 10^{17} cm^{-3}$*

Poly $N_D = 10^{20}$cm$^{-3}$

In Fig. 1 the charge density profile is shown for an *n*MOS device with oxide thickness $t_{ox}$ = 2nm, acceptor concentration $N_A = 5 \times 10^{17}$cm$^{-3}$, $n^+$-polysilicon gate with $N_D = 10^{20}$cm$^{-3}$, and gate voltage $V_g$ = 3V. Results are plotted from a semiclassical simulation (solid line), a quantum simulation with isotropic mass equal to $(m_t^2 m_l)^{1/3}$ (dashed line), and a quantum simulation including the anisotropic effective mass (dotted line). As can be seen, the peak of the electron density in the quantum case is ~1nm deeper than that at the $Si$-$SiO_2$ interface, meaning that the electric field is not completely screened at the $Si$-$SiO_2$ interface and causes a potential drop in the channel region, so that the field in the oxide is reduced with respect to that obtained with a semiclassical model.

In Fig. 2 the electric field in the oxide $E$ is plotted against the gate voltage for the same device. The solid line represents the very naive model of parallel plate capacitor $V_g/t_{ox}$, while the squares are the results from a semi-classical solution of the nonlinear Poisson equation, neglecting gate depletion (i.e. considering a metal gate). The slight deviations from the solid line are due to the finite density of states in silicon and to the Fermi-Dirac statistics, both reducing the screening properties of the inversion layer. The black circles are results from a semiclassical calculation where depletion of the $n^+$-polysilicon gate with $N_D = 10^{20}$cm$^{-3}$ is considered. Finally, the triangles and the white circles are the results from a quantum simulation with isotropic and anisotropic effective mass, respectively. Also in this case, it can be seen that the anisotropic mass has to be considered, otherwise the quantum correction is overestimated.

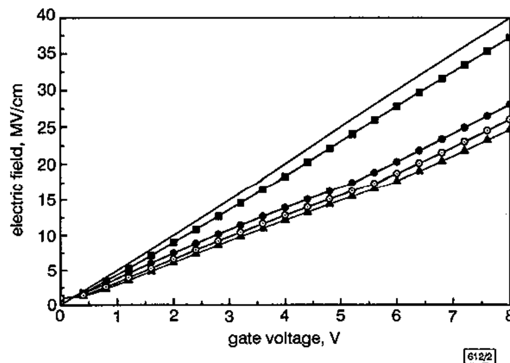


**Fig. 2** *Electric field against gate voltage for device described in text*

——— $V_g/tox$
■ semiclassical model with metal gate
● semiclassical model with poly gate
▲ quantum model with poly gate and isotropic effective masss
○ quantum model with anisotropic effective mass

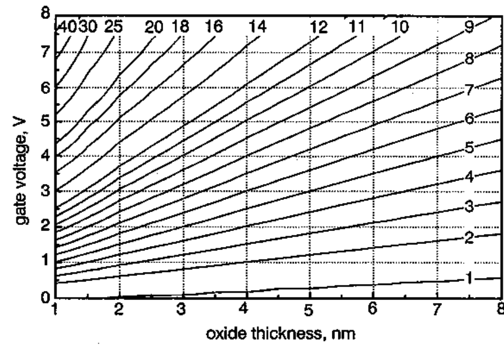


**Fig. 3** *Contour plot of electric field against oxide thickness and gate voltage computed with complete quantum model, with $N_D = 10^{20} cm^{-3}$*

Further details are in text

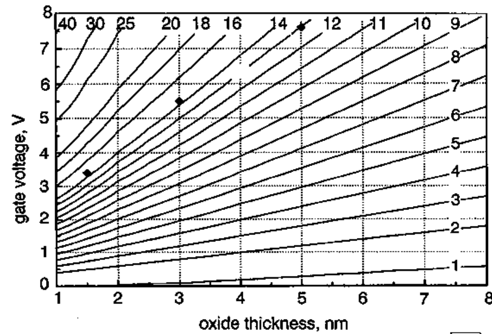


**Fig. 4** *Contour plot of electric field against oxide thickness and gate voltage computed with complete quantum model, with $N_D = 2 \times 10^{20} cm^{-3}$*

◆ breakdown voltages extracted from [3]

In Figs. 3 and 4 we show the contour plots of the vertical electric field in the oxide as a function of gate voltage and oxide thickness for a donor concentration in the poly gate $N_D = 10^{20}$cm$^{-3}$ and $ND = 2 \times 10^{20}$cm$^{-3}$, respectively. The quantum simulation takes into account mass anisotropy in silicon and considers an acceptor concentration in the channel of $N_A = 5 \times 10^{17}$cm$^{-3}$; however, the dependence of the electric field in the oxide on $N_A$ can be neglected for fields higher than a few MV/cm. On the other hand, as can be seen, the higher polysilicon doping leads to an increase of a few percent in the electric field in the oxide. Both Figures can be used as reference charts in which the electric field can be readily obtained once $t_{ox}$ and $V_g$ are known.

In Fig. 4, we have also indicated with black diamonds the breakdown voltage of the gate oxides discussed in [3]. As can be seen, while the naive approximation $E = V_g/t_{ox}$ would suggest strongly increased breakdown fields with decreased $t_{ox}$, a detailed calculation shows that the actual breakdown field is practically not dependent on the oxide thickness, and is between 13 and 14 MV/cm.

In conclusion, we have computed the electric field in thin oxide MOSFETs on the basis of a detailed quantum simulation, have shown that a naive estimation of electric fields can lead to an error in excess of 100%, and that even for extremely thin oxides the breakdown field is close to 14MV/cm.

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## Logic circuit elements using single-electron tunnelling transistors

N.J. Stone and H. Ahmed

Logic elements have been demonstrated using single-electron tunnelling transistors. The transistors are biased at different positions in the conductance oscillation cycle so that they are analogous to either *n*-type or *p*-type transistors. The circuit operation is stable at a temperature of 1.6 K despite the low gain of the transistors.

Single-electron memory and logic circuits have been demonstrated using the Coulomb gap of a single-electron device to define the status of the system [1 – 4]. Tucker *et al.* [5] proposed the use of conductance oscillations in a single-electron tunnelling transistor (SETT) as the basis of a logic circuit. They noted that by biasing a transistor on either a peak or a trough of its conductance oscillation either decreasing or increasing conductance would be obtained for an increase in gate voltage. It is possible on this basis to make transistors equivalent to either *n*-type or *p*-type metal oxide semiconductor field effect transistors (MOSFETs). The circuits for SETT logic using this technique can therefore be analogous to CMOS logic circuits. Furthermore, single-electron logic offers the advantage of low power consumption and lower battery voltage than conventional CMOS and could lead to higher levels of integration in logic circuits. We report the experimental verification of this proposal by Tucker *et al.*

The SETT transistors used in the experiment reported here are in the form of Si nanowires [6] fabricated in silicon-on-insulator (SOI) using high-resolution e-beam lithography and reactive ion etching (RIE). At 77 K and below, the silicon nanowires break up into a series of conducting islands separated by tunnel barriers; this makes up a multiple tunnel junction (MTJ) [7] which shows clear Coulomb blockade and is relatively immune to offset charge effects.

The fabrication process is as follows: optical lithography is used to form bond pad regions and interconnects, then Cr/Ag is evaporated and lifted off to form a metal etch mask. High-resolution electron beam lithography is used to write the circuit, and Al is evaporated and lifted off to complete the metal mask. RIE then transfers the pattern to the SOI wafer consisting of a 40nm conducting Si layer doped with phosphorous ($10^{19}$cm$^{-3}$), separated by 350nm of $SiO_2$ from the silicon substrate and capped with a 20nm $SiO_2$ protective layer. After etching the metal mask, the circuit is oxidised at 1000°C in dry oxygen for 15min. The first optical stage is then repeated and a SILOX etch is used to remove the protective oxide in the bondpad and interconnect regions. This is followed by evaporation and lift off of Cr/Au to complete the device.

A circuit schematic is shown in Fig. 1. Fig. 2*a* shows an SEM (scanning electron micrograph) of the circuit, Fig. 2*b* shows an SEM at higher magnification of a single transistor (rotated by 90°) which is 300nm in length by approximately 30nm in width. The circuit consists of four MTJ SETTs each with two side gates; one of the side gates is used to bias the device and the other forms the logic signal input. A drain bias of 0.01V was applied to $V_{DD}$ and the voltage at $V_O$ was monitored. Each SETT was characterised by sweeping its side gate voltage while a constant bias voltage

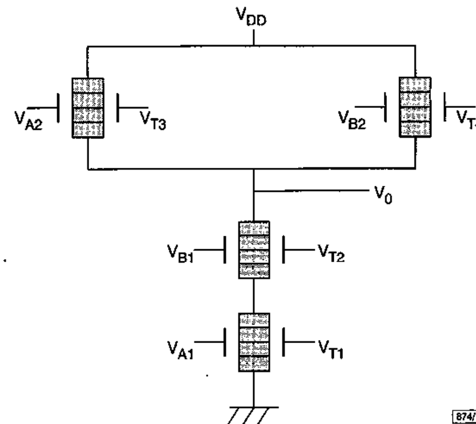


**Fig. 1** *Schematic diagram of NAND circuit showing input voltages to MTJ gates and trimming gate voltages*

was applied to all the other gates. The SETTs showed similar but not identical electrical characteristics with clearly observable Coulomb oscillations in the output voltage $V_O$ for a range of $V_T$ from 2V to −2V for each device. The characteristic for SETT1 is shown in Fig. 3*a*. As the side gate voltage $V_T$ of a device is swept through a range of values, its Coulomb gap oscillates i.e. the voltage dropped across it changes, thereby pulling $V_O$ towards either $V_{DD}$ or ground. The SETT characteristic consists of multiple periods, as shown in Fig. 3*a*. It is totally reproducible; subsequent sweeps map out precisely the same trace. It is believed that the oxidation process described earlier passivates the device such that the effects of RTS (random telegraph switching) are almost absent.

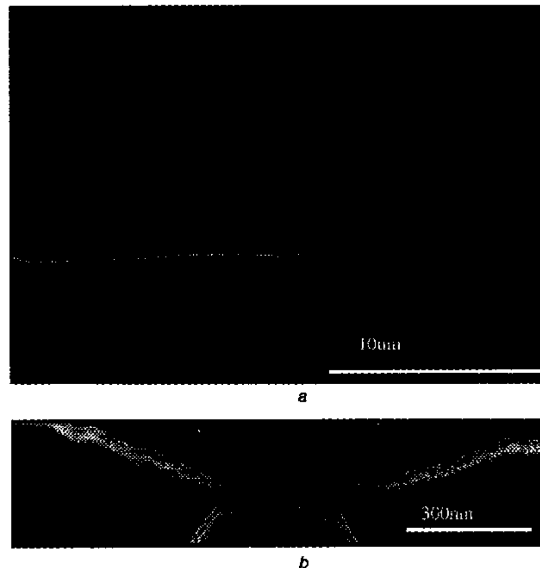


**Fig. 2** *SEMs of circuit in SOI material and of individual SETT*
*a* SOI material
*b* Individual SETT

To demonstrate a NAND function, an oscillation with a negative slope is required. In this case, an input going from 0 to 1 gives an output going from 1 to 0. For each device, as shown in Fig. 3*b*, *c*, *d* and *e*, an oscillation of suitable magnitude was chosen. The peak and trough values of each curve were taken as the high and low input values for the corresponding device. These inputs were applied as a logic pulse train to the circuit in the form of 0,0: 0,1: 1,0: 1,1. The second side gates for the SETTs were adjusted by a small amount to compensate for the measured characteristic of a device being dependent on the bias voltage applied to the device. The resulting output waveform is shown in Fig. 4. Although the SETT gain is less than 1 (~0.1) the NAND function is clearly obtained. The device was operated at low speed with