Tuning of surface boundary conditions for the 3D simulation of gated heterostructures

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We propose a method for treating the boundary conditions at the exposed surface of semiconductor nanostructures, and compare the results from simulations based on such a method with experimental measurements on test devices defined electrostatically by metal gates on AlGaAs/GaAs heterostructures. In particular, we show that the pinch-off voltage of quantum point contacts realized with split gates can be reasonably reproduced, provided the lithographic gap is small enough.

Key words: surface states, heterostructures, split gates.

1. Introduction

In the simulation of semiconductor nanostructures the issue of boundary conditions at the exposed surface has often been neglected or treated with drastic approximations that provide only quantitative agreement with the experimental data. Notable exceptions are, for example, the work by Larkin and Davies [1], where the results from Dirichlet and Neumann boundary conditions are discussed, and that by Chen and Porod [2], who considered a distribution of surface states and computed their occupancy solving the Poisson equation in the air above the semiconductor.

We have developed a 3D multi-grid nonlinear Poisson solver for the determination of the confinement potential within a GaAs/AlGaAs nanostructure due to the action of metal gates at the surface, for an arbitrary layer structure, and we have fabricated full and split gates of several different sizes.

Depletion of the two-dimensional electron gas (2DEG) at the heterointerface is strongly dependent on the choice of boundary conditions at the exposed surface and the main focus of our work has been on devising a proper treatment for such a surface. With Dirichlet boundary conditions (i.e. assuming perfect Fermi level pinning) the voltage that needs to be applied to the gates to completely pinch off a quantum point contact is usually larger than what is experimentally measured, due to the screening action of the surface. On the other hand, Neumann boundary conditions with zero electric field at the interface [3] lead to results that are not in good agreement with the measurements, either.

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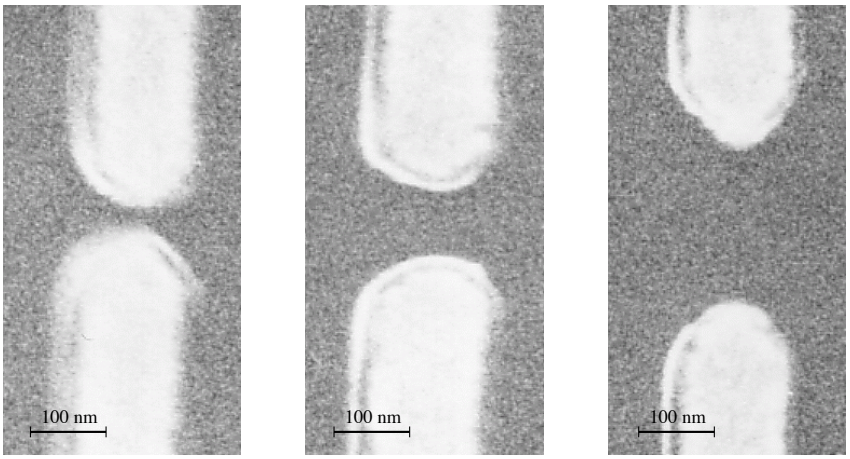

Fig. 1. SEM photographs of the split gate structures E1, F1, and G1.

2. Approach

Our approach consists of performing an initial calculation with all gates grounded and assuming Fermi level pinning at the exposed surface. The difference E_{pin} between the conduction band edge E_C and the energy at which the Fermi level is actually pinned is determined by fitting the experimental sheet charge density in the 2DEG at equilibrium. From the Poisson solver we determine the electric field at the semiconductor–air interface and therefore the surface charge density.

We then proceed considering that at very low temperatures ($\approx$4.2 K) the surface charge remains substantially unchanged when nonzero voltages are applied to the gates for normal device operation. In addition, since at the surface there is an abrupt change of the dielectric constant from GaAs ($\epsilon_{\text{r}} = 12.9$) to air, we can reasonably translate the assumption of constant surface charge into that of constant electric field at the GaAs surface. Therefore, the previously determined value of the electric field is used as a Neumann boundary condition for a new solution of the nonlinear Poisson equation with the proper gate voltages. In such a way, the domain of the 3D Poisson equation is limited to the semiconductor, and does not have to be extended to the air above the surface.

3. Experiment

Samples have been fabricated on an AlGaAs/GaAs heterostructure with the following layer sequence: undoped GaAs substrate, 20 nm thick undoped AlGaAs, silicon delta doping with a dose of 6×10^{12} cm^{-2}, 10 nm thick undoped AlGaAs, 5 nm GaAs cap layer. A two-dimensional electron gas is obtained at a depth of 35 nm, with a measured sheet electron density $n_s = 4.9 \times 10^{11}$ cm^{-2} at the temperature of 4.2 K.

Several gate layouts have been patterned by electron beam lithography and successive lift-off. In particular, single gates with a width of 80, 160, 220, and 540 nm, and split gates with a width of 120 nm and different lithographic gaps have been realized: 60, 120, 200 nm for the samples E1, F1, and G1, respectively, which are shown in Fig. 1.

It is important to point out that in order to improve gate adhesion on the surface, a slight etching step ($\approx$3–4 nm) precedes metal evaporation, so that the gates are actually deeper than the exposed surface. This has a significant effect on the pinch-off voltage of the full gates, and a much less relevant effect on the pinch-off

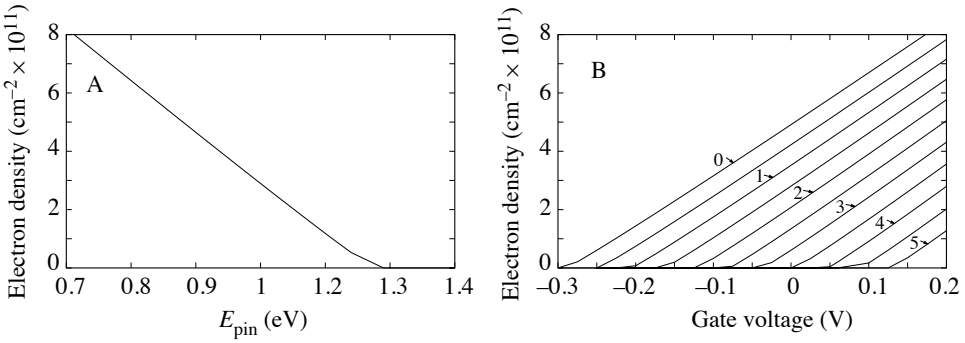

Fig. 2. A, Electron density in the 2DEG as a function of E_{pin}; B, electron density as a function of the gate voltage for different etching depths (nm) with $E_{\text{pin}} = 0.74$.

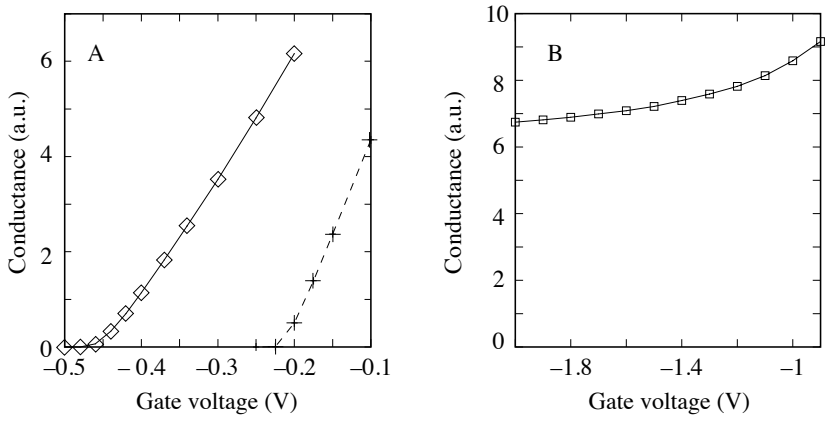

Fig. 3. Theoretical conductance of constrictions E1, F1 (left) and G1 (right) as a function of the gate voltage.

voltage of the split gates. In this paper, we focus on the split gate structures, and, among the full gates, we consider only the one with the largest width, whose pinch-off value should be essentially equal to that due to an infinite metal plane at the surface of the heterostructure.

4. Results and discussion

With a nonlinear 1D Poisson solver we have first computed the value of n_s at equilibrium as a function of E_{pin} (Fig. 2A), in order to obtain the value of E_{pin} corresponding to the measured n_s ($E_{\text{pin}} = 0.855$ eV). Such a value is well within the range of values for E_{pin} found in the literature [4]. The corresponding electric field at the surface is $\mathcal{E} = 0.772$ MV cm^{-1}. We have then computed the sheet electron density in the 2DEG as a function of the gate voltage for different values of the etching depth (Fig. 2B): an etching depth of 1 nm corresponds to a shift of about 70 mV for the pinch-off voltage. The experimental pinch-off values for the 540 nm wide single gate are 60 and 173 mV, which are well fitted by an etching depth of 4 and 6 nm, respectively.

We have then solved the 3D nonlinear Poisson equation for the split gates. The actual shape of the gates has been obtained from the SEM photographs shown in Fig. 1. We have assumed an etching depth of 4 nm under the gates and for each gate voltage we have computed the electron density, the conduction band edge profiles,

and the Drude conductance, assuming a local conductivity $\sigma(\mathbf{r}) = q\mu n(\mathbf{r})$, where q is the electron charge, μ the mobility, n the electron density. In Fig.3 the conductance is plotted as a function of the gate voltage for the three samples. The computed pinch-off voltages can be obtained directly from Fig.3: they are -0.22 and -0.46 V for E1 and F1, respectively, while there is no pinch-off up to -2 V for G1. The experimental values are -0.23, -0.39, -0.97 V for E1, F1, and G1, respectively. The agreement is reasonable for the split gates with the smaller gaps. In the case of sample G1, the proposed approach fails. We can identify two possible reasons for such a behavior: first, the approximation of constant charge and constant electric field may not be valid for larger exposed areas; furthermore the simulation should take into account the complete gate layout, since the capacitive coupling between the constriction and the gates, in the case of wide gaps, could have a substantial contribution from wide gate regions far from the tips.

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References

[1] I. A. Larkin and J. H. Davies, Phys. Rev. **B52**, R5535 (1995).
[2] Minhan Chen and W. Porod, J. Appl. Phys. **78**, 1050 (1995).
[3] M. Stopa, Phys. Rev. **B48**, 18340 (1993).
[4] S. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981) pp. 270–279.