Program, Erase and retention times of thin-oxide Flash EEPROMs

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The purpose of this work is the simulation of program, erase, and retention times of thin-oxide Flash EEPROMs, in which the floating gate is charged through Fowler-Nordheim (FN) or direct tunneling.

We have developed a code which allows to simulate the complete time-dependent process of charging and discharging the floating gate in one dimension, with a fully quantum-mechanical approach, including both tunneling through the barrier and quantum confinement in the channel. As the floating gate is progressively charged, the tunneling current undergoes a steep decrease due to the increased potential barrier. Therefore, a reliable estimate of write and retention times must rely upon the accurate simulation of the time-evolution of potential profiles and charge densities.

We focus on two different types of memories: *i)* "conventional" flash memories with thin oxides, in order to evaluate possible trade-offs between write and retention times; *ii)* flash memories with a very thin floating gate [1], in which quantum confinement in the floating gate is significant.

As a first example, we consider a Flash EEPROM with the following structure: substrate doping $N_A = 10^{18}$ cm^{-3}, tunnel oxide, n-type polysilicon floating gate ($N_D = 10^{19}$ cm^{-3}), triple O.N.O. layer (5 nm-thick oxide, 10 nm-thick nitride, 5 nm-thick oxide), and n$^+$ poly control gate ($N_D = 10^{20}$ cm^{-3}).

First we have simulated the charging process (program operation) with gate-to-channel voltage of 18 V. In Fig. 1 the threshold voltage increase ΔV_T obtained is plotted as a function of the required program time for tunnel oxides ranging from 6 to 10 nm. As can be seen, in the case of 6 nm-thick oxide, 5 μs are needed to increase the threshold voltage by 2 V.

In Fig. 2 results are shown for the erase operation. The initial ΔV_T is plotted as a function of the time required for reducing the charge in the floating gate (FG) to 10% of the initial value. The voltage difference between gate and source is -18 V. The erase time is slightly reduced with increasing charge storage, since the presence of charge in the FG induces a curvature in the potential profile which increases the tunneling probability.

In Fig 3 data retention is considered. No voltage is applied to the control gate, and data is considered lost when 10% of the initial charge leaks out. Again, the programmed ΔV_T is represented on the y-axis while retention time is on the x-axis. As can be seen, the ten-year limit is guaranteed even for the 6 nm-thick oxide, if defect-assisted tunneling is negligible.

Results for several structures with more aggressive oxide thickness or different gate stacks [2] will be presented, in order to show that the code developed can be very helpful for the design of flash memories with optimized trade-off between write speed and data retention.

References

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2. K. K. Likharev, *Layered tunnel barriers for nonvolatile memory devices*, Applied Physics Letters, 73, pp. 2137-2139, 1998.

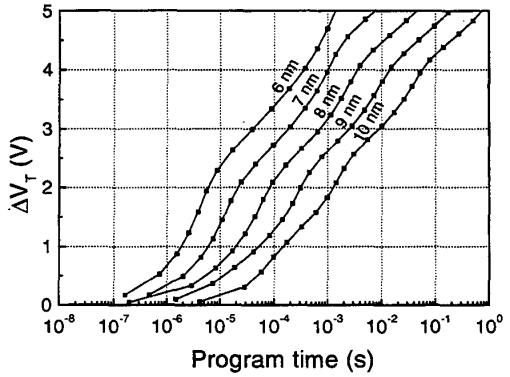

Fig. 1: Program times and associated threshold voltage increase ΔV_T for different oxide thicknesses of the device described in the text

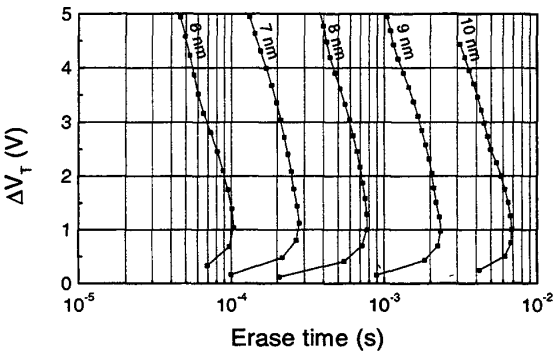

Fig. 2: Erase times and associated initial ΔV_T for different oxide thicknesses. Data is erase when charge in the floating gate is reduced to 10% of the initial value.

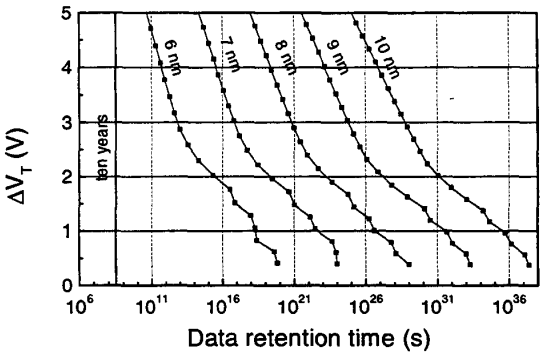

Fig. 3: Data retention times and associated initial ΔV_T for different oxide thicknesses. Data is considered lost when 10% of the initial charge leaks out.