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Three-dimensional simulation of nanocrystal Flash memories

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Three-dimensional simulation of nanocrystal Flash memories

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We have developed a code for the detailed simulation of nanocrystal Flash memories, which consist of metal–oxide–semiconductor field-effect transistors (MOSFETs) with an array of semiconductor nanocrystals embedded in the gate dielectric. Information is encoded in the MOSFET threshold voltage, which depends on the amount of charge stored in the nanocrystal layer. Nanocrystals are charged through direct tunneling of electrons from the channel. Such memories are promising in terms of shorter write–erase times, larger cyclability, and lower power consumption with respect to conventional nonvolatile memories. We show results obtained from the self-consistent solution of the Poisson–Schrödinger equation on a three-dimensional grid, focusing on the charging process and on the effect of charge stored in the nanocrystals on the threshold voltage. © *2001 American Institute of Physics*. [DOI: 10.1063/1.1361097]

A nanocrystal Flash memory is basically a metal–oxide–semiconductor field-effect transistor (MOSFET) in which the gate dielectric is replaced by a gate stack consisting of a thin tunneling oxide, a layer of semiconductor nanocrystals embedded in silicon oxide, and a thicker oxide. Such memory devices have been recently proposed[1,2] and extensively studied in industrial and academic laboratories.[3–7]

The memory is programmed by applying to the gate a positive voltage of a few volts that lowers the thin oxide conduction band and enhances tunneling of electrons from the substrate to the nanocrystals. Electrons get trapped in the nanocrystals, since further tunneling to the gate is inhibited by the thicker top oxide. However, due to already observed Coulomb blockade effects at room temperature,[3] only a well defined number of electrons (depending on the applied gate voltage) can occupy each nanocrystal, so that charging of the nanocrystals is a self-limited process.

When an electron is added to each nanocrystal the MOSFET threshold voltage increases in steps, so that both single and multibit storage is possible. The information stored in the memory is then simply read by measuring the saturation current corresponding to a gate voltage significantly smaller than that used for programming. The memory is erased by applying a negative gate voltage that ejects electrons from the nanocrystals into the channel.

While a conventional Flash electrically erasable programmable read-only memory (EEPROM) has a tunneling oxide typically thicker than 7 nm and requires programming voltages larger than 10 V, a nanocrystal memory has a very thin tunneling oxide (2–4 nm), and exhibits short programming times with direct tunneling and much smaller write–erase voltages (≈3 V). It is therefore extremely promising in terms of endurance to write–erase cycles and power consumption,[4] while it usually has a poor retention time compared to the 10-year requirement typical of commercial Flash EEPROMs.

Nanocrystal memories have interesting applications as quasi-nonvolatile memories, where cyclability and power consumption are more important than 10-year data retention, or as dynamic random access memories with very long refresh time. In addition, Coulomb blockade effects should enable easy implementation of multibit storage schemes.

Several materials have been investigated for the nanocrystals and the dielectric layer, and are listed in Table I. At present, silicon rich oxide deposited by low pressure chemical vapor deposition (LPCVD) on SiO_2 (Ref. 4) and implanted Si or Ge in SiO_2 (Ref. 5) are the most promising from the point of view of compatibility with current complementary MOS (CMOS) technology, retention time, and threshold voltage shift per electron.

Since the device structure is inherently three-dimensional (3D) and electrons in the dot are strongly confined (the nanocrystal diameter is usually in the range of 3–10 nm), an equivalent electrical circuit would not be adequate for obtaining accurate results. For this reason, we have developed a code for the self-consistent solution of Poisson and Schrödinger equations on a 3D grid, based on density functional theory with local density approximation.[8]

While nanocrystals are of course randomly distributed in the layer, we have considered a simplified situation in which disorder is removed, that is, nanocrystals occupy a perfect two-dimensional lattice in the dielectric layer. We consider the device structure shown in Fig. 1: a MOSFET with a gate stack consisting of a 3 nm thick bottom tunneling oxide, a

TABLE I. A few prototypes of nanocrystal memories presented in the literature, with measured ΔV_T per electron and retention time.

Dot/insulator material	ΔV_T per electron (V)	Retention time	Reference
Si in SiO_2	0.36	Not shown	1
InAs/AlGaAs	0.25	1 h at 100 K	6
Si or Ge in SiO_2	0.3	≈1 h	5
SiGe/SiO_2	0.4	1 day	7
SRO/SiO_2	≈1	Not shown	4
Si/Si_3N_4–SiO_2	0.48	≈3 h	3

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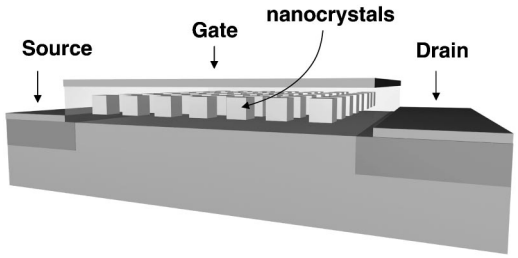

FIG. 1. Device structure considered in the simulation. A regular two-dimensional array of cubic Si nanocrystals is embedded in the gate oxide of a MOSFET.

rectangular two-dimensional array of silicon nanocrystals embedded in SiO_2, and a 6 nm thick top oxide layer. Without loss of generality, we assume cubic dots with 5 nm edges and average donor doping of $10^{19}\,\mathrm{cm}^{-3}$ (here we will not consider the effect of discrete dopants). The substrate has an acceptor doping of $10^{18}\,\mathrm{cm}^{-3}$ and the gate is metallic.

The regular arrangement of the dots allows us to simulate only the region that represents the elementary cell of the lattice structure, and then to apply periodic boundary conditions on the potential. The domain in which we actually solve the Schrödinger–Poisson equation is therefore the one shown in Fig. 2. The surface density of nanocrystals σ_{nc} is the inverse of the area of the domain considered on the horizontal plane: we consider an area of $10\times10\,\mathrm{nm}^2$, corresponding to $\sigma_{\mathrm{nc}}=10^{12}\,\mathrm{cm}^{-2}$.

Let us point out that we are making two implicit assumptions: that all nanocrystals are in the same charge conditions and that edge effects acting on nanocrystals located close to the contacts are not relevant. While the latter can be readily accepted if we assume a sufficiently large number of nanocrystals under the gate (e.g., at least 5×5), the former is only justified because here we focus on stationary properties of the memories: it would not be acceptable if we were interested in the time-dependent process of nanocrystal charging. The potential profile in our domain is determined by the Poisson equation

$$\nabla[\epsilon\nabla\phi(\mathbf{r})]=-\rho(\mathbf{r})=-q[p(\mathbf{r})-n(\mathbf{r})+N_D^+(\mathbf{r})-N_A^-(\mathbf{r})], \tag{1}$$

where ϕ is the scalar potential, ϵ the dielectric constant, p and n the hole and electron densities, respectively, and N_D^+ and N_A^- the concentrations of ionized donors and acceptors,

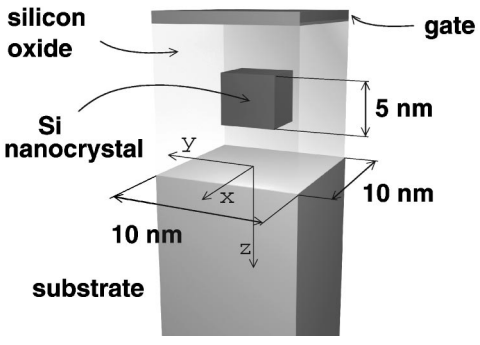

FIG. 2. View of the simulation domain: The nanocrystal is a silicon cube with 5 nm edges, and the thickness of the top and bottom oxide is 6 and 3 nm, respectively.

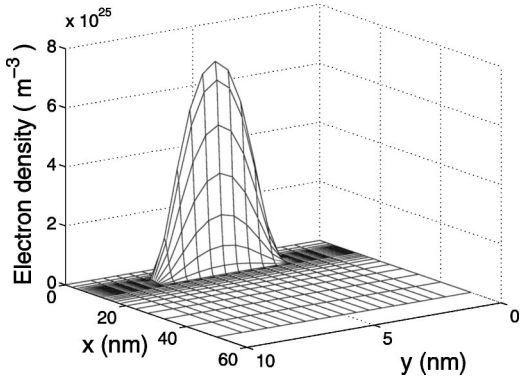

FIG. 3. Electron density on the $x-z$ plane for an applied gate voltage of 1.2 V and one electron in the dot.

respectively, that depend on ϕ as indicated in Ref. 9. While electrons and hole concentrations in the substrate are computed with the semiclassical approximation,[9] electrons in the nanocrystal are strongly confined, and therefore their density is computed by solving the Schrödinger equation with density functional theory

$$-\frac{\hbar^2}{2}\nabla\left(\frac{1}{m}\nabla\Psi\right)+E_c(\mathbf{r})\Psi+V_{xc}(\mathbf{r})\Psi=E\Psi, \tag{2}$$

where E_c is the conduction band in the nanocrystal [$E_c=E_c(\phi=0)-q\phi$], $\hbar$ is the reduced Planck constant, and V_{xc} is the exchange-correlation potential in the local density approximation[8]

$$V_{xc}(\mathbf{r})=-\frac{q^2}{4\pi^2\epsilon_0\epsilon_r}[3\pi^3 n(\mathbf{r})]^{1/3}. \tag{3}$$

Nanocrystals are randomly oriented, therefore we prefer not to use the effective mass tensor for silicon, but only a single effective mass for the density of states $m=0.32m_0$, where m_0 is the electron mass at rest. Each eigenfunction Ψ_i of energy E_i has a degeneracy of 12, due to spin degeneracy and to the presence of six equivalent minima in the conduction band. If the dot is occupied by N electrons, and l and m are two integer such as $N=12\times l+m$ (with $m<12$) the electron density reads

$$n(\mathbf{r})=12\sum_{i=1}^{l}|\Psi_i(\mathbf{r})|^2+m|\Psi_{l+1}(\mathbf{r})|^2 \tag{4}$$

under the assumption that the electron density in the dot is not appreciably different from that in the ground state.

The Poisson–Schrödinger equation is self-consistently solved for several values of N and of the gate voltage V_G. The maximum number of electrons that can occupy a dot $N_{\max}$ is a function of V_G: if $\mu(N,V_G)$ is the chemical potential of the dot with N electrons and applied gate voltage V_G, and E_F is the Fermi energy in the substrate, $N_{\max}$ must satisfy the conditions

$$\mu(N_{\max},V_G)<E_F;\quad \mu(N_{\max}+1,V_G)>E_F. \tag{5}$$

The chemical potential is computed with Slater's transition rule[10] as $\mu(N)=E_{N-1/2}$, where $E_{N-1/2}$ is the highest occupied eigenvalue of the system with $N-1/2$ electrons, computed with density functional theory.

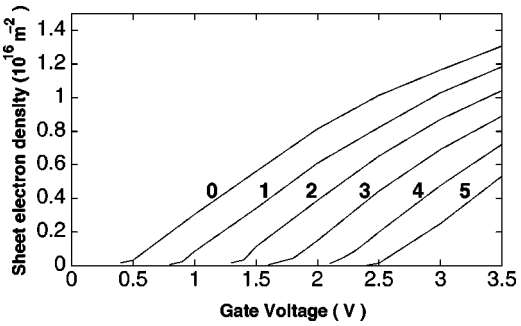

FIG. 4. Sheet electron density in the channel as a function of the gate voltage for a number of electrons in a nanocrystal ranging from 0 to 5.

By keeping fixed the number of electrons and computing the electron density in the channel as a function of V_G, one can directly obtain the value of the threshold voltage for any number of electrons in the nanocrystal.

The electron density in the nanocrystal on the $x-z$ plane for an applied voltage of 1.2 V and an occupancy of one electron is plotted in Fig. 3. As can be seen, the electron density has the shape of the first eigenfunction, with only one peak at the center.

In Fig. 4 we plot the sheet electron density in the channel as a function of the gate voltage V_G for a number of additional electrons in the nanocrystal ranging from 0 to 5 (thin solid lines). From those curves the threshold voltage can be obtained as the intercept on the horizontal axis of the line approximating each curve in the quasilinear region. As can be seen, the threshold voltage with no electrons in the nanocrystal is $V_{T0}=0.5$ V and the V_T shift is approximately 0.4 V per each stored electron.

In Fig. 5 we plot the chemical potential μ of the dot as a function of V_G for a number of electrons N ranging from 1 to 7. The Fermi level in the channel is zero, therefore the intercept of all the curves with the horizontal axis gives the gate voltage at which an additional electron can enter the nanocrystal.

We can see from Figs. 4 and 5 that several options for write and read voltages are available. For example, if we assume that the logical ''0'' corresponds to zero electrons in the nanocrystal, we could write a logical ''1'' by applying a voltage pulse of 2 V, thereby introducing three electrons in the nanocrystal (as can be seen from Fig. 5) and obtaining a threshold voltage $V_{T1}=1.7$ V (as obtained from Fig. 4). Then we could choose a voltage $V_{GR}=0.6$ V to read the status of the memory, since it satisfies $V_{TO}<V_{GR}<V_{T1}$ and, in addition, is small enough not to introduce any additional electron in the dot (see Fig. 5).

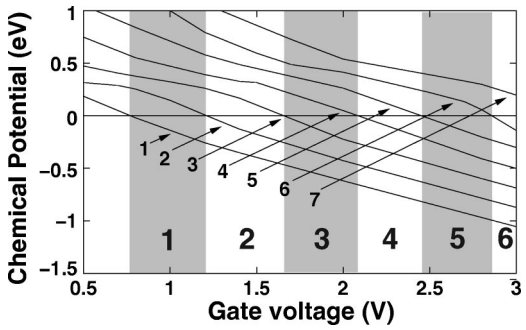

FIG. 5. Chemical potential of the nanocrystal as a function of the gate voltage for a number of stored electrons ranging from 1 to 7.

We have developed a numerical model for the three-dimensional quantum-mechanical simulation of nanocrystal Flash memories, and we have shown results for a typical device structure. The model developed is a useful tool for exploring the effects of process parameters and of geometry on the electrical properties of such memory devices.

For simplicity, we have considered a perfectly regular array of nanocrystals. A disordered distribution of nanocrystals would have an effect very similar to that of the random distribution of dopants in conventional MOSFETs, causing statistical dispersion of V_T and of V_T shifts. From this analogy, we can say that the relative dispersion of V_T shifts increases when the channel area is reduced, but decreases with increasing nanocrystal density σ_{nc}, and can be therefore kept under control by increasing σ_{nc}.[11] However, a detailed investigation on this subject is required.

A very important aspect for the industrial application of nonvolatile memories based on nanocrystal layers is the evaluation of write, erase, and retention times. Promising results have been obtained in experiments[3–7] and the issue has been partially addressed from the theoretical point of view in Ref. 12. An in-depth analysis of this aspect is also needed to evaluate the maximum operating temperature as a function of the required retention time. This issue is beyond the scope of this letter and will be addressed in the near future.

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