Semiclassical simulation of quantum cellular automaton circuits

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Semiclassical simulation of quantum cellular automaton circuits

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SUMMARY

We present a simulator for quantum cellular automaton (QCA) circuits, based on a semiclassical model and aimed at the determination of the error probability in the presence of thermal excitations. Different methods are discussed; either a complete exploration of the configuration space, or a partial exploration by means of simulated annealing. Results for the probability of obtaining the ground state and the correct logical output are derived and compared for a chain of cells, for a majority voting gate and for a simple combinatorial network. This approach can be extended to generic implementations of the QCA paradigm. Copyright © 2001 John Wiley & Sons, Ltd.

KEY WORDS: quantum cellular automata; simulated annealing; thermal behaviour

1. INTRODUCTION

The analysis and simulation of circuits based on nanoelectronic devices poses new challenges and is gaining relevance as nanoscale devices are being put together from the beginning to obtain more complex functionalities. Compared to the simulation of single devices, circuit simulation involves a much larger computational effort, and requires a trade-off between model refinement and the amount of acceptable computational complexity. It is, therefore, necessary to develop efficient approximations, which reproduce the behaviour of single devices in a reasonably accurate way, but allow treatment of many of them at the same time.

We have developed a few simulators for quantum cellular automaton (QCA) circuits implementing the computational paradigm proposed by Lent *et al.* [1] for the realization of combinatorial logic circuits based on bistable cells containing two electrons that can be localized according to two possible configurations, corresponding to the two logic states. Our main purpose at this stage has been represented by the rigorous evaluation of error probabilities due to thermal excitations and by the determination of the maximum allowed operating temperature. For this reason, whenever possible, we have used models that, although simplified, have a capability of representing not only the two lowest energy states of a QCA cell (the ones

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corresponding to the logical values 1 and 0), but also the excited states that can be populated when temperature is raised.

In this paper, we present an approach to the simulation of QCA circuits based on a semiclassical model, in which electrons are considered as classical particles that can arrange in the four dots in such a way as to minimize the total electrostatic energy, with the only added nonclassical property of being able to tunnel between adjacent dots. The model is developed with a numerical simulation that includes all six possible configurations of two electrons in each cell and with an analytical extension for a reduced number of configurations. For large circuits an exhaustive search for the ground state becomes prohibitive, and specialized search techniques have been developed, based on a simulated annealing procedure.

In the next section, we present a general description of the semiclassical model, with a discussion of the energy spectrum of a wire of QCA cells. Section 3 deals with the application of the semiclassical model to the evaluation of the error probability in a wire, while Section 4 deals with the evaluation of this quantity for more complex circuits. The simulated annealing procedure for the determination of the ground state of large QCA logic circuits is presented in Section 4. Finally, Section 5 summarizes with conclusions.

2. SEMICLASSICAL MODEL

As already stated in the introduction, our semiclassical model for QCA cells is based on treating the electrons as classical particles, which can however tunnel between adjacent quantum dots. A cell has the structure represented in Figure 1(a), with four dots separated by tunnelling barriers. Owing to electrostatic repulsion, electrons will tend to align along one of the two diagonals, since these are the configurations that correspond to the maximum spatial separation. In the absence of external electric fields, these two configurations will have exactly the same energy, while in the presence, for example, of a nearby cell with a well-defined polarization, one of them will be energetically favoured. There are also four more possible configurations (we do not consider the situations in which more than one electron are confined in a single dot, due to the very large associated electrostatic energy), for a total of six configurations, as indicated in Figure 1(b). While we associate the logic values 1 and 0 with the two lowest energy states (1 with the state with electrons in dots 1 and 3, 0 with the one with electrons in dot 2 and 4), no logic value is to be assigned to the other four states corresponding to electrons aligned along directions parallel to the sides of the cell, therefore, we define them X states. If several cells are lined up to form a wire (we will define it 'binary wire' in the following) and a given polarization is enforced for the first cell, polarization will propagate along the wire in a domino fashion [2], until all cells have reached the same configuration.

In our simulations a positive background charge $e/2$ (e being the electron charge) is assumed in each dot, in order to keep the cell overall neutral, thus, avoiding undesired effects associated with the monopole electric field component that would be produced by a non-neutral cell, which would tend to push both electrons contained in the nearby cells towards the further side. The total electrostatic energy of an array of QCA cells can, within our semiclassical model, be expressed as the energy of a system of point charges:

$$E = \sum_{i \neq j} \frac{q_i q_j}{4\pi\varepsilon_0 \varepsilon_r r_{ij}}, \tag{1}$$

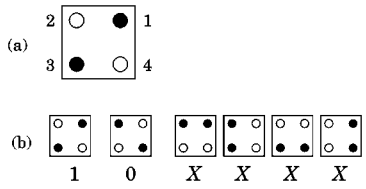

Figure 1. (a) Layout of a four-dot QCA cell with two electrons. (b) Possible configurations for two electrons in a four-dot cell.

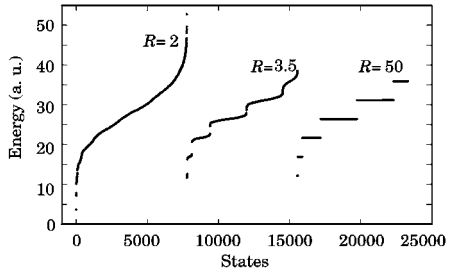

Figure 2. Energy spectra for different values of the ratio R of the intercell separation d to the distance between dots in the same cell a. The plots for $R = 3.5$ and $R = 50$ have been translated to the right for the sake of graphic clarity.

where q_i is the charge associated with the ith dot, r_{ij} is the distance between dot i and dot j, ε_0 is the vacuum permittivity, and ε_r is the relative permittivity of the medium (we consider the case of GaAs/AlGaAs, assuming a uniform relative permittivity of 11.9).

By repeating the evaluation of the total energy for all possible configurations (6^N if the circuit contains N cells) we can determine the ground state and the distribution of energy values. The energy spectrum of a binary wire is strongly influenced by the ratio R of the separation between cell centers d to the distance a between the nearest dots in the same cell. If this ratio is large, a 'kink' in the wire (i.e. a single discontinuity in the polarization of the cells) corresponds to an increase in the electrostatic energy that is almost independent of the position of the kink itself. Therefore, all configurations with one kink have the same energy, corresponding to the first excited state of the chain. As two kinks appear, the total electrostatic energy is further raised, yielding a second 'level' in the energy spectrum. The same situation is repeated with increasing number of kinks, leading to a discrete staircase spectrum, as seen in Figure 2 for $R = 50$. If R is reduced, repulsion effects between the electrons cause the appearance of X states which correspond to intermediate energy values, thereby, leading to a more complex spectrum (central plot in Figure 2), that, for $R = 2$, becomes continuous.

As the number of cells increases, the time required to perform an exhaustive exploration of the energy values for all configurations grows exponentially, becoming prohibitive if more than about 12–13 cells are considered. If larger circuits are to be investigated, one can either resort to a simplified model (with fewer states) or apply techniques based on an incomplete, targeted exploration of the configuration space, such as in the case of the simulated annealing method, which will be discussed in Section 5.

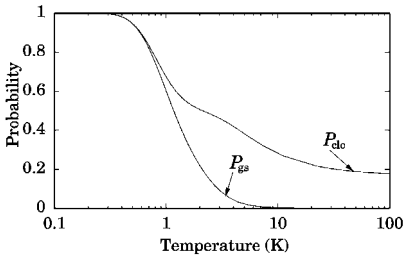

Figure 3. Plot of the probability of a six-cell binary wire being in the ground state (P_{gs}) and of presenting the correct logical output (P_{clo}). The intercell separation is 100 nm and the distance between dots in the same cell is 40 nm.

3. THERMAL BEHAVIOUR OF A BINARY WIRE

As already mentioned in the introduction, our main focus has been on the investigation of finite temperature effects on the operation of QCA logic circuits. While at zero temperature a QCA array will always relax, given a sufficient time, down to the ground state, providing the expected output values, different configurations may appear with a nonvanishing probability in the presence of thermal excitations associated with a finite temperature. The higher the temperature, the more likely the occurrence of configurations other than the ground state will be. It is important to remind of the fact that in any conceivable implementation of QCA logic data readout will be performed by means of a detector, which, due to its characteristic time constant, will provide an average value of the output cell polarization state. Therefore, the actual error probability on the data available at the output of the readout circuit will be much smaller, owing to the averaging effect, than that on the actual instantaneous polarization state of the output cell.

In order to evaluate the mentioned error probabilities we need to know the probability for the system being in the ground state and in any given excited state. Such probability for the jth state can be expressed by means of the Boltzmann factor divided by the partition function. In particular, the probability of the system being in the ground state is given by

$$P_{gs} = \frac{e^{-E_{gs}/(kT)}}{Z} = \frac{1}{1 + \sum_{i \neq gs} e^{-\Delta E_i(/kT)}}, \tag{2}$$

where Z is the partition function, given by $Z = \sum_i \exp -E_i/(kT)$, $\Delta E_i = E_i - E_{gs}$, k is the Boltzmann constant and T is the temperature. The summation is performed over all excited states. Besides P_{gs}, we may also be interested in knowing the probability of having the correct logical output P_{clo}, which is larger than P_{gs}, since there are other configurations, in addition to that corresponding to the ground state, which share the correct output value. In order to obtain P_{clo} we need to sum over the probabilities corresponding to such configurations:

$$P_{clo} = \frac{\sum_j e^{-E_j/(kT)}}{Z}. \tag{3}$$

We have evaluated these two relevant quantities for structures of increasing complexity, as a function of temperature, assuming a separation a between the dots within a cell of 40 nm and an intercell distance d of 100 nm. The first object of investigation has been represented

by the already mentioned binary wire: results for P_{gs} and P_{clo} are reported in Figure 3, for the case of a six-cell wire. Both probabilities decrease with increasing temperature, but, while P_{gs} drops down to an extremely small value, P_{clo} saturates at about 0.167. The reason for this behaviour is rather simple: for large values of the temperature, when kT becomes much larger than the separation in energy between the different configurations, all such configurations become approximately equally probable. Thus, the possible configurations for the wire are 6^5 (the polarization of the input cell is enforced from the outside, therefore, only 5 cells participate in creating the configuration spectrum) and only one corresponds to the ground state, $\lim_{T\to\infty} P_{gs} = 1/6^5$. The possible polarization states for the output cell are instead 6, thus leading to a P_{clo} of $1/6$ for large values of T. Given a maximum acceptable error probability, the limiting operating temperature can be obtained from the plot of Figure 3. As the length of the wire is increased, the maximum operating temperature decreases logarithmically, as discussed in Reference [3] on the basis of entropy arguments and in Reference [4] by means of an analytical version of the procedure we have just discussed.

4. THERMAL BEHAVIOUR OF LOGIC CIRCUITS

The analysis performed on a binary wire can be extended to an arbitrary logic gate, as long as treatment of the full configuration space is possible. One of the simplest gates that can be obtained with the QCA approach is the majority voting gate, whose layout is represented in the inset of Figure 4: the logic state of the output cell corresponds to that of the majority of the inputs. Such a gate can also operate as a programmable OR or AND [2], by using one of the inputs to control the logic function: if the control input is set at 1, the output corresponds to an OR operation between the two inputs. If, instead, the control input is set at 0, the output corresponds to the AND of the inputs. The behaviour of P_{gs} and P_{clo} as a function of temperature is rather similar to that for the binary wire shown in Figure 3 and exhibits some variations in dependence of the input configuration. Such a dependence is clearly recognizable in the plot of Figure 4, which represents the maximum operating temperature as a function of $R = d/a$, with $a = 40\,\text{nm}$, for the control input set at 1 (OR gate) and all possible combinations of the A and B input values. The minimum acceptable P_{clo} has been set at 0.9 (which corresponds to a much higher actual correct readout probability, as already discussed). The operating temperature decreases with increasing R, due to the reduced interaction; an anomalous behavior is however observed for values of R less than 2. In this latter case the dependence of the maximum operating temperature on R is reversed, as a consequence of the appearance of X states in the first excited configuration, which completely alters the energy splitting between the ground state and the first excited state, whose ratio to the thermal energy kT is the figure of merit determining the error probability [4]. Notice, in particular, that the curve for $A = 0$, $B = 0$ drops to zero for R below approximately 1.6, because in this range neither the ground state nor the first excited state correspond to the expected output value 0 and, therefore, there is no temperature at which the output has the correct logical value.

We have extended our investigation of the error probability also to more complex structures, such as the one shown in Figure 5, which contains two AND gates providing the inputs to an OR gate, thus implementing the logic function $AB + CD$. This circuit is made up of 18 cells, of which 7 (represented with thick boundaries) have logic values enforced from the outside; therefore the configuration space contains 6^{11} elements, and its complete exploration requires

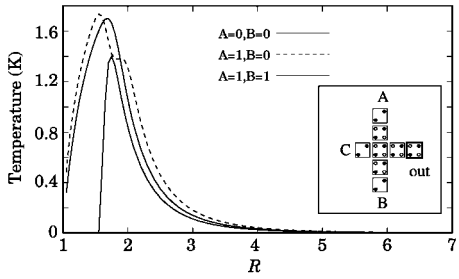

Figure 4. Maximum operating temperature versus the ratio of the intercell distance to the separation between dots in a cell, for a majority voting gate, assuming $C = 1$ and considering all possible combinations for the other two inputs. The layout for a QCA majority voting gate is shown in the inset.

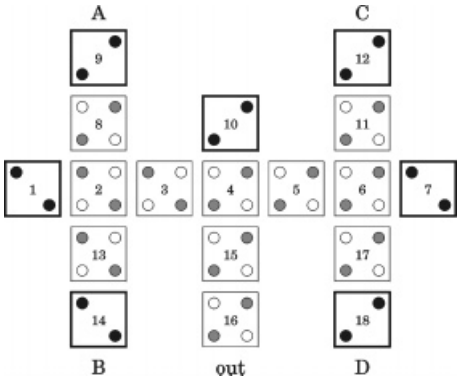

Figure 5. Layout of a QCA circuit implementing the logic function $AB + CD$. Cells with an externally enforced polarization are represented with thick boundaries.

approximately 36 h on a DEC Alpha 500au workstation. Results are reported in Figure 6 for two choices of the input variables: $A = B = C = D = 1$ for Figure 6(a) and $A = 0$, $B = C = D = 1$ for Figure 6(b). A difference between the two cases is clearly visible, in particular for low temperatures, and originates from the variation, between the two input configurations, of the energy splitting between the first excited state and the ground state. In the case corresponding to Figure 6(a) such a splitting is 0.159 meV, while in the other case is 0.086 meV: this leads to a lower operating temperature being required to obtain the same error probability.

5. SIMULATED ANNEALING

The exploration of the configuration space for the circuit with 11 active cells described in the previous section was already taking 36 h on a high-performance workstation: addition of just a few more cells, each of which involves a sixfold increase of such a time, would make the calculation computationally unfeasible.

For this reason, we have implemented a technique, based on simulated annealing, which allows to obtain the ground state and the low-lying excited states without exploring the whole

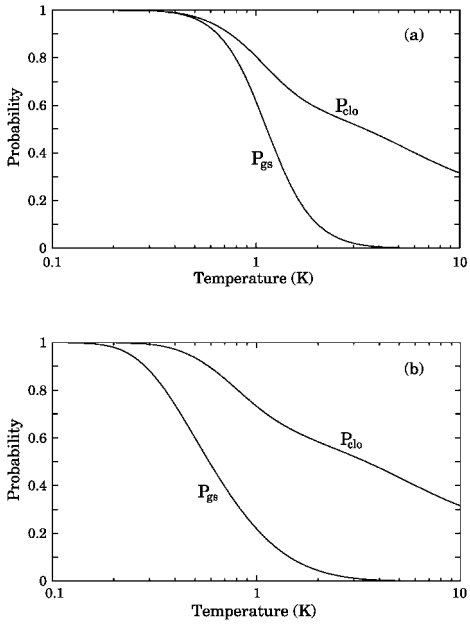

Figure 6. Plot of P_{gs} and P_{clo} as a function of temperature for a combinatorial network implementing the operation $AB + CD$, for $A = B = C = D = 1$ (a) and for $A = 0,\ B = C = D = 1$ (b).

configuration space. Simulated annealing has been already proposed in the context of QCA circuits [6] as a means of actually operating the circuits themselves. In this paper, we will instead show how it can be used for an efficient simulation of QCA systems.

Simulated annealing basically consists in initializing the system in a random position in the configuration space, and then letting it evolve until it reaches the configuration of minimum energy. In particular, we start by assuming the system in a randomly selected configuration of energy E_0 at an initial temperature T_0. Let us call E_a the instantaneous (in the sense of corresponding to the current configuration) energy of the system: at the beginning $E_a = E_0$. Then, we pick a new configuration at random, obtained from the current one by simply moving one electron from one dot to another within the same cell. We then let the system evolve into the new configuration with a probability p_{new} depending on E_a and on the energy E_{new} of the new configuration:

$$p_{new} = \begin{cases} 1 & \text{if } E_{new} \leqslant E_a \\ \exp[-(E_{new} - E_a)/kT] & \text{if } E_{new} > E_a \end{cases} \tag{4}$$

The first condition allows the system to evolve along trajectories of descending energy, while the second prevents the system from getting stuck in metastable states, corresponding to local minima. This cycle is repeated many times, progressively decreasing the temperature from T_0 to a value at which a stable configuration is reached. If the system is cooled down at a sufficiently slow rate, the stable state is the ground state. In Figure 7 the instantaneous configuration energy and the temperature are plotted as a function of the iteration number for a binary wire with six cells. In the case shown, the number of iterations required to reach the

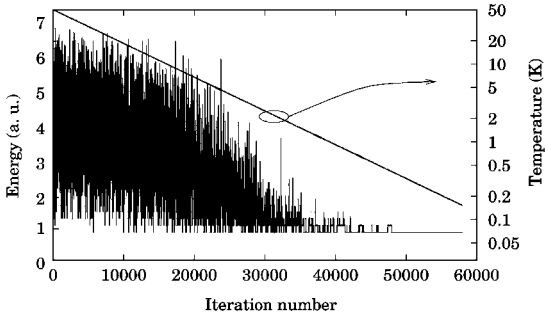

Figure 7. Monte Carlo run of simulated annealing for a wire consisting of six cells. The instantaneous energy (in Kelvin) and the temperature are plotted as a function of the iteration number.

ground state is larger than the total number of configurations ($6^5 = 7776$); however, it increases much more slowly with increasing number of cells, therefore becomes quite convenient for a number of cells larger than 10.

In order to validate the code, it is useful to verify whether the thermodynamic properties of the circuit are well reproduced with the simulated annealing method. The probability density $N(E,T)$ that the system in a state of energy E is the product of the density of states $D(E)$ and of the Boltzmann factor $P(E,T)$

$$N(E,T) = D(E)P(E,T) = D(E)\frac{e^{-E/kT}}{Z} \tag{5}$$

We first obtain $N(E,T)$ from Equation (5), by computing the energies of all possible configurations and hence, the partition function and the density of states. Then, we compute $N(E,T)$ directly with the simulated annealing method, keeping the temperature constant, and computing the statistics of the instantaneous energy by means of an average over iteration cycles: $N(E)\Delta E$ is the ratio of the number of iterations at which the system is at an energy between E and $E + \Delta E$ to the total number of iterations. In Figure 8, $N(E)$ obtained from the simulated annealing (solid line) and from the complete method (dashed line) are plotted as a function of energy for four different temperatures: 50, 20, 10 and 2 K. In all cases the agreement is extremely good.

In order to show the ability of the simulated annealing method to reproduce the thermodynamic behaviour of QCA circuits, we have plotted in Figure 9 P_{gs} and P_{clo} as a function of temperature for the two-level combinatorial network described in the previous section and shown in Figure 6, for a given input: the agreement with the result obtained with the complete method is extremely good.

There is actually a possibility for the simulated annealing method to get stuck in a configuration corresponding to a local energy minimum and, therefore to converge to a state different from the ground state. In Figure 10 we show the relative frequency with which, repeating the annealing sequence starting from different random initial configurations, the actual ground state and a few low-lying excited states are reached as a result, for a two-to-one multiplexer circuit (shown in the inset of Figure 10). The ground state is obtained 54% of the times. Such percentage can be adjusted and optimized by modifying the rate of decrease of temperature with increasing iteration number. However, in general, the safer approach consists in perform-

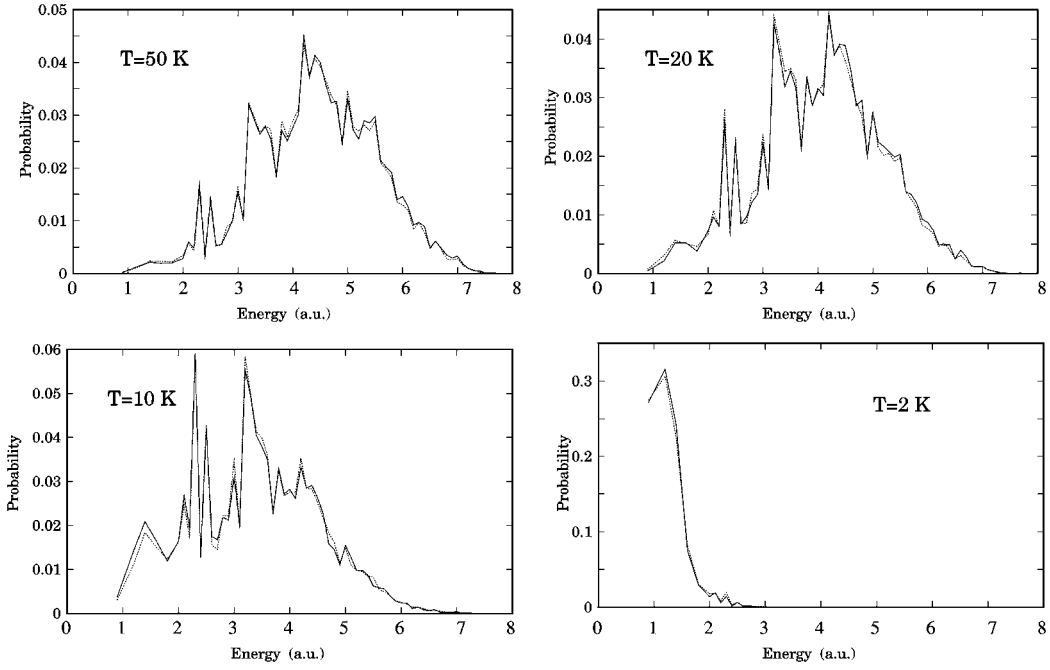

Figure 8. Probability density $N(E,T)$ that the system is in a state of energy E for four different temperatures: $50, 20, 10$ and $2\,\mathrm{K}$: results obtained with simulated annealing (solid lines) and with the complete exploration of the configuration space (dashed lines).

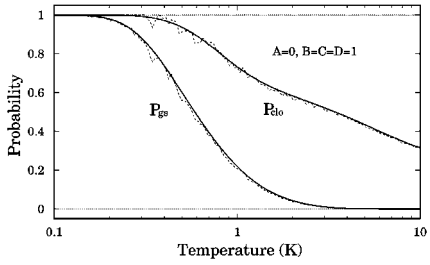

Figure 9. Probability of the ground state P_{gs} and of correct logical output P_{clo} for the two-level combinatorial network described in Figure 6 for $A=0$, $B=C=D=1$: results from the complete exploration of the configuration space (solid lines) and from simulated annealing (dashed lines).

ing a sort of 'thermal cycling' procedure, i.e. letting the system converge to a stable state, iteratively increasing the temperature T to drive the system to an excited state, and finally reducing T until a stable state is reached. Among all the obtained stable states, the probability that the state of minimum energy corresponds to the real ground state is $1-(1-P_1)^m$ where m is the number of thermal cycles and P_1 is the probability of obtaining the ground state without thermal cycling. For example, in the case shown in Figure 10 ($P_1=0.54$), the probability of finding the ground state with eight thermal cycles is 0.998.

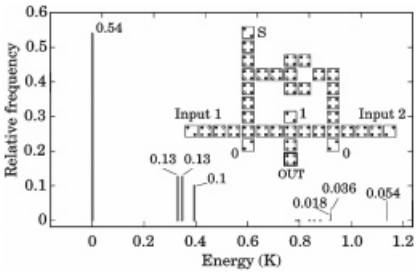

Figure 10. Relative frequency of the ground state and of a few excited states in the outcome of the annealing simulation.

6. CONCLUSION

Starting from a simplified, semiclassical model for a QCA cell, we have developed a set of tools that allow the simulation of QCA circuits containing relatively complex logic gates. Our tools are aimed, in particular, at the analysis of the error probability due to the presence of thermal excitations associated with finite temperatures, and computational techniques are tuned according to the size of the circuit to be simulated. Up to 11–12 cells it is possible to explore the complete configuration space, built starting from six different states for each cell, while for larger structures approximations must be used, in which we either reduce the number of cell states considered, thus significantly shrinking the overall size of the configuration space, or implement methods that involve exploration of only a portion of such space. We have found that the error probability is mainly influenced by the ratio of the energy splitting between the first excited state and the ground state to the thermal energy kT. If a reasonably low error probability is to be achieved, the mentioned energy splitting must be at least an order of magnitude larger than kT, which involves severe technological problems, because a large energy splitting requires a strong electrostatic interaction, that, in turn, implies the availability of very small cells [5].

The temperature dependence of the error probability has been computed for a binary wire, for a majority voting gate and for a small combinatorial network: results show a similar behaviour, with a maximum operating temperature for a given error probability that roughly drops logarithmically with the number of involved cells. Significant differences, however, can be observed depending on the logic values at the inputs, which influence the splitting between ground state and first excited state and, as a consequence, determine variations of the allowed operating temperature for a given error probability. In order to evaluate the maximum operating temperature for a QCA logic circuit, it is, therefore, necessary to compute the error probabilities as a function of temperature for all possible input configurations and choose the least favourable result.

For circuits that are too large to allow a complete exploration of the configuration space we have developed a simulated annealing technique which, starting from a random configuration, converges to the ground state in a number of iterations much smaller than the number of possible configurations. A thermal cycling procedure has been devised to prevent the annealing sequence from getting stuck in local energy minima. Our simulated annealing code has been validated by comparing, with good agreement, the thermodynamic properties obtained for a

few simple circuits with those computed with methods performing the full exploration of the configuration space.

The range of application of the simulation tools that we have developed is not limited to the semiconductor implementation of QCA circuits: our codes can be easily adapted to any QCA architecture, including those based on possibly bistable molecules or on the recently proposed magnetic dot arrays [7], which have a potential for higher temperature operation, due to the stronger cell-to-cell interaction.

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