Performance assessment of adiabatic quantum cellular automata

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We investigate the feasibility of an adiabatic logic scheme for cellular automaton systems recently proposed by Tóth and Lent [J. Appl. Phys. **85**, 2977 (1999)], based on structured arrays of six-dot cells and on the use of a four-phase trapezoidal clock. With respect to the original quantum cellular automaton (QCA) concept, focused on ground state computation, a clocked scheme would have the advantage of being immune to the presence of metastable states and would allow pipelined operation, at the expense of additional complexity, due to the clock distribution circuitry. Based on realistic cell geometries and material systems, we have evaluated the obtainable switching times of QCA cells, and have determined the region in the parameter space that allows operation at a reasonable clock speed. © *2001 American Institute of Physics*. [DOI: 10.1063/1.1365078]

I. INTRODUCTION

The quantum cellular automaton (QCA) architecture initially proposed in Ref. 1 has very innovative features with respect to conventional electronic circuits. First, it is characterized by extreme modularity: a QCA circuit is a structured two-dimensional array of identical cells, each consisting of four (or five) dots separated by tunneling barriers, with two excess electrons, as sketched in Fig. 1(a). Binary information is encoded in dot occupancy: electrons tend to align along one diagonal (corresponding to logical ''1'') or along the other (logical ''0'').

Cells are coupled with one another only through electrostatic interaction. Let us consider two adjacent cells such as those shown in Fig. 1(b). If the logical state of a cell (the driver cell) is enforced from the outside, then the other cell (the driven cell) will evolve toward the same logical state, since the configuration of minimum energy is the one corresponding to the pair of electrons aligned along parallel diagonals. No current flows in the circuit across cell boundaries and no traditional interconnect lines are required, which offers the perspective of extremely low power operation.

A QCA circuit performs logical operations on the basis of the so-called ''ground state computation'' principle: the input cells are set in the state corresponding to the logical input vector, the system is allowed to relax to the ground state, then the logical output vector is obtained by reading the final states reached by the output cells. It has been demonstrated by Lent *et al.*[1,2] that any combinatorial logical function can be implemented by properly assembling an array of QCA cells.

Further details on the QCA architecture can be found in Ref. 2 and references therein. Recently, experimental demonstrations of the operation of coupled QCA cells and of a majority voting gate have been successfully obtained with cells consisting of metal islands connected by capacitive tunnel junctions.[3–5] Very promising nanoscale cells have been fabricated on silicon-on-insulator substrates.[6]

A few serious drawbacks of QCA architectures have however been pointed out in the last few years. First, extremely tight fabrication tolerances (prohibitive, at least in the medium term) are required for proper operation of QCA circuits[7] without a careful adjustment of each single cell. Second, room temperature operation is not achievable with semiconductor or metal QCA systems.[8,9] The interested reader can find further details in the cited papers. Molecular implementations seem to be the only possibility of fabricating large scale QCA circuits operating at room temperature and based on the electrostatic interaction, but detailed studies on the subject are still missing, although some fundamental difficulties have already been recognized, such as that of obtaining a substrate without stray charges. Further problems may appear when ground state computation is performed on relatively large QCA systems: a large system is very likely to get temporarily stuck in a metastable state, corresponding to a wrong logical output, and to reach the ground state after an extremely long time.[10] For this reason, an adiabatic logic scheme has been proposed, in which the evolution of the system is driven by a multiphase clock.[2]

In the present work we will address the adiabatic operation of QCA circuits, focusing in particular on a recent proposal by Tóth and Lent.[11] In the following, we describe the proposed implementation of adiabatic switching; then, we perform an analytical calculation of the switching time as a function of several device parameters and, focusing on a realistic cell geometry, we determine the region in the parameter space that allows operation at an acceptable clock speed.

A. Six-dot QCA cell

Adiabatic switching of a QCA cell consists of letting the cell evolve in the instantaneous ground state, and then ''freezing'' the electron configuration when the cell must be used to drive nearby cells. This can be achieved by modulating the interdot barriers:[2] barriers should be raised to lock the electrons in the dots they are currently occupying, and then

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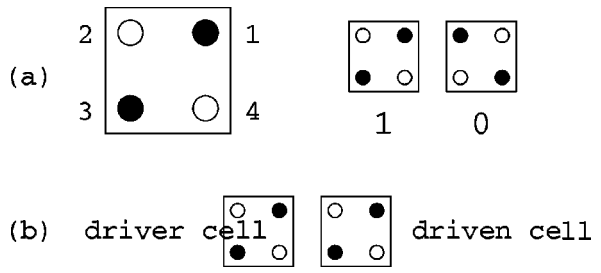

FIG. 1. (a) A QCA cell consists of four dots separated by tunneling barriers with two excess electrons; electrons tend to align along one diagonal (logical ''1'') or along the other (logical ''0''); (b) If the driver cell is set into a specific logic state, the driven cell will evolve toward the same logical state, in order to minimize the total electrostatic energy.

lowered slowly enough not to drive the system into an excited state. An interesting way of modulating the interdot barriers in a metal dot QCA implementation has been proposed in Ref. 11: it consists of replacing the barrier with another dot whose potential can be varied by means of an external voltage. A complete cell is shown in Fig. 2 and is made up of six dots: the ordinary four dots (1, 3, 4, and 6) plus the two dots required for the modulated barriers (2 and 5). The potential of each dot is adjusted by means of capacitively coupled voltage sources.

Let us first focus on the left semicell, containing dots 1, 2, and 3, whose interaction is described classically by means of capacitive couplings. The semicell configuration can be described by means of the triplet of integers $[n_1,n_2,n_3]$, which represent the occupations of dots 1, 2, and 3, respectively. Under operating conditions there is only one excess electron, thus the three possible configurations are [1, 0, 0], [0, 1, 0] and [0, 0, 1]. The semicell operation is controlled by the central-dot voltage V_c.

When V_c is kept sufficiently low as to make the [0, 1, 0] configuration energy much higher than the [1, 0, 0] or [0, 0, 1] configuration energies, the semicell is locked in one

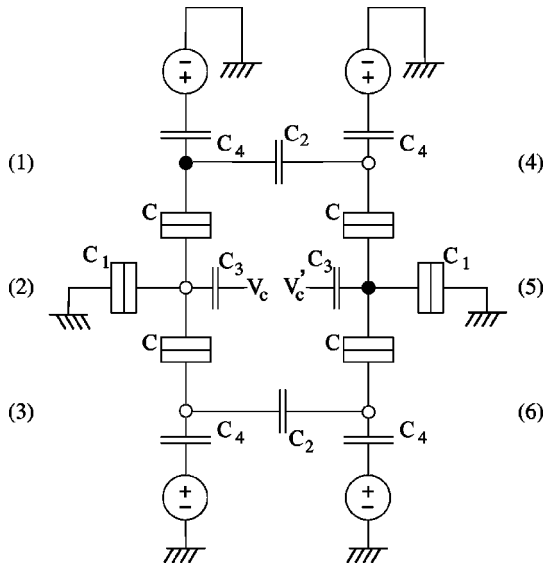

FIG. 2. The entire cell, made up of six dots. Each semicell consists of three dots connected by tunneling junctions and coupled to external voltage sources via capacitors.

of these last states, because V_c creates a potential barrier that prevents the motion of the electrons between dots 1 and 3. On the other hand, if the central-dot potential is much larger (lower electron potential energy) than the others, the semicell is said to be in the null state, which corresponds to the excess electron stuck in the central dot (state [0, 1, 0]). The last condition, the active condition, is obtained when the energy of the [0, 1, 0] configuration is comparable to that of the other configurations.

Semicell operation is achieved by varying the central-dot potential, and thus the cell condition, from the null to the locked state and vice versa. In the null state the semicell does not interact with the neighboring cells, while in the active state electrons can move across the semicell and the local ground state can be easily reached. Finally, in the locked state, the configuration is frozen and thus the semicell can be used as a driver element.

By applying an appropriate clock sequence to the cells of the QCA system, it is thus possible to control the data flow and to avoid the problems connected with the existence of metastable states.[2]

Typical operation is sketched in Fig. 2.[11] The first semicell is locked and has an excess electron in the upper dot (black dot). This causes an energy difference 2Δ between the configurations [1, 0, 0] and [0, 0, 1] of the second semicell. The second semicell is initially in the null state, and the potential of its central dot is gradually raised to allow switching: we are in the situation depicted in Fig. 3, where we show the energy levels of the three possible configurations. Figure 3(a) corresponds to the initial null state. The tunneling process becomes possible when the central level approaches the energy of the lower of the other two, as in Fig. 3(b), and becomes more important as the energy difference $\delta \equiv E_{010} - E_{001}$ increases. The single-electron tunneling rate increases with δ because of barrier distortion and of the increase in the number of electrons which can tunnel from the central dot.

While it is clear that metastable states are no longer a problem for adiabatic logic, signal propagation is limited by the switching time of single cells. Proper operation can be obtained if transition rates for tunneling are sufficiently large to allow an electron to actually tunnel into the proper dot while the cell is in the active state. Moreover, the energy unbalance 2Δ needs to be much larger than kT. In the following, we will evaluate the switching times by computing the transition rates for electrons as a function of material parameters and cell geometry, for an energy of the [0, 1, 0] configuration intermediate between those of the [1, 0, 0] and [0, 0, 1] configurations.

II. TRANSITION RATES FOR A SEMICELL

In order to obtain results in a quasianalytic form, we will make several simplifying assumptions. We emphasize that we intentionally choose approximations that lead to an overestimation of tunneling rates. This means that our results give an optimistic prediction of the maximum obtainable clock frequency.

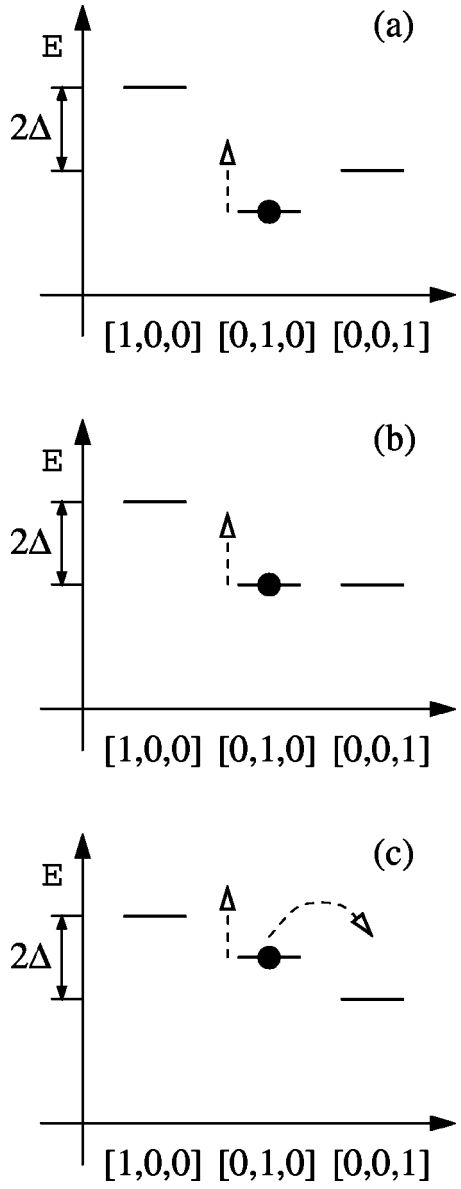

FIG. 3. Representation of the energy for the different configurations and of the tunneling path for three consecutive time steps. The [0, 1, 0] energy increases due to the decrease in the control voltage V_c'.

We neglect charging effects and energy quantization in the dots and, in addition, we consider the case in which the interdot barrier thickness is much smaller than the dot size, so that the tunneling process can be essentially studied in one dimension, in the direction normal to the junction (z axis), as shown in Fig. 4. This approximation also leads to an overestimation of the tunneling rate with respect to the three-dimensional case, since perfect overlap between transverse states is assumed.

Regions 1 and 2 in Fig. 4 represent the central and side dots, respectively, while the barrier is due to the insulating medium that separates the dots.

The important parameters are the barrier thickness a and height B, the effective electron mass in the dot m, and inside the barrier m_B, the energy offset Δ, and the distance between the Fermi level and the bottom of the conduction band in the dots E^*. If we set the reference value for the energy at the

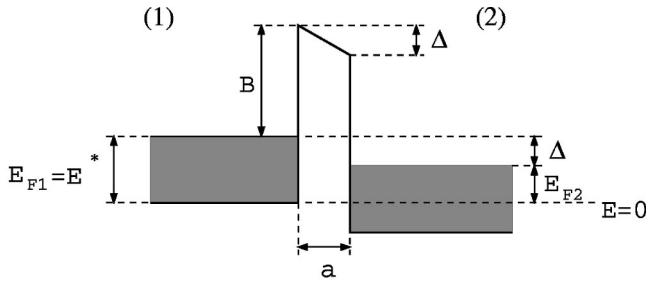

FIG. 4. The conduction band profile used to estimate the tunneling rate between the central dot and a side one. We show the typical biased situation which corresponds to Fig. 3(c).

bottom of the conduction band of dot 1, we can define the quasi Fermi levels of dots 1 and 2, respectively, as $E_{F1} \equiv E^*$ and $E_{F2} \equiv E^* - \Delta$, as shown in Fig. 4. In the following we will also need the dielectric constant ϵ of the insulator.

Let us now consider an electron of transverse wave vector $k_\parallel$ and energy E_z along the z axis. We can assume conservation of spin, total energy, and transverse wave vector during tunneling, therefore the current density across the barrier can be written as

$$J = \frac{2e}{\hbar} \int dE_z \int \frac{d^2 k_\parallel}{(2\pi)^3} 2T(E_z)[F(E,E_{F1}) - F(E,E_{F2})], \tag{1}$$

where $F(E,E_{Fi})$ is the occupation probability for a state of energy E in dot i, the 2 factor considers spin degeneracy, e is the electron charge, and $\hbar$ is the reduced Planck constant. The barrier transmission probability is denoted $T(E_z)$, which in our case does not depend on the transverse wave vector. The integral is over all $\mathbf{k}_\parallel$ and $E_z > 0$.

If we assume to be in the low temperature limit, we can describe the occupation probability as a step function and we have

$$\begin{aligned} &F(E,E_{F1}) - F(E,E_{F2}) \\ &\quad = \Theta(E - E_{F2})\Theta(E_{F1} - E) \\ &\quad = \Theta(E - E_{F1} + \Delta)\Theta(E_{F1} - E). \end{aligned} \tag{2}$$

For simplicity, we assume parabolic bands, so that $E = E_z + \hbar^2 k_\parallel^2/(2m)$, and we use for E^* an effective value which allows a correct estimation of the density of states at the Fermi energy. After performing a change of coordinates to $\eta^2 \equiv \hbar^2/(2m)(k_x^2 + k_y^2)$ and $\phi \equiv \text{arctg}(k_y/k_x)$, we can write Eq. (1) as

$$\begin{aligned} J = \frac{me}{4\pi^3 \hbar^3} \int dE_z T(E_z) \int_0^{2\pi} d\phi \int d\eta \, \eta \\ \times \Theta(E^* - E_z - \eta^2)\Theta(E_z - E^* + \eta^2 + \Delta). \end{aligned} \tag{3}$$

If $E_z < E^* - \Delta$, the integration domain is represented by the circular area enclosed between two circles of radius $\eta_1 = \sqrt{E^* - E_z - \Delta}$ and $\eta_2 = \sqrt{E^* - E_z}$, while, for $E^* - \Delta < E_z < E^*$, the domain is the disk of radius $\eta = E^* - E_z$. Thus, performing a polar integration, we obtain

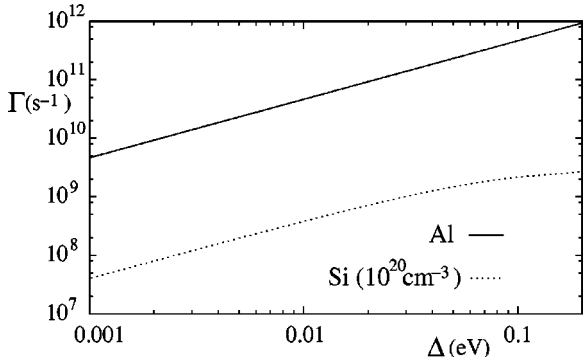

FIG. 5. The tunneling rate as a function of the energy offset Δ. The two results correspond to an Al dot (solid line) and to an *n*-doped ($n = 10^{20}\,\mathrm{cm}^{-3}$) Si dot (dashed line). In both cases we choose SiO_2 as a dielectric and the value of the parameters are: $a = 2$ nm and $S = 100\,\mathrm{nm}^2$.

$$J = \frac{me}{2\pi^2\hbar^3}\left[\int_0^{E^*-\Delta} dE_z T(E_z)\Delta - \int_{E^*-\Delta}^{E^*} dE_z T(E_z)(E^*-E_z)\right]. \tag{4}$$

We now need an explicit form for the transmission coefficient. Limiting our analysis to the case in which the barrier can be considered much higher than the electron energy, we can write

$$T(E_z) \approx \frac{E_z}{B}\exp\left[-\frac{2a}{\hbar}\sqrt{2m_B(B_{\mathrm{eff}}-E_z)}\right], \tag{5}$$

where B_{eff} is the effective height of the barrier seen by an electron of longitudinal energy E_z. If the deformation of the barrier due to the junction bias is small, we can simply choose its average height $B_{\mathrm{eff}} = B + E^* - \Delta/2$. The integrals in Eq. (4) result in a complicated polynomial expression, which we shall evaluate numerically.

If S is the area through which the electrons can tunnel from one dot to the other, the transition rate can be written as

$$\Gamma = JS/e. \tag{6}$$

If $\Delta \ll E^*$, the current density and the rate Γ depend linearly on Δ. When Δ approaches E^* we have a quasisaturation of the current [for $\Delta = E^*$ the first integral in Eq. (4) and any explicit dependence on Δ vanish]. For larger bias J still depends on Δ, but only through the dependence of the transmission coefficient T on this parameter. In Fig. 5 we plot Γ as a function of Δ for Al dots and highly doped Si dots and a SiO_2 barrier of thickness $a = 2$ nm and cross section $S = 100\,\mathrm{nm}^2$. The main difference between the two cases lies in the value of E^*. We computed it in the free electron approximation; in the metallic case we can use the measured free electron density as shown in Ref. 12 to obtain $E^* = 11.7$ eV for the Al case, while in the silicon case the parabolic approximation gives $E^* \approx 0.15$ eV. In this last case we can observe the saturation of Γ for values of Δ comparable to E^*. The linear tunneling resistance at zero temperature can be calculated as $R_T = \Delta/(e^2\Gamma)$ for $\Delta \ll E^*$.[13]

III. EXPLORATION OF THE PARAMETER SPACE

A. Tunneling rate

We want to determine the region of parameter space where the tunneling rate is large enough to allow adiabatic switching of the cell with a frequency useful for practical purposes. We assume that in order to obtain a switching frequency of 10 MHz the tunneling rate has to be at least 100 times larger: therefore our minimum transition rate is $\Gamma_{\min} = 10^9\,\mathrm{s}^{-1}$.

Before examining the particular cell described in Fig. 2, we shall discuss the general parametric dependence of the rate introduced in Eq. (6). To explore the multidimensional parameter space we need a strategy allowing for a simple visualization of the acceptable parameter regions. We first study some different material combinations and concentrate on barrier characteristics. For each considered temperature T, we assume a value of the energy unbalance Δ sufficient for operation at T, namely $\Delta = 10k_BT$. It is not trivial to satisfy this condition, as we will discuss in the following.

There are three barrier parameters: the barrier height B, the barrier thickness a and the electron effective mass inside the barrier m_B. In Figs. 6(a)–6(d) we choose $a = 2$ nm, and plot the curves corresponding to $\Gamma = \Gamma_{\min} = 10^9\,\mathrm{s}^{-1}$, given by Eqs. (4) and (5).

In each figure we show three different choices of the dot material and two values of the operating temperature: $T = 4.2$ K (solid lines) and $T = 77$ K (dashed lines). Moreover, for each temperature we report results for two typical junction surface values: $S = 10\,\mathrm{nm}^2$ and $10^4\,\mathrm{nm}^2$, which correspond to the lower and upper curve, respectively. The area below each curve corresponds to a transition rate larger than $10^9\,\mathrm{s}^{-1}$, i.e., to the acceptable region. We also added markers corresponding to the values of B and m_B of typical barrier materials.

We considered degenerately doped semiconductors, namely n^+-doped Si and Ge with $N_D = 10^{20}\,\mathrm{cm}^{-3}$ and GaAs with $N_D = 10^{19}\,\mathrm{cm}^{-3}$. In degenerate semiconductors donor levels form an extended subband, which practically mixes with the conduction band. As a result, we have an effective thinning of the energy gap and complete donor ionization, even at zero temperature, so that $n = N_D$.

In Figs. 7(a)–7(d) the same data are computed for an extremely optimistic barrier thickness $a = 1$ nm (while SiO_2 layers thinner than 1 nm have been successfully fabricated, a 1 nm thick insulating layer in the lateral direction is beyond the current state of the art).

To discuss these results, we first point out that the increase of the tunneling rate with increasing temperature is simply due to the fact that we are considering different values of Δ for each temperature, assuming that the energy unbalance Δ is equal to $10k_BT$: if T increases, we have a proportional increase of Δ and, as a consequence, of Γ. In the following section we will discuss the constraints this requirement poses on cell geometry.

As expected, the rate strongly increases with decreasing barrier thickness a. As can be seen in Fig. 7(a), with $a = 1$ nm and Al dots we can obtain a sufficiently large rate for practically any choice of insulator, temperature, and junction

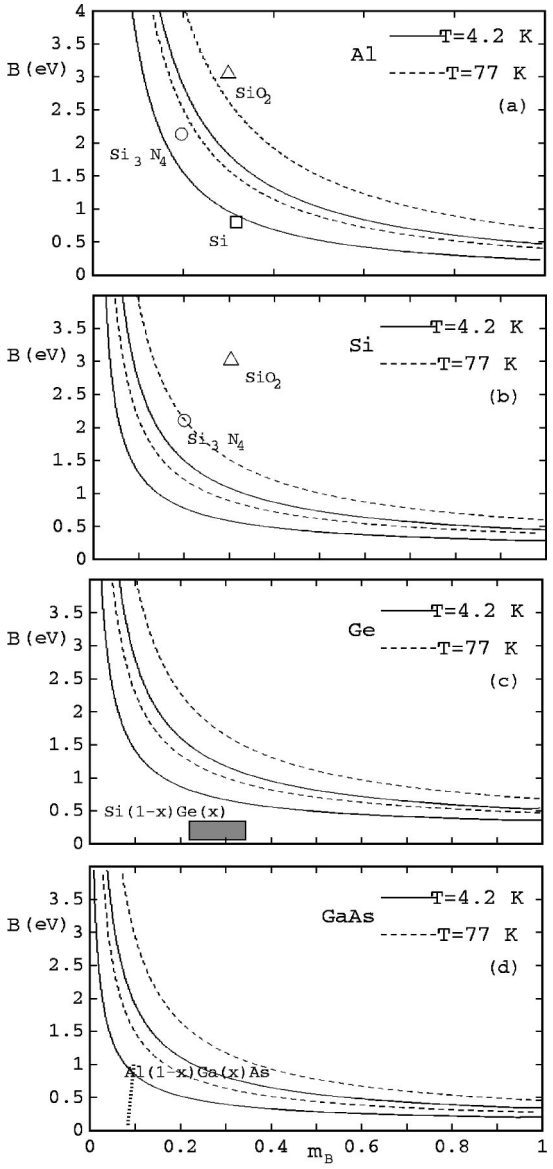

FIG. 6. The curves indicate the values of the barrier height B and of the effective mass m_B (expressed in terms of the electron mass) for which the rate $\Gamma = 10^9\ s^{-1}$. We show the $T = 4.2$ K (solid lines) and $T = 77$ K (dashed lines) cases. The two curves for each temperature indicate the rate for a junction surface S equal to $S = 10\ nm^2$ (lower curve) and $S = 10^4\ nm^2$ (upper curve). The barrier thickness is $a = 2$ nm. We consider typical barrier and dot materials. The wide dashed region in (c) approximately indicates the range of SiGe parameters for varying strain and Ge concentration. The dashed thick line in (d) indicates the range of values for an $Al_{1-x}Ga_xAs$ alloy.

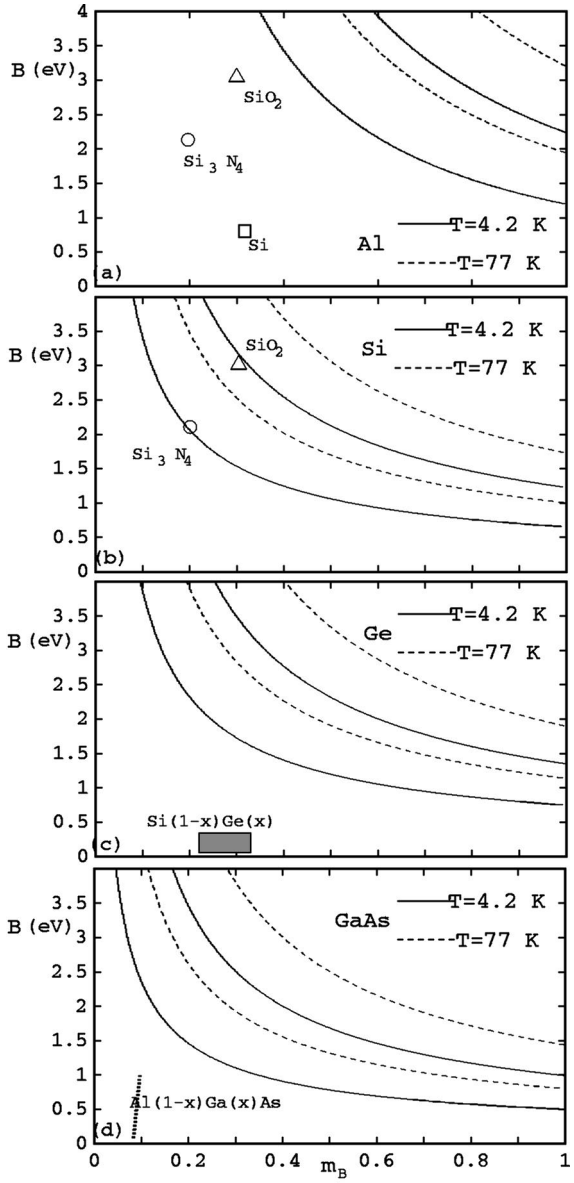

FIG. 7. The curves indicate the values of the barrier height B and of the effective mass m_B (expressed in terms of the electron mass) for which the rate $\Gamma = 10^9\ s^{-1}$. We show the $T = 4.2$ K (solid lines) and $T = 77$ K (dashed lines) cases. The two curves for each temperature indicate the rate for a junction surface S equal to $S = 10\ nm^2$ (lower curve) and $S = 10^4\ nm^2$ (upper curve). The barrier thickness is $a = 1$ nm. We consider typical barrier and dot materials. The wide dashed region in (c) approximately indicates the range of SiGe parameters for varying strain and Ge concentration. The dashed thick line in (d) indicates the range of values for an $Al_{1-x}Ga_xAs$ alloy.

area. However, Fig. 7 is mainly a demonstrative result, because fabricating a structure with such a fine spatial resolution is likely to be beyond technological capabilities in the medium term.

Figure 6 presents results for a slightly more realistic structure which, however, is still well beyond the current state of the art. From these two figures we can draw some general conclusion: with semiconductor dots, even with very high doping, the number of carriers is lower than in the metallic case while, on the other hand, the tunneling barrier height B can be much smaller and, using $Al_xGa_{1-x}As$-GaAs or Si_xGe_{1-x}-Ge, can be reasonably adjusted.

There are two possible main choices: we can use metal islands or semiconductor quantum dots. In the first case we have the advantage of a very large number of carriers available for tunneling, and the transition rate is only limited by the barrier height and the effective mass of available insulators. In the second case lower barrier heights and smaller effective mass values in the barrier are available, while the number of carriers in each dot is extremely limited. Perspectives for the metal island solution seem more promising, since the possibility of using intrinsic semiconductors as insulators can make available a wide range of thin gap materials, with low barrier height and low effective mass.

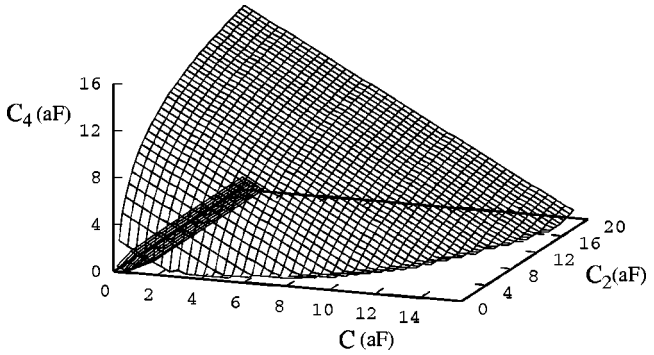

FIG. 8. The regions under the wire-mesh surfaces represent the regions in the parameter space $\{C, C_2, C_4\}$ where $\Delta > 3.6\times10^{-3}$ eV (upper surface) and $\Delta > 6.7\times10^{-2}$ eV (lower surface). The two surfaces correspond to an operating temperature of 4.2 and 77 K, respectively.

B. Energy unbalance as a function of coupling capacitances

In this section we focus on the relationship between the energy unbalance Δ and the geometrical structure of a cell. We refer to the cell described in Sec. I, and compute the electrostatic energy of the different configurations.

The cell system, made up of six metallic dots with capacitive interaction, can be described in a completely classical way by considering the values of five capacitances. The configuration energy of the cell can be written as the total energy

$$E = \frac{1}{2}(\mathbf{q}\,\mathbf{q}')\mathbf{C}^{-1}\begin{pmatrix}\mathbf{q}\\ \mathbf{q}'\end{pmatrix} - \mathbf{v}\cdot\mathbf{q}', \tag{7}$$

where $\mathbf{v}$ is the vector containing the voltages on the leads and $\mathbf{q}$,$\mathbf{q}'$ are the vectors of the charge on the dots and on the leads, respectively. $\mathbf{C}^{-1}$ is the inverse of the capacitance matrix. By using Eq. (7) we can evaluate the energy difference between two configurations which differ in the position of one electron (see Fig. 3). In our notation, this energy difference is 2Δ. Moreover, the symmetry properties of the cell we are considering warrant that Δ depends only on the three capacitances, C, C_2 and C_4, as can be seen in Fig. 2.

In Fig. 8 we show the region in the capacitance space where Δ is larger than a certain value. We show the acceptable region for two different values of Δ: $\Delta = 3.6\times10^{-3}$ eV (upper surface) and $\Delta = 6.7\times10^{-2}$ eV (lower surface), which correspond to $\Delta = 10k_BT$ for $T = 4.2$ K and $T = 77$ K, respectively. It is worthwhile to point out that the energy unbalance is a decreasing function of C and C_4 but increases as C_2 is increased. As we see from Fig. 8, the acceptable area strongly decreases as we increase the value of Δ: capacitances of the order of a few attofarad are required for operation at 4.2 K, while capacitances close to 1 aF are required for operation at 77 K. While these values can be obtained in principle, it would be extremely difficult to obtain a satisfactory tradeoff with the barrier thickness required for a sufficiently large tunneling rate.

On the other hand, a very large value of C_2 would mean a large structure, or a distance small enough to make possible electron tunneling between different semicells, which should be avoided.

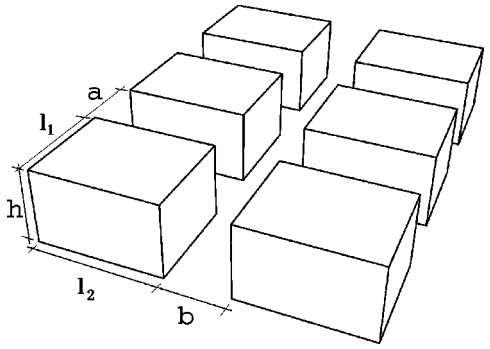

FIG. 9. A sketch of the considered cell geometry.

It is clear that the same physical and geometrical parameters affect both the transition rates and the energy unbalance in a complex way. For this reason, in Sec. IV we will consider a particular cell geometry and explore the possibility of fitting the physical constrains just discussed.

IV. AN EXAMPLE OF A SIX-DOT CELL

Let us focus on the cell of Fig. 2 and on a simple geometry, namely a cell made up of six parallelepiped dots located on a rectangular mesh as shown in Fig. 9. With this configuration the important parameters are the dot dimensions (l_1, l_2 and h), the intracell distance b and the tunneling barrier width a. We also need to take into account the dielectric constant of the insulating medium in which the dots are embedded, the tunneling barrier height B and the effective electron mass m_B in the barrier, which again depend on the insulator. The last parameters to be considered are the values of E^* and m, which depend on dot material. Considering technological limitations, we can assume a lower limit for the distances between dots on the order of a few nanometers, while we can choose the other parameters from a relatively wide range, thanks to the various material combinations that can be used.

After choosing a parameter set, we can compute the electronic tunneling rate by using the results of Sec. II and, as a first order approximation, the parallel plate capacitor formula for the evaluation of the various capacitances and of the electrostatic energy unbalance via Eq. (7).

We consider a metal–insulator cell, consisting of Al dots with three different insulators: SiO_2, Si_3N_4, and Si, and two possible values of the barrier thickness a: 2 and 3 nm. Other parameters are $b = 5$ nm and $l_1 = l_2 = h = 10$ nm, while B, m_B, and ϵ_r depend on the insulator as shown in Table I.

TABLE I. Material parameters for different choices of the insulator between Al dots. B is the barrier height, ϵ_r the relative dielectric constant, m_B the effective mass in the barrier (in units of the electron mass in a vacuum).

	SiO_2	Si_3N_4	Si
B	3.05 eV	2.1 eV	0.8 eV
ϵ_r	3.9	6.7	11.1
m_B	0.3	0.2	0.33

TABLE II. Tunneling rate γ and maximum operating temperature T_{max} for different choices of the insulator between aluminum dots. The quantity 2Δ corresponds to the energy unbalance between different configurations, a is the barrier thickness.

	$a=3$ mn			$a=2$ mn		
	SiO_2	Si_3N_4	Si	SiO_2	Si_3N_4	Si
Λ	18.9 s^{-1}	4.7×10^{5} s^{-1}	1.1×10^{7} s^{-1}	4.5×10^{5} s^{-1}	3.5×10^{8} s^{-1}	2.1×10^{9} s^{-1}
Δ	1.5×10^{-2} eV	1.2×10^{-2} eV	8.6×10^{-3} eV	9.8×10^{-3} eV	7.6×10^{-3} eV	5.1×10^{-3} eV
T_{max}	16.9 K	13.8 K	9.9 K	11.4 K	8.8 K	5.9 K

The results for the rate are shown in Table II, where we also show the energy unbalance Δ and the maximum operating temperature $T_{max}\equiv 10k_B/\Delta$.

As we noted previously, due to the exponential dependence of the rate on barrier dimensions, the barrier thickness a, the barrier height B and the mass m_B are critical parameters. The barrier thickness can be reduced if fabrication technology is improved, while m_B and B depend on material choice. For example, by simply reducing a down to 2 nm, we obtain for the previous example (with Si as an insulator) $\Gamma=2\times10^{9}\ s^{-1}$, which would be an acceptable rate.

A more detailed study can be done in the $\{a,b,L\}$ parameter space, in which we consider cubic dots with edge length L. In Fig. 10 we plot the surface in the $\{a,b,L\}$ space corresponding to $\Gamma=\Gamma_{min}=10^{9}\ s^{-1}$. Points below the surface correspond to a larger tunneling rate. It is quite clear that the tunneling rate is strongly dependent on the interdot distance a and that, even for large dot sizes, we need a very small a to obtain an acceptable rate. On the surface shown in Fig. 10 we also plot curves corresponding to given maximum operating temperature values T_{max}.

This clearly represents another important constraint: very small dots (small L) and small intercell distances b are required to obtain an energy unbalance Δ suitable for operation at a temperature of a few Kelvin.

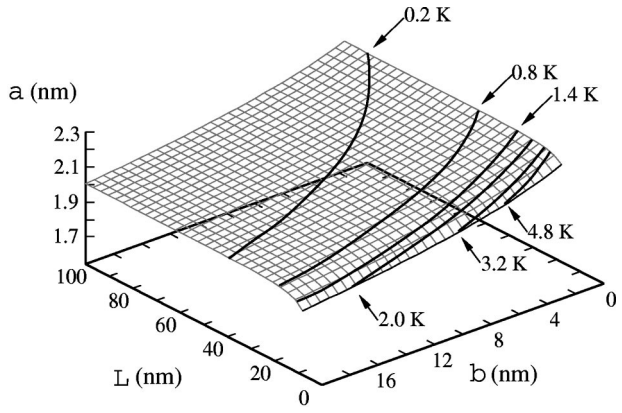

FIG. 10. The surface indicates the region in the $\{a,b,L\}$ parameter space which corresponds to a rate $\Delta=10^{9}\ s^{-1}$. All lengths are expressed in nanometers, and the device is made up of Al dots and intrinsic Si acting as an insulator. In the region below the surface the rate is larger. The continuous lines indicate the working temperature T_{max}.

V. CLOCKED QCA SIMULATOR

We performed a numerical simulation of a chain of semicells, in order to verify some of the assumptions made in the previous sections, and to assess the actually achievable operating frequency for the circuit.

We considered a simplified model, which is however still capable of reproducing the main features of the system. We studied the propagation of a signal along a QCA wire made up of five semicells. A simplified view of the chain is shown in Fig. 11, where the bias voltage sources are not indicated. We have chosen an initial condition with an excess electron in the upper dot of the first semicell and with the excess electrons of the other semicells in the central dots. The first semicell has been set in the locked state (no transition allowed) by adjusting the voltage V_c of its control gate, while all the other gate voltages have been set at a value corresponding to the null state. Then we sequentially sweep the control voltage V_c of each semicell until the end of the chain is reached, as shown at the bottom of Fig. 11.

The gate voltage is swept linearly from the value corresponding to the null state to that corresponding to the locked

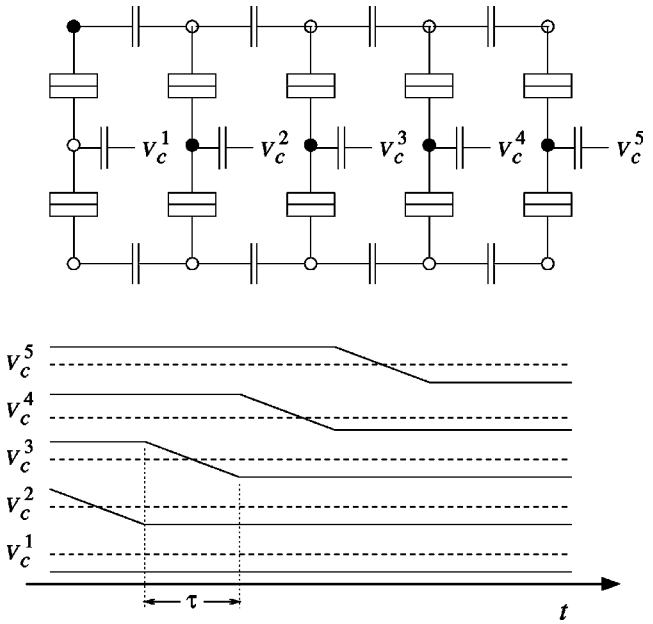

FIG. 11. A schematic view of the semicell chain and of the time sequence of the control gate voltages.

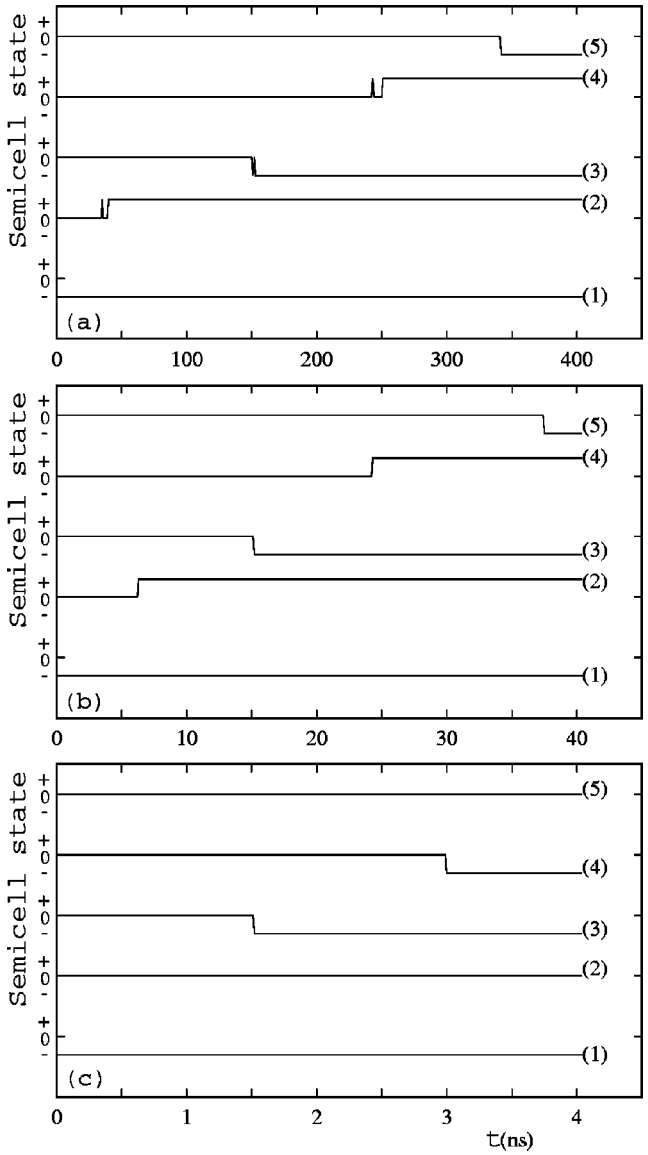

FIG. 12. Time evolution of a clocked binary array of Al–Si cells corresponding to a rise time of 10^{-7} s (a), 10^{-8} s (b), and 10^{-9} s (c). We have considered cubic Al dots with edge $L=10$ nm, intracell distance $a=2$ nm, and intercell distance $b=5$ nm. Symbols 0, −, and + on the vertical axis correspond to states [0, 1, 0], [1, 0, 0], and [0, 0, 1], respectively.

state; the rise time τ can be assumed to be one quarter of the period of the trapezoidal clock.

For the simulation, we need to know the values of the capacitances and of the tunneling resistance. These parameters can be obtained from the previously described model, once device sizes and materials have been specified. In particular, the tunneling resistance R_T is obtained from the tunneling rate of Eq. (6). We can also include the effect of finite temperature on the transition probability between two configurations which differ by an energy Δ[13] so that the transition rate reads

$$\Gamma = \frac{\Delta}{e^2 R_T (1-\exp(-\Delta/k_B T))}. \tag{8}$$

This will allow also for transitions to a higher energy configuration.

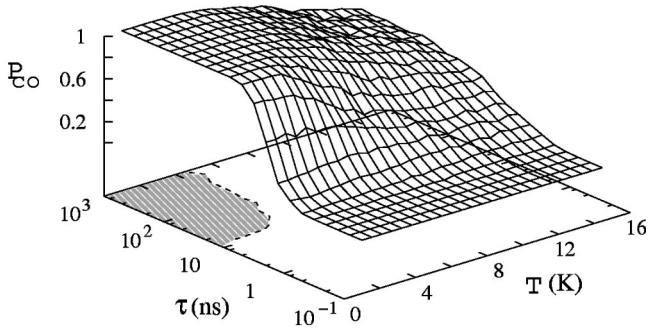

FIG. 13. Probability of correct operation P_{co} of a clocked QCA chain as a function of the rise time τ and temperature. We have considered cubic Al dots with edge $L=10$ nm, intracell distance $a=2$ nm, and intercell distance $b=5$ nm. The shaded area corresponds to a value of P_{co} larger than 0.99.

The maximum and minimum values for V_c, which correspond to the locked and null states, depend on system parameters. We determine them by computing the energy of the three possible semicell configurations. The maximum value of V_c (which corresponds to the null state) is that for which the [0, 1, 0] configuration energy is $10k_BT$ lower than the minimum energy between the [1, 0, 0] and [0, 0, 1] configurations. Similarly, the minimum value of V_c is that for which the energy of the [0, 1, 0] configuration is $10k_BT$ higher than the maximum between [1, 0, 0] and [0, 0, 1].

We consider semicells consisting of cubic 10 nm Al dots embedded in Si, with intercell distance $a=2$ nm and intracell distance $b=5$ nm. From Table II, the maximum operating temperature of such cells is 5.9 K and the transition rate is $\Gamma=2.1\times10^9\ \mathrm{s}^{-1}$.

We perform the simulation at a temperature of 2 K, lock the first cell in state [1, 0, 0] and sequentially activate the other semicells through the control gate voltage, as shown in the lower part of Fig. 11. The time evolution of the state of all semicells for a single Monte Carlo run is shown in Fig. 12 for three different values of the rise time τ: 10^{-7} s [Fig. 12(a)], 10^{-8} s [Fig. 12(b)], and 10^{-9} s [Fig. 12(c)].

As can be seen, for $\tau=10^{-7}$ [Fig. 12(a)] thermal heating allows the semicell to bounce back and forth between the initial and final configurations during the active state, while this behavior is not observed for $\tau=10^{-8}$ s [Fig. 12(b)]. Proper operation is not obtained for the shorter rise time $\tau=10^{-9}$ s [Fig. 12(c)], which is comparable to $1/\Gamma$.

A quantitative assessment of QCA chain operation as a function of temperature and rise time can be done by performing a simulation over a statistical ensemble of Monte Carlo runs. In Fig. 13 we plot the probability of correct operation P_{co} as a function of temperature and rise time. P_{co} is close to unity for $\tau>2\times10^{-8}$ s and $T<3$ K, while it goes smoothly to zero for higher temperatures and smaller rise times.

VI. DISCUSSION

We have investigated the feasibility of an adiabatic logic scheme for cellular automaton systems based on cells in which the tunnel barriers between dots can be controlled by an external voltage. Information flow is driven by a four-

phase trapezoidal clock, which removes the problem of metastable states that might be responsible for indefinite delays in the evolution of the system towards the ground state.

We have derived a quasianalytical formula for the tunneling rates between dots for typical material parameters and device geometries, and we have evaluated the region in the parameter space that allows a transition rate of at least $10^9\ s^{-1}$, which would make possible a clock frequency of 10 MHz. A clock frequency much smaller than 10 MHz would not be interesting from the point of view of applications, because the speed of propagation along a binary wire is limited to the ratio of cell-to-cell distance to the rise time (a quarter of the clock period). Let us point out that in our derivation we have consistently used approximations that lead to an overestimation of transition rates. This means that our model can be used to select promising solutions for further investigation.

Implementations based on metal islands embedded in intrinsic semiconductors used as insulators seem the most promising, providing at the same time large electron density and low barrier heights. Based on the results derived, we have focused on a specific example of a six-dot Al–Si cell with a transition rate larger than $10^9\ s^{-1}$ at 4.2 K, and have used a purposely developed Monte Carlo simulator to test the validity of our assumptions and evaluate the maximum operating frequency in the temperature range 0–16 K.

While the proposed structure can successfully operate at a clock frequency slightly larger than 10 MHz at a temperature up to 3 K, we must point out again that fabrication of such a device structure is beyond the technological capabilities expected in the medium term. The problem of metastable states is successfully solved with the adiabatic logic scheme, but the overhead circuitry required for individually tuning each cell in order to compensate for asymmetries due to fabrication tolerances and stray charges is still required, in addition to that for clock distribution. This is the most serious obstacle for any actual large-scale implementation of QCA systems except, maybe, for those based on magnetic nanostructures[14] and, possibly, molecular cells, whose development is currently at a very early stage.

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