# *Characterization of Soft Breakdown in Thin Oxide NMOSFETs Based on the Analysis of the Substrate Current*

**Felice Crupi**
Dipartimento di Fisica della Materia e Tecnologie Fisiche Avanzate,
Università di Messina
**Giuseppe Iannaccone**
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni,
Università di Pisa
**Isodiana Crupi**
Istituto Nazionale di Metodologie e Tecnologie per la Microelettronica (IMETEM),
Consiglio Nazionale delle Ricerche
**Robin Degraeve**
Interuniversity Micro-Electronics Center (IMEC)
**Guido Groeseneken**
Interuniversity Micro-Electronics Center (IMEC)
**Herman E. Maes**
Interuniversity Micro-Electronics Center (IMEC)

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# Characterization of Soft Breakdown in Thin Oxide NMOSFETs Based on the Analysis of the Substrate Current

Felice Crupi, Giuseppe Iannaccone, Isodiana Crupi, Robin Degraeve, Guido Groeseneken, *Senior Member, IEEE*, and Herman E. Maes, *Fellow, IEEE*

***Abstract*—We have investigated the properties of soft breakdown (SBD) in thin oxide (4.5 nm) nMOSFETs with measurements of the gate and substrate leakage currents using the carrier separation technique. We have observed that, at lower gate voltages, the level of the substrate current exhibits a plateau. We propose that the observed plateau is due to the Shockley-Hall-Read (SHR) generation of hole-electron pairs in the space charge region and at the Si-$SiO_2$ interface. At higher voltages, the substrate current steeply increases with voltage, due to a tunneling mechanism, trap-assisted or due to a localized effective thinning of the oxide, from the substrate valence band to the gate conduction band, which becomes possible for gate voltages higher than the threshold voltage. The proposed interpretation is consistent with the results of measurements performed at different operating conditions, in the presence of light and in the case of substrate reverse bias. The presented results are also useful for characterizing the performance of MOSFETs after SBD.**

***Index Terms*—Dielectric breakdown, leakage currents, MOSFETs, reliability.**

## I. Introduction

SOFT BREAKDOWN (SBD) has been extensively studied in recent years because of its implications on the reliability of thin silicon dioxide films [1]–[11]. Such phenomenon is characterized by a large increase of the low field current and of the noise at the gate electrode. Depending on the type of induced noise, two SBD modes have been identified:

1) the *analog* or *stable* mode, characterized by $1/f$ noise, and
2) the *digital* or *unstable* mode, characterized by random telegraph signal (RTS) noise [8], [9].

Several models of soft breakdown (SBD) have been proposed, but a general consensus on the main transport mechanism is still missing. In particular, Yoshida *et al*. [4] proposed that SBD conduction could be caused by a dramatic increase of the direct tunneling current component due to the formation of a localized conducting filament which extends into the oxide within 3 nm from the $SiO_2$/Si interface. On the other hand, Halimaoui *et al*. [5] found that the best fit of the current–voltage ($I-V$) characteristic after SBD with a direct tunneling mechanism requires a potential barrier height of 6.2 eV, which is not realistic. Therefore, they suggested that SBD coincides with the generation of conducting paths between the electrodes, in which the transport mechanism is the same as for the hard breakdown (HBD) case. The higher conductance observed after the HBD could be explained by a difference in the effective cross section of the conducting path.

Other models are based on trap-assisted-tunneling: in particular, Okada *et al*. explained the temperature dependence of the current through the SBD spot by the variable range hopping model, where transport is mediated by localized states, including various trap sites and interface states induced by the electrical stressing [6]. The power law behavior of the $I-V$ characteristics observed in the SBD regime is explained in [7] with a distribution of percolation thresholds, on the basis of the percolation theory of nonlinear conductor networks.

All the above-mentioned work investigates the SBD phenomenon in MOS capacitors, where only the gate current can be monitored. On the other hand, using nMOSFETs, additional data on transport in the SBD regime can be obtained, by means of the simultaneous observation of the substrate current. Lee *et al*. reported that the SBD event gives rise to a large substrate current jump at the high stress fields [2]. They proposed that the physically damaged region of the SBD spot effectively lowers the barrier for holes and reduces the hole tunneling distance, resulting in a large increase of hot hole injection from the anode. Recently, the characteristics of the substrate current as a function of the gate voltage after SBD were reported [9]: current noise at the gate and substrate electrodes exhibit a strong correlation in both the analog and digital SBD mode.

This paper focuses on an experimental investigation of the substrate current, with the aim of acquiring further information on the transport mechanisms through the SBD spot and on the characteristics of nMOSFETs after SBD. Indeed, the substrate current provides information complementary to the gate current, enabling verification of existing models. We report new experimental results on the substrate current in nMOSFETs after analog SBD in different operating conditions and propose an explanation of its origin.

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F. Crupi is with the Dipartimento di Fisica della Materia e Tecnologie Fisiche Avanzate, Università di Messina, I-98165 Messina, Italy.

G. Iannaccone is with the Dipartimento di Ingegneria dell'Informazione, Università di Pisa, I-56126 Pisa, Italy.

I. Crupi is with the Istituto Nazionale di Metodologie e Tecnologie per la Microelettronica (IMETEM), Consiglio Nazionale delle Ricerche, I-95121 Catania, Italy.

R. Degraeve, G. Groeseneken, and H. E. Maes are with the Interuniversity Micro-Electronics Center (IMEC), B-3001 Leuven, Belgium.

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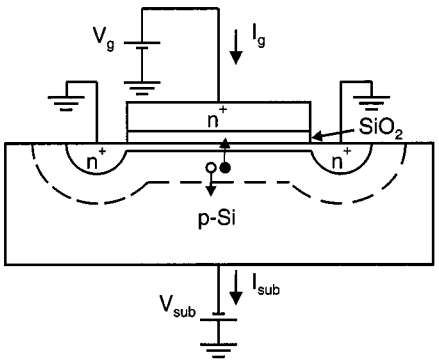


Fig. 1. Experimental setup for carrier separation in nMOSFETs.

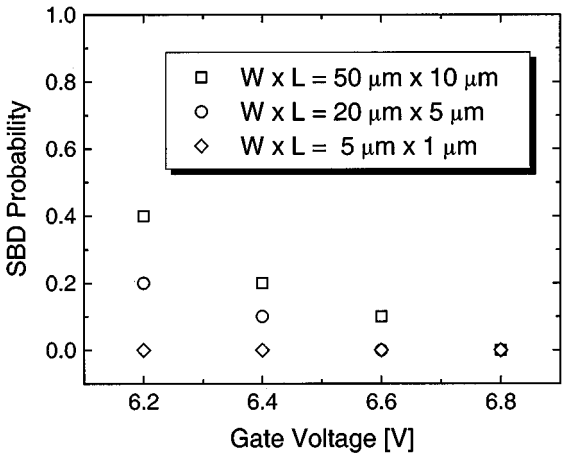


Fig. 2. SBD probability as a function of the applied gate voltage for different geometries of the oxide layer. Each point corresponds to ten samples. The SBD incidence increases reducing the applied voltage and in larger devices.

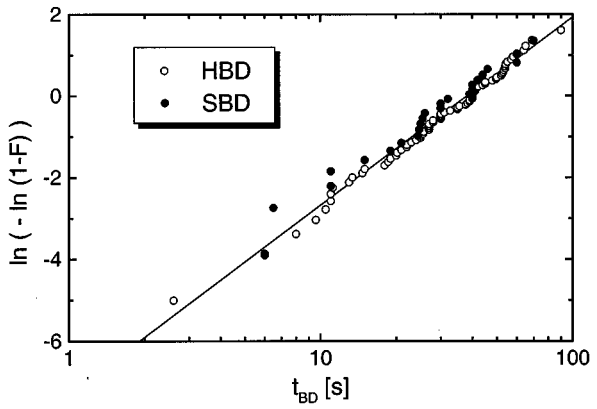


Fig. 3. Weibull plot of the distributions of the time to breakdown $t_{\rm BD}$ for soft and hard breakdown. It is clearly observed that the two distributions are well fitted by the same Weibull distribution.

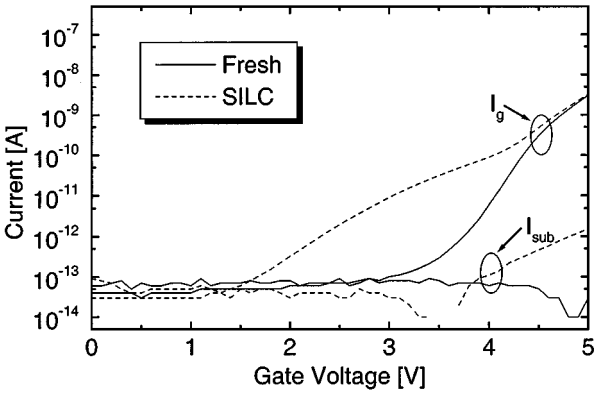


Fig. 4. Gate and substrate currents as a function of the gate voltage in a fresh oxide (a-solid line) and in the SILC regime (a-dashed line).

## II. Experimental Procedure

The starting material is a (100)-oriented p-type silicon substrate. The edge structure of the devices was realized by local oxidation of silicon (LOCOS). The 4.5-nm thick oxide results from a wet oxidation at 700 °C. The gate was implanted with phosphorus at 30 keV (dose $2 \times 10^{14}$ cm$^{-2}$). After the definition of the gate, arsenic was implanted into the source and drain regions at 75 keV. The electrodes were silicided and then metalized with aluminum in order to obtain a low contact resistance for the electrical measurements. The threshold voltage $V_{\rm th}$, measured on several samples, is 1.1 V, and no significant change was observed after SBD, in agreement with other results presented in the literature [10].

We performed all the experiments biasing the nMOSFETs in the inversion region using the Ginovker carrier separation configuration [12]–[15], illustrated in Fig. 1. Due to the applied voltages, the gate current is almost entirely caused by the electron current flowing from the inversion layer, whereas a hole current can be measured as substrate current.

## III. Results and Discussion

Several samples with different geometries have been stressed at different gate voltages. A threshold of 100 $\mu$A for the gate current increase at the first breakdown event was chosen in order to distinguish between SBD and HBD. The two breakdown modes were clearly distinguished because the typical gate current jump was close to 1 $\mu$A for SBD and more than 1 mA for HBD. The obtained results, shown in Fig. 2, clearly indicate that the SBD probability increases with decreasing stress voltage and device area, in agreement with the results reported in [11].

In order to compare the time to breakdown ($t_{\rm BD}$) distributions for SBD and HBD, 100 samples have been stressed at a condition where both soft and HBD can be observed. We have computed the two distribution functions of $t_{\rm BD}$ for soft and hard breakdown, $F_{\rm SBD}$ and $F_{\rm HBD}$, respectively, and have plotted $\ln(-\ln(1-F))$ as a function of $\ln(t_{\rm BD})$, both for $F = F_{\rm SBD}$ and $F = F_{\rm HBD}$. As can be seen in Fig. 3, both curves are well fitted by the same straight line, i.e., by the same Weibull distribution. This observation allows us to measure a unique distribution of the first breakdown event at higher fields and extrapolate to the lower fields used in the normal operating conditions of the devices, because only the SBD probability will change.

Figs. 4 and 5 show the gate current $I_g$ and the substrate current $I_{\rm sub}$ as a function of the gate voltage $V_g$ at different degradation stages, with $V_{\rm sub} = 0$ V. The curves of Fig. 4 were measured for a fresh oxide and after high field stress that causes additional stress-induced leakage current (SILC) at both electrodes. A large increase of both currents is observed after SBD,

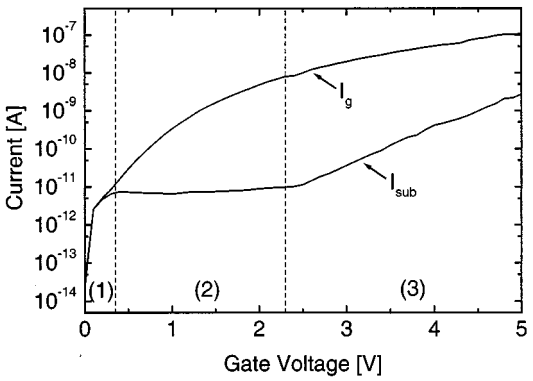


Fig. 5. Gate and substrate currents as a function of the gate voltage after SBD. Three different regions can be identified in the substrate current.

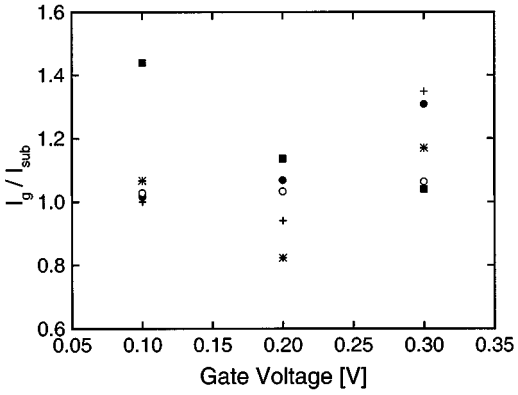


Fig. 6. Values of the ratio of the gate current to the substrate current at low gate voltages for five different samples.

as shown in Fig. 5. A limited device-to-device variation is observed in the post-SBD curves, being dependent on the particular failure occurred; nevertheless, they exhibit a regular and reproducible behavior, which allows to identify clearly three different regions.

The first region is defined by $0 < V_g < V_{P1} \sim 0.3 - 0.5$ V (Fig. 5): both $I_g$ and $I_{\rm sub}$ increase with the applied voltage, and have approximately the same value. This is confirmed by the data shown in Fig. 6, where the ratio $I_g/I_{\rm sub}$ in the first region is plotted for five different devices after SBD, and in all cases is very close to one, meaning that $I_g$ and $I_{\rm sub}$ are practically coincidental. The second region is defined by $V_{P1} < V_g < V_{P2}$, where $V_{P2}$ has value in the range of 1.1–2.5 V, depending on the particular sample. In this region, $I_g$ rapidly increases with $V_g$, while $I_{\rm sub}$ exhibits a plateau ranging from a few picoamperes to a few tens of picoampere, again depending on the particular sample. The plateaus are usually rather flat, and in many cases the substrate current exhibits a shallow minimum near the middle of the plateau. In the third region $(V_g > V_{P2})$ the behavior of the gate current is practically unchanged, while the substrate current steeply increases with the gate voltage.

In Fig. 7 the conduction and valence bands are shown, computed with a one-dimensional (1-D) self-consistent Poisson-Schrödinger solver for different values of the gate voltage. For $V_g$ lower than $V_{P1}$ [Fig. 7(a)] the current is basically due to the generation of hole-electron pairs in the space charge region and at the Si-$SiO_2$ interface via the Shockley-Hall-Read (SHR) mechanism, and to the consequent drift and diffusion of carriers toward the channel and the substrate. In the case of fresh oxide electrons cannot escape the inversion layer, therefore recombination exactly balances generation, drift and diffusion in both directions are balanced, and there is no net current. When SBD occurs, generated electrons are quickly collected at the gate electrode and holes at the substrate electrode, so that there is a net deficit of carriers in the channel region that sustains generation and hence the current.

Since the gate voltage is still very low, electrons cannot reach the channel from the contacts because of the high potential barrier they encounter, therefore $I_g$ and $I_{\rm sub}$ must be practically identical, as shown in Fig. 6.

In the second region $(V_{P1} < V_g < V_{P2})I_g$ rapidly increases with respect to $I_{\rm sub}$ because a new contribution is added

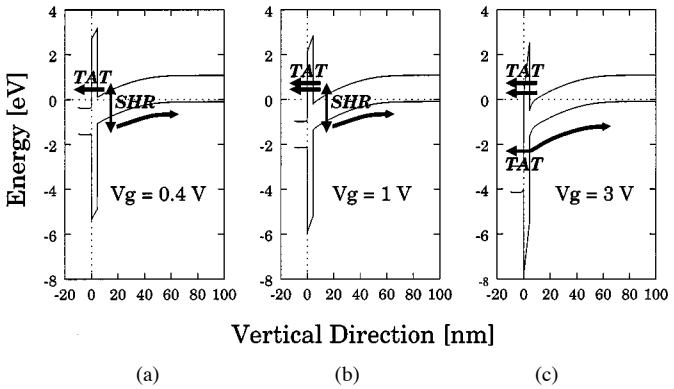


Fig. 7. Conduction and valence band profiles computed with a one-dimensional (1-D) Schrödinger-Poisson solver for different values of the gate voltage: (a) 0.4 V; (b) 1 V; and (c) 3 V. SHR indicates Shockley-Hall-Read generation, while TAT stays for trap-assisted tunneling or tunneling through an effectively thinned oxide region).

to $I_g$. With increasing $V_g$, the transmission probability of the gate oxide rapidly increases, and electrons in the inversion layer are more effectively collected at the gate. In addition, when $V_g$ approaches $V_{\rm th}$, the potential barriers from the drain and source contacts to the Si-$SiO_2$ interface are progressively lowered, so that electrons from the contacts easily reach the SBD spot and contribute to $I_g$. Since there is a low-impedance path for electrons from the contacts to the gate, the quasi-Fermi level for electrons in the channel is virtually unchanged, leaving diffusion and generation currents between the substrate and the channel unchanged. This is the reason for the plateau of $I_{\rm sub}$.

When $V_g$ is increased above $V_{P2}$, $I_{\rm sub}$ undergoes a steep increase, because a new mechanism becomes dominant: as can be seen in Fig. 7(c), for $V_g$ greater than $V_{\rm th}$, some type of tunneling from the valence band in the bulk to the conduction band of the gate can take place (e.g., trap-assisted-tunneling or tunneling through a localized thinner spot of the oxide). This contribution to the current increases more rapidly than the gate current, since the number of states available for interband tunneling increases superlinearly with the gate voltage, while electrons in the conduction band available for tunneling are proportional to $V_g - V_{\rm th}$.

The interpretation of the substrate current behavior discussed above is consistent with the data shown in Fig. 8, where sub-

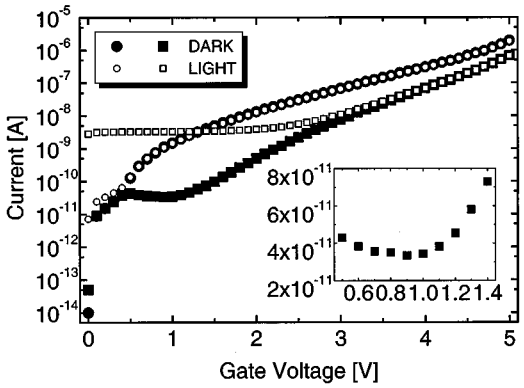


Fig. 8. Gate (circles) and substrate (squares) currents after SBD at dark and under light irradiation. Illumination increases only the plateau of the substrate current. The inset highlights a threshold in the substrate current at about 1.1 V.

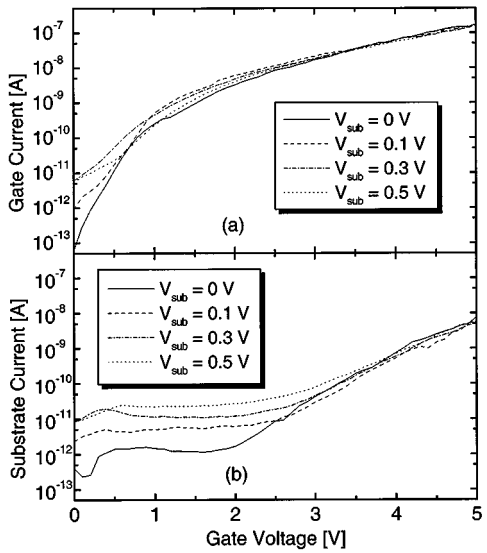


Fig. 9. (a) Gate and (b) substrate currents as a function of the gate voltage for different values of the substrate voltage after SBD. Only the plateau of the substrate current increases significantly with the substrate voltage.

strate and gate currents after SBD at dark and under light irradiation are plotted as a function of $V_g$. As can be seen, only the substrate current in the first and second region is greatly enhanced by light, confirming the fact that electron-hole generation in the space charge region and/or at the $SiO_2$ interface is the dominant mechanism. On the other hand, in the third region, both $I_{\rm sub}$ and $I_g$ are due to mechanisms completely unaffected by photon absorption.

It is worth noticing that the device considered in Fig. 8 has the highest substrate current among the samples considered, therefore has a highly conductive SBD spot: for this reason, it has the lowest value of $V_{P2}$, which is practically equal to $V_{\rm th}$ (as highlighted in the inset), consistent with the minimum allowed value of $V_g$ for interband tunneling.

In Fig. 9, the gate and substrate currents are plotted as a function of $V_g$ for different values of the substrate voltage $V_{\rm sub}$. With increasing $V_{\rm sub}$ the generation of carriers in the space charge region is enhanced because the depletion region is widened, and quasi-Fermi levels for electrons and holes are separated; in addition, a net current is established due to electrons from the substrate (minority carriers) being drifted by the electric field toward the channel region and then tunneling to the gate. Both these factors increase the substrate current in the first and second region, while, as expected, they do not affect other components of $I_g$ and $I_{\rm sub}$.

## IV. Conclusion

An experimental investigation of the substrate current in nMOSFETs after SBD has been performed in different operating conditions. In addition, an interpretation of the experimental results has been presented in substantial agreement with the measurements performed. In our opinion, two main aspects still need to be clarified. The first is whether generation of electron-hole pairs occurs mainly in the space charge region or at the silicon-silicon dioxide interface, due to traps induced by SBD. The second is the detailed tunneling mechanism of electrons and holes through the SBD spot. From the characterization of the substrate current, it is clear that a sort of interband tunneling is dominant at higher gate voltages (when the conduction band of the gate overlaps with the valence band of the substrate). The experimental results are consistent with a description based on trap-assisted-tunneling and on the presence of a conducting filament, but not with an ohmic conductive region. The main problem in the investigation of the mentioned issues is the extreme variability of the characteristics of SBD spots, which makes it difficult to compare and correlate quantitatively results from different samples. For this reason, it is extremely important to obtain as much information as possible from the same sample; therefore, we think that the simultaneous measurement of current due to electrons and holes could make easier the development and validation of a quantitative model for transport through the SBD spot.

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**Felice Crupi** was born in Lamezia Terme, Italy, on December 21, 1972. He received the degree in electrical engineering (cum laude) from Università di Messina, Messina, Italy, in 1997. He is currently pursuing the Ph.D. degree at Università di Pisa, Pisa, Italy.

In 1998 and 1999, he was Visitor at the Interuniversity Micro-Electronics Center (IMEC), Leuven, Belgium, and in 2000 he was Visitor at the IBM T. J. Watson Research Center, Yorktown Heights, NY. In 2000, he joined the Dipartimento di Fisica della Materia e Tecnologie Fisiche Avanzate, Università di Messina, as a Research Contractor. His main research interests include the modeling of the degradation and of the breakdown processes in thin oxide layers, the study of the noise in MOSFET devices, and the design of ultralow-noise instrumentation.

**Giuseppe Iannaccone** was born on April 28, 1968. He received the "laurea" degree (summa cum laude) in electrical engineering and the Ph.D. degree with a thesis on transport and noise phenomena in ultrasmall structures, both from Università di Pisa, Pisa, Italy, in 1992 and 1996, respectively.

He is currently on the Faculty of the Dipartment of Information Engineering (Dipartimento di Ingegneria dell'Informazione) of the Università di Pisa, as "Ricercatore" (Assistant Professor). He is currently the coordinator of the European research project NanoTCAD (Nanotechnology Computer Aided Design), funded within the Nanotechnology Information Device Initiative of the IST Program. His interests include transport and noise modeling in nanoelectronic devices, detailed numerical modeling of realistic nanoscale devices, the exploitation of quantum effects in conventional electron devices, and investigation of new device concepts.

**Isodiana Crupi** was born in Lamezia Terme, Italy, on May 11, 1974. She received the degree in electrical engineering (cum laude) from Università di Messina, Messina, Italy, in 1999.

In 1999, she was Visitor at the Interuniversity Micro-Electronics Center (IMEC), Leuven, Belgium. In the same year, she joined the Istituto Nazionale di Metodologie e Tecnologie per la Microelettronica (IMETEM), Consiglio Nazionale delle Ricerche (CNR), Catania, Italy. Her main research activities cover the modeling of the degradation and of the breakdown processes in thin oxide layers and the study of the semiconductor memory devices based on silicon nanocrystals.

**Robin Degraeve** received the M.Sc. degree in electrical engineering from the University of Ghent, Ghent, Belgium, in 1992, and the Ph.D. degree from the Catholic University of Leuven, Belgium, in 1998.

He joined the R&D Laboratory, Interuniversity Micro-Electronics Center (IMEC), Leuven, the Technology Reliability and Yield group, where he is currently a Researcher. His present interests and activities cover hot-carrier reliability issues in MOSFETs, the study of the physics of degradation and breakdown phenomena in oxides, the reliability of ultrathin oxide layers for VLSI technologies, and high-k materials as MOSFET gate insulators for future CMOS generations.

Mr. Degraeve presented short courses at several conferences (IRPS, P2ID, ESREF, and UCPSS) and serves as a member of the program committee of IRPS, INFOS, and SISC.

**Guido Groeseneken** (M'80–SM'95) was born in Belgium on March 27, 1958. He received the M.Sc. degree in electrical and mechanical engineering in 1980 and the Ph.D degree in applied sciences in 1986, both from the Katholieke Universiteit (KU), Leuven, Belgium. His Ph.D. work was on programming and degradation behavior of EEPROM memory cells and technologies.

From 1980 until 1987, he was with the Laboratory for Physics and Electronics of Semiconductors, KU Leuven, as a Research Assistant (1980–1984) and Senior Research Assistant (1985–1987) of the Belgian National Fund for Scientific Research (NFWO). Since 1987, he has been with the R&D Laboratory, IMEC, Leuven, where he is now responsible for research in reliability physics for submicron CMOS and nonvolatile memory technologies. He has authored or coauthored more than 150 publications, more than 100 conference contributions, and three book chapters in his fields of expertise.

Dr. Groeseneken has served as a member of several international scientific conferences, among which IEDM, IRPS, SISC, INFOS, and ESSDERC. In 1999, he chaired the Process and Device subcommittee for the International Reliability Physics Symposium, as well as the CMOS Device and Interconnect Reliability committee of the IEEE International Electron Devices Meeting.

**Herman E. Maes** (S'73–M'73–SM'89–F'98) was born in Leuven, Belgium, on August 15, 1947. He received the M.Sc. degree in electrical engineering in 1971 and the Ph.D. degree in 1974, both from the Katholieke Universiteit (KU), Leuven.

From 1971 until 1974, he was a Research Assistant (Fellow of the National Fund of Scientific Research of Belgium, NFWO) in the laboratory for Physics and Electronics of the University of Leuven. In 1974, he was granted a CRB fellowship by the Belgian American Educational Foundation and spent 14 months at the Electrical Engineering Research Laboratory of the University of Illinois, Urbana, as a Research Associate. From 1975 until 1985, he was with the ESAT laboratory at the University of Leuven as a Senior Research Associate of the Belgian National Fund for Scientific Research and a Lecturer at the university. Since 1985, he has been a Professor at the University of Leuven. In 1985, he joined the newly established R&D Laboratory of the Interuniversity Micro-Electronics Center (IMEC), Leuven, as Head of Analysis and Reliability. In 1990, he became an Associate Vice-President in IMEC and in 1998 Vice-President, heading the Division on "Silicon Technology and Device Integration." He has authored or coauthored more than 320 international technical papers including eight book chapters and more than 340 conference papers including more than 40 invited papers. He has been guiding 25 students to the Ph.D. degree over the past ten years. His current interests cover nonvolatile memory devices (including Ferro-electric memories), silicon integration, physics of semiconductor devices, reliability issues and physics of integrated circuits, and the use of physical techniques in semiconductor related problems.

Dr. Maes was elected a Fellow of the IEEE in 1997 for contributions in the field of nonvolatile silicon memory devices and for contributions to MOS reliability physics.