Characterization of Soft Breakdown in Thin Oxide NMOSFETs Based on the Analysis of the Substrate Current

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Abstract—We have investigated the properties of soft breakdown (SBD) in thin oxide (4.5 nm) nMOSFETs with measurements of the gate and substrate leakage currents using the carrier separation technique. We have observed that, at lower gate voltages, the level of the substrate current exhibits a plateau. We propose that the observed plateau is due to the Shockley-Hall-Read (SHR) generation of hole-electron pairs in the space charge region and at the Si-SiO₂ interface. At higher voltages, the substrate current steeply increases with voltage, due to a tunneling mechanism, trap-assisted or due to a localized effective thinning of the oxide, from the substrate valence band to the gate conduction band, which becomes possible for gate voltages higher than the threshold voltage. The proposed interpretation is consistent with the results of measurements performed at different operating conditions, in the presence of light and in the case of substrate reverse bias. The presented results are also useful for characterizing the performance of MOSFETs after SBD.

Index Terms—Dielectric breakdown, leakage currents, MOSFETs, reliability.

I. INTRODUCTION

SOFT BREAKDOWN (SBD) has been extensively studied in recent years because of its implications on the reliability of thin silicon dioxide films [1]–[11]. Such phenomenon is characterized by a large increase of the low field current and of the noise at the gate electrode. Depending on the type of induced noise, two SBD modes have been identified:

1) the analog or stable mode, characterized by 1/f noise, and
2) the digital or unstable mode, characterized by random telegraph signal (RTS) noise [8], [9].

Several models of soft breakdown (SBD) have been proposed, but a general consensus on the main transport mechanism is still missing. In particular, Yoshida et al. [4] proposed that SBD conduction could be caused by a dramatic increase of the direct tunneling current component due to the formation of a localized conducting filament which extends into the oxide within 3 nm from the SiO₂/Si interface. On the other hand, Halimaoui et al. [5] found that the best fit of the current–voltage (I-V) characteristic after SBD with a direct tunneling mechanism requires a potential barrier height of 6.2 eV, which is not realistic. Therefore, they suggested that SBD coincides with the generation of conducting paths between the electrodes, in which the transport mechanism is the same as for the hard breakdown (HBD) case. The higher conductance observed after the HBD could be explained by a difference in the effective cross section of the conducting path.

Other models are based on trap-assisted-tunneling: in particular, Okada et al. explained the temperature dependence of the current through the SBD spot by the variable range hopping model, where transport is mediated by localized states, including various trap sites and interface states induced by the electrical stressing [6]. The power law behavior of the I-V characteristics observed in the SBD regime is explained in [7] with a distribution of percolation thresholds, on the basis of the percolation theory of nonlinear conductor networks.

All the above-mentioned work investigates the SBD phenomenon in MOS capacitors, where only the gate current can be monitored. On the other hand, using nMOSFETs, additional data on transport in the SBD regime can be obtained, by means of the simultaneous observation of the substrate current. Lee et al. reported that the SBD event gives rise to a large substrate current jump at the high stress fields [2]. They proposed that the physically damaged region of the SBD spot effectively lowers the barrier for holes and reduces the hole tunneling distance, resulting in a large increase of hot hole injection from the anode. Recently, the characteristics of the substrate current as a function of the gate voltage after SBD were reported [9]: current noise at the gate and substrate electrodes exhibit a strong correlation in both the analog and digital SBD mode.

This paper focuses on an experimental investigation of the substrate current, with the aim of acquiring further information on the transport mechanisms through the SBD spot and on the characteristics of nMOSFETs after SBD. Indeed, the substrate current provides information complementary to the gate current, enabling verification of existing models. We report new experimental results on the substrate current in nMOSFETs after analog SBD in different operating conditions and propose an explanation of its origin.
II. EXPERIMENTAL PROCEDURE

The starting material is a (100)-oriented p-type silicon substrate. The edge structure of the devices was realized by local oxidation of silicon (LOCOS). The 4.5-nm thick oxide results from a wet oxidation at 700°C. The gate was implanted with phosphorus at 30 keV (dose \(2 \times 10^{14} \text{ cm}^{-2}\)). After the definition of the gate, arsenic was implanted into the source and drain regions at 75 keV. The electrodes were silicided and then metalized with aluminum in order to obtain a low contact resistance for the electrical measurements. The threshold voltage \(V_{\text{th}}\), measured on several samples, is 1.1 V, and no significant change was observed after SBD, in agreement with other results presented in the literature [10].

We performed all the experiments biasing the nMOSFETs in the inversion region using the Ginovker carrier separation configuration [12]–[15], illustrated in Fig. 1. Due to the applied voltages, the gate current is almost entirely caused by the electron current flowing from the inversion layer, whereas a hole current can be measured as substrate current.

III. RESULTS AND DISCUSSION

Several samples with different geometries have been stressed at different gate voltages. A threshold of 100 \(\mu\text{A}\) for the gate current increase at the first breakdown event was chosen in order to distinguish between SBD and HBD. The two breakdown modes were clearly distinguished because the typical gate current jump was close to 1 \(\mu\text{A}\) for SBD and more than 1 mA for HBD. The obtained results, shown in Fig. 2, clearly indicate that the SBD probability increases with decreasing stress voltage and device area, in agreement with the results reported in [11].

In order to compare the time to breakdown \(t_{\text{BD}}\) distributions for SBD and HBD, 100 samples have been stressed at a condition where both soft and HBD can be observed. We have computed the two distribution functions of \(t_{\text{BD}}\) for soft and hard breakdown, \(F_{\text{SBD}}\) and \(F_{\text{HBD}}\), respectively, and have plotted \(\ln(-\ln(1-F))\) as a function of \(\ln(t_{\text{BD}})\), both for \(F = F_{\text{SBD}}\) and \(F = F_{\text{HBD}}\). As can be seen in Fig. 3, both curves are well fitted by the same straight line, i.e., by the same Weibull distribution. This observation allows us to measure a unique distribution of the first breakdown event at higher fields and extrapolate to the lower fields used in the normal operating conditions of the devices, because only the SBD probability will change.

Figs. 4 and 5 show the gate current \(I_g\) and the substrate current \(I_{\text{sub}}\) as a function of the gate voltage \(V_g\) at different degradation stages, with \(V_{\text{sub}} = 0\text{ V}\). The curves of Fig. 4 were measured for a fresh oxide and after high field stress that causes additional stress-induced leakage current (SILC) at both electrodes. A large increase of both currents is observed after SBD,
as shown in Fig. 5. A limited device-to-device variation is observed in the post-SBD curves, being dependent on the particular failure occurred; nevertheless, they exhibit a regular and reproducible behavior, which allows to identify clearly three different regions.

The first region is defined by $0 < V_g < V_{P1} \sim 0.3 - 0.5$ V (Fig. 5): both $I_g$ and $I_{sub}$ increase with the applied voltage, and have approximately the same value. This is confirmed by the data shown in Fig. 6, where the ratio $I_g/I_{sub}$ in the first region is plotted for five different devices after SBD, and in all cases is very close to one, meaning that $I_g$ and $I_{sub}$ are practically coincidental. The second region is defined by $V_{P1} < V_g < V_{P2}$, where $V_{P2}$ has value in the range of 1.1–2.5 V, depending on the particular sample. In this region, $I_g$ rapidly increases with $V_g$, while $I_{sub}$ exhibits a plateau ranging from a few picamperes to a few tens of picamperes, again depending on the particular sample. The plateaus are usually rather flat, and in many cases the substrate current exhibits a shallow minimum near the middle of the plateau. In the third region ($V_g > V_{P2}$) the behavior of the gate current is practically unchanged, while the substrate current steeply increases with the gate voltage.

In Fig. 7 the conduction and valence bands are shown, computed with a one-dimensional (1-D) self-consistent Poisson-Schrödinger solver for different values of the gate voltage. For $V_g$ lower than $V_{P1}$ (Fig. 7(a)) the current is basically due to the generation of hole-electron pairs in the space charge region and at the Si-SiO$_2$ interface via the Shockley-Hall-Read (SHR) mechanism, and to the consequent drift and diffusion of carriers toward the channel and the substrate. In the case of fresh oxide electrons cannot escape the inversion layer, therefore recombination exactly balances generation, drift and diffusion in both directions are balanced, and there is no net current. When SBD occurs, generated electrons are quickly collected at the gate electrode and holes at the substrate electrode, so that there is a net deficit of carriers in the channel region that sustains generation and hence the current.

Since the gate voltage is still very low, electrons cannot reach the channel from the contacts because of the high potential barrier they encounter, therefore $I_g$ and $I_{sub}$ must be practically identical, as shown in Fig. 6.

In the second region ($V_{P1} < V_g < V_{P2}$) $I_g$ rapidly increases with respect to $I_{sub}$, because a new contribution is added to $I_g$. With increasing $V_g$, the transmission probability of the gate oxide rapidly increases, and electrons in the inversion layer are more effectively collected at the gate. In addition, when $V_g$ approaches $V_{th}$, the potential barriers from the drain and source contacts to the Si-SiO$_2$ interface are progressively lowered, so that electrons from the contacts easily reach the SBD spot and contribute to $I_g$. Since there is a low-impedance path for electrons from the contacts to the gate, the quasi-Fermi level for electrons in the channel is virtually unchanged, leaving diffusion and generation currents between the substrate and the channel unchanged. This is the reason for the plateau of $I_{sub}$.

When $V_g$ is increased above $V_{P2}$, $I_{sub}$ undergoes a steep increase, because a new mechanism becomes dominant: as can be seen in Fig. 7(c), for $V_g$ greater than $V_{th}$, some type of tunneling from the valence band in the bulk to the conduction band of the gate can take place (e.g., trap-assisted-tunneling or tunneling through a localized thinner spot of the oxide). This contribution to the current increases more rapidly than the gate current, since the number of states available for interband tunneling increases superlinearly with the gate voltage, while electrons in the conduction band available for tunneling are proportional to $V_g - V_{th}$.

The interpretation of the substrate current behavior discussed above is consistent with the data shown in Fig. 8, where sub-
substrate and gate currents after SBD at dark and under light irradiation are plotted as a function of $V_{G}$. As can be seen, only the substrate current in the first and second region is greatly enhanced by light, confirming the fact that electron-hole generation in the space charge region or at the SiO$_2$ interface is the dominant mechanism. On the other hand, in the third region, both $I_{SB}$ and $I_{G}$ are due to mechanisms completely unaffected by photon absorption.

It is worth noticing that the device considered in Fig. 8 has the highest substrate current among the samples considered, therefore has a highly conductive SBD spot: for this reason, it has the lowest value of $V_{R2}$, which is practically equal to $V_{th}$ (as highlighted in the inset), consistent with the minimum allowed value of $V_{G}$ for interband tunneling.

In Fig. 9, the gate and substrate currents are plotted as a function of $V_{G}$ for different values of the substrate voltage $V_{SB}$. With increasing $V_{SB}$, the generation of carriers in the space charge region is enhanced because the depletion region is widened, and quasi-Fermi levels for electrons and holes are separated; in addition, a net current is established due to electrons from the substrate (minority carriers) being drifted by the electric field toward the channel region and then tunneling to the gate. Both these factors increase the substrate current in the first and second region, while, as expected, they do not affect other components of $I_{G}$ and $I_{SB}$.

IV. CONCLUSION

An experimental investigation of the substrate current in nMOSFETs after SBD has been performed in different operating conditions. In addition, an interpretation of the experimental results has been presented in substantial agreement with the measurements performed. In our opinion, two main aspects still need to be clarified. The first is whether generation of electron-hole pairs occurs mainly in the space charge region or at the silicon-silicon dioxide interface, due to traps induced by SBD. The second is the detailed tunneling mechanism of electrons and holes through the SBD spot. From the characterization of the substrate current, it is clear that a sort of interband tunneling is dominant at higher gate voltages (when the conduction band of the gate overlaps with the valence band of the substrate). The experimental results are consistent with a description based on trap-assisted-tunneling and on the presence of a conducting filament, but not with an ohmic conductive region. The main problem in the investigation of the mentioned issues is the extreme variability of the characteristics of SBD spots, which makes it difficult to compare and correlate quantitatively results from different samples. For this reason, it is extremely important to obtain as much information as possible from the same sample; therefore, we think that the simultaneous measurement of current due to electrons and holes could make easier the development and validation of a quantitative model for transport through the SBD spot.

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REFERENCES

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