# *Simulation of time evolution of clocked and nonclocked quantum cellular automaton circuits*

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# Simulation of time evolution of clocked and nonclocked quantum cellular automaton circuits

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We have studied, by means of a Monte Carlo simulation, data propagation in quantum cellular automaton circuits, comparing the performance of nonclocked and clocked implementations. Based on two choices of fabrication parameters, we have evaluated the maximum achievable clock speed for different operating temperatures, concluding that better performance can be obtained with the clocked architecture, which, however, involves significant technological difficulties. The large discrepancy existing between a simple estimate of the cell switching time, based on the $RC$ time constant, and our results is discussed and explained by means of an intuitive argument. Two different circuits have been investigated, a binary wire and a majority voting gate, obtaining analogous results, with a slightly smaller maximum clock rate for the majority voting gate, due to the larger number of cells involved. © *2002 American Institute of Physics*.
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## I. INTRODUCTION

The quantum cellular automaton (QCA) architecture initially proposed in Ref. 1 has very innovative features with respect to conventional electronic circuits. For example, it is characterized by extreme modularity and by a very low power consumption.

The basic element of a QCA circuit is a cell made up of four quantum dots arranged at the vertices of a square, as shown in Fig. 1(a). The cell contains two excess electrons, which can tunnel between dots and encode the binary information: electrons tend to align along one of the square diagonals, giving rise to two possible polarization states, which can be associated to the two binary logic values. Adjacent cells interact via Coulomb coupling, which allows propagating logic values along a chain of cells, and, more in general, obtaining combinatorial circuits through the assembly of two-dimensional (2D) arrays of cells.[1]

In principle, QCA operation can be achieved without net current flow along the circuit, because the two electrons belonging to each cell may be prevented from tunneling to nearby cells, which leads to extremely low-power consumption. A QCA circuit performs logical operations on the basis of the so-called ''ground state computation'' principle: the *input* cells are set into the state corresponding to the logical input vector, the system is allowed to relax to the ground state, then the logical output vector is obtained by reading the final states reached by the *output* cells. Let us consider, for example, two adjacent cells such as those shown in Fig. 1(b). If the logical state of a cell (the *input* cell) is enforced from the outside, then the other cell (the *output* cell) will evolve towards the same logical state, since the configuration of minimum energy is the one corresponding to the two pairs of electrons aligned along parallel diagonals.

It has been demonstrated by Lent *et al.*[1] that any combinatorial logical function can be implemented by properly assembling 2D arrays of QCA cells. Recently, experimental demonstration of the operation of coupled QCA cells and of a majority voting gate has been achieved with cells consisting of metal islands connected by means of capacitive tunnel junctions.[2,3] Very promising nanoscale cells have also been fabricated on SOI substrates.[4]

A few serious drawbacks of the QCA architecture have however been pointed out in the last few years. First, extremely tight fabrication tolerances (prohibitive, at least in the medium term) or a careful adjustment of each cell are required for proper operation of QCA circuits.[5] Second, the operating temperature for semiconductor or metal QCA systems remains far below room temperature.[6,7] The only possibility to obtain large-scale QCA circuits operating at room temperature seems to be that of molecular implementations, although detailed studies on the subject are still missing, and some difficulties have already been recognized, such as that of obtaining a substrate completely free from stray charges. Further problems may appear when large QCA systems are considered in the framework of ground-state computation: a large system is very likely to get temporarily stuck in a metastable state and thus reach the ground state after a time too long for computational purposes.[8] For this reason, an adiabatic logic scheme has been proposed, in which the evolution of the system is driven by a multiphase clock.[9]

In a previous paper,[10] we addressed the adiabatic operation of QCA circuits, focusing on a recent proposal by Tóth and Lent.[11] We performed an analytical calculation of the switching time as a function of several device parameters and, considering a realistic cell geometry, we determined the region in the parameter space that allows operation at an acceptable clock speed. These results were supported also by means of a simple numerical simulation of a QCA wire.[10] In the present article, we report the results of numerical Monte Carlo simulations of more complex circuits, in order to better assess the differences between the operation of QCA circuits

 

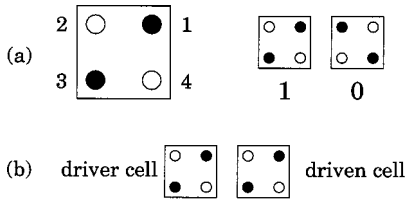


FIG. 1. (a) A QCA cell consists of four dots separated by tunneling barriers with two excess electrons; electrons tend to align along one diagonal (logical "1") or along the other (logical "0"); (b) if the driver cell is set into a specific logic state, the driven cell will evolve towards the same logical state, in order to minimize the total electrostatic energy.

based on the relaxation to the ground state and those based on an adiabatic clocked scheme.

In particular, we shall determine the maximum data processing rate that can be achieved with the two schemes and discuss the reasons for a discrepancy of several orders of magnitude between the minimum switching time for a clocked array and the estimate that can be obtained from simple considerations on the involved time constants. In Sec. II we briefly discuss the clocked model, while in Sec. III the Monte Carlo simulator is outlined, along with the approach used to include cotunneling. The overall simulation strategy is introduced in Sec. IV, while Sec. V deals with the analysis of a clocked and of a nonclocked binary wire, including an intuitive justification of the results achieved. Finally, the performance of a more complex logic gate, a majority voting gate, is discussed in Sec. VI, and conclusions are presented in Sec. VII.

## II. SIX-DOT CLOCKED QCA CELL

The problem of the existence of metastable states could be avoided if we were able to modulate the potential barriers which separate cell dots. By lowering and raising these barriers, we could drive the system towards the correct logical output without getting stuck in any metastable state. For this purpose, an adiabatic logic scheme has been proposed, in which the evolution of the system is driven by a multiphase clock.[9]

Adiabatic switching of a QCA cell consists in letting the cell evolve into the instantaneous ground state, and then "freezing" the electron configuration when the cell must be used to drive nearby cells. This can be achieved by modulating the interdot barriers:[9] barriers should be raised to lock the electrons in the dots they are currently occupying, and then lowered slowly enough not to drive the system into an excited state.

An interesting way of modulating the interdot barriers in a metal-dot QCA implementation has been proposed in Ref. 11: it consists of replacing the barrier with another dot whose potential can be varied by means of an external voltage. A clocked cell is shown in Fig. 2 and is made up of six dots: the ordinary four dots (1, 3, 4, and 6) plus the two dots required for implementation of the modulated barriers (2 and 5). The potential of each dot is adjusted by means of capacitively coupled voltage sources.

The operation of circuits based on the cell of Fig. 2 has been previously described, for example, in Refs. 10 and 11.

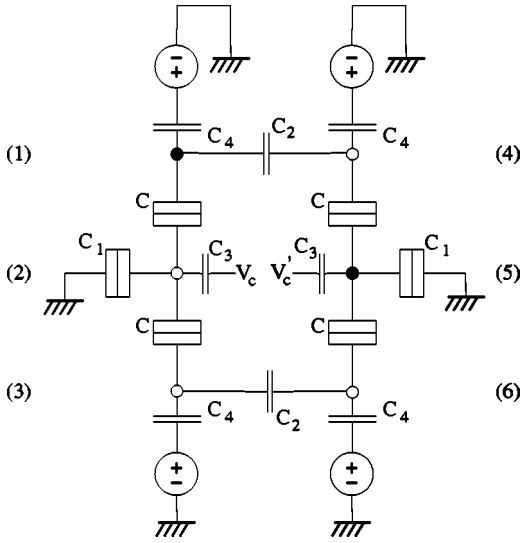


FIG. 2. Complete cell, made up of six dots. Each semicell consists of three dots connected by tunneling junctions and coupled to external voltage sources via capacitors.

By applying an appropriate clock sequence to the cells, it is possible to control the data flow and to avoid the problems connected with the existence of metastable states.[9] However, while metastable states are no longer a problem for adiabatic QCA logic, signal propagation is still limited by the switching time of single cells. Proper operation can be obtained if transition rates for tunneling are sufficiently large to allow an electron to actually tunnel into the proper dot while the cell is in the active state. Moreover, the typical energy differences between the various electronic configurations in the cells need to be much larger than $kT$, in order to prevent thermally excited random fluctuations of the logical values. In Ref. 10, we evaluated the switching time by computing the transition rates for electrons as a function of material parameters and cell geometry. Here we shall use those results to test operation of QCA circuits with and without clock, via a Monte Carlo simulation.

## III. QCA CIRCUIT SIMULATOR

The numerical simulation of the circuits discussed in the following has been performed with a semiclassical approach, in the framework of the orthodox Coulomb blockade theory,[13] since quantum effects associated with the confinement energy can be neglected at the dimensional scale being considered, because such an energy is much smaller than the electrostatic interaction energy.

We used a Monte Carlo code that we have developed,[12] specifically adapted to cope with circuits containing clocked single-electron devices. Our software allows simulating circuits made up of capacitors, tunneling capacitors, and voltage sources, with very few topological constraints. The voltage sources can provide piecewise linear waveforms. Cotunneling has also been taken into consideration, although approximately.[14]

Our code is based on a semistatic Monte Carlo technique: the simulation is divided into a given number of steps, and, for each step, we first evaluate the adjustment gate volt-

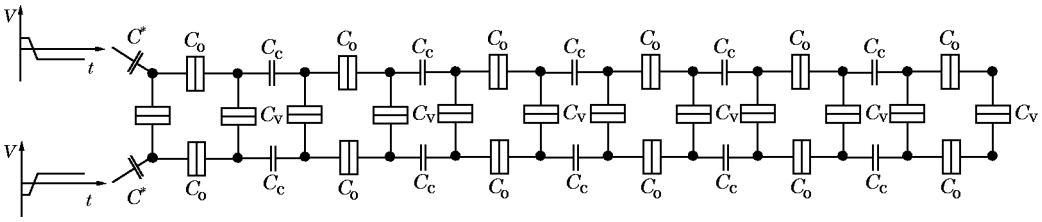


FIG. 3. Chain made up of six nonclocked cells. The first cell to the left is coupled to external leads via the capacitors $C^*$. The voltage variations which enforce the state of the first cell are sketched next to such capacitors.

ages, according to the linear evolution rule defined in the input file, then we compute the variation of the free energy $\Delta E$ associated with each possible single-electron transition through the tunneling junctions. Once the free-energy variations have been determined, we can compute the corresponding probability rates using the "orthodox" Coulomb blockade theory[13]

$$\Gamma = \frac{1}{e^2 R_T} \frac{\Delta E}{1 - e^{-\Delta E/k_B T}}, \tag{1}$$

where $R_T$ is the tunneling resistance, $e$ the electron charge, $k_B$ the Boltzmann constant, and $T$ the temperature.

In this way, we can compute all the transition rates, and the actual transition taking place is chosen randomly with a relative probability proportional to its rate. The transition is then implemented by changing the dot occupancy, the new gate voltage configuration is computed, and the same procedure repeated until the total predefined simulation time has elapsed.

This standard procedure does not take into consideration the cotunneling effect, namely, the possibility of simultaneous tunneling of two or more electrons. This effect is usually far less probable than single-electron tunneling, but can become prevalent when no direct tunneling transition is energetically viable (negative $\Delta E$), while simultaneous many-electron tunneling transitions can lead to a lower-energy state.

A rigorous simulation of the cotunneling effect is quite a difficult task, but, as we shall discuss later, we have realized that in some range of parameters cotunneling cannot be disregarded, if the nonclocked scheme of Sec. II is adopted. Thus, we have included its effects, considering only the first-order contribution, which corresponds to the simultaneous tunneling of two electrons. Following Fonseca *et al.*,[14] we can write the two-electron cotunneling probability as

$$\Gamma = \frac{\hbar}{12\pi e^4} \frac{1}{R_T^{(1)}} \frac{1}{R_T^{(2)}} \times \left[ \frac{1}{\Delta E^{(1)} - \Delta E/2} + \frac{1}{\Delta E^{(2)} - \Delta E/2} \right]^2 \times \frac{\Delta E}{e^{\Delta E/k_B T} - 1} [\Delta E^2 + (2\pi k_B T)^2)]. \tag{2}$$

This expression is not suitable for numerical simulation, because of the divergences occurring when one of the intermediate transitions matches one half of the total energy difference. This problem can be avoided by resorting to the following approximate expression:

$$\Gamma = \frac{16}{3} \frac{\hbar}{\pi} \frac{C^2}{e^8 R_T^2} \frac{\Delta E}{e^{\Delta E/k_B T} - 1} [\Delta E^2 + (2\pi k_B T)^2)], \tag{3}$$

where $R_T$ and $C$ represent, respectively, the average value of the tunneling resistance and of the capacitance of the junctions involved in the cotunneling event. This expression is a somehow crude approximation, but it has been shown[14] to give the correct order of magnitude of the effect, which is what we need.

## IV. CIRCUITS AND SIMULATION STRATEGIES

In order to test the operation of clocked and nonclocked architectures, we studied two different circuits: a linear chain made up of six QCA cells and a majority voting gate made up of eight QCA cells. They are shown in Figs. 3–5. For the linear chain, we present both the nonclocked and the clocked implementation, while for the majority voting gate we report only the circuit diagram for the nonclocked version, since the other can be easily derived looking at that for the clocked linear chain. The greater complexity of the clocked case is apparent. In Figs. 3–5, we sketch also the time evolution of the applied potentials that produces switching of the first cell, while in Fig. 4, the clocked external gate potentials are shown).

The simulation strategy differs in the two cases. In the case without clock, we are strictly following the ground-state calculation paradigm. Namely, the circuit output becomes valid after the system has relaxed to the ground state. In the case of the chain, this implies that we can perform the simulation starting from the ground state, with all the cells in the same logical state, then switching the first cell via the above-mentioned voltage variation, and observing the time evolution, until the new ground state is reached. By repeating several times the simulation, we shall be able to check circuit reliability and to compute the average time needed to reach the correct logical output.

In the clocked case, the situation is different, because the switching time is enforced from the outside. Thus, in order to check circuit operation, we follow the time evolution of each single cell and verify that its logical state is correct in the appropriate time intervals. In this case, we do not need to

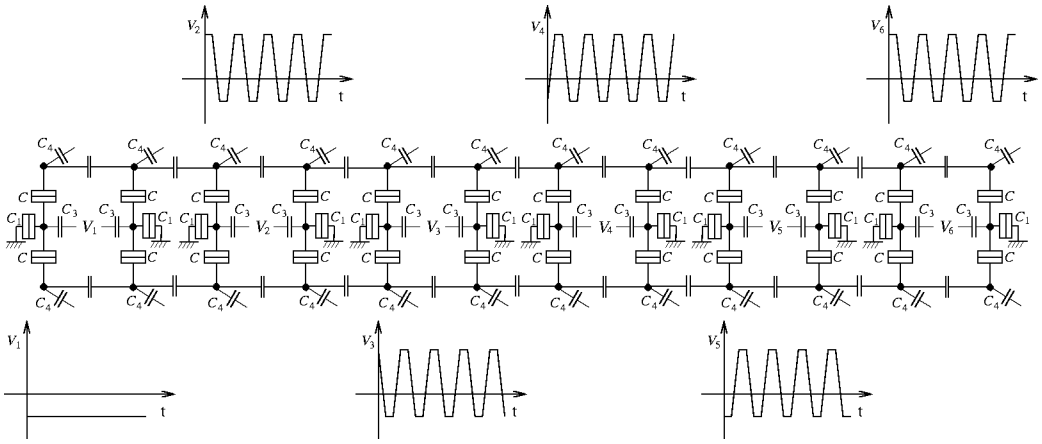

FIG. 4. Chain made up of six clocked cells like the one represented in Fig. 2. The external voltages which drive the cells are labeled as $V_1, V_2 \cdots V_6$ and their time behavior is sketched below and above the circuits diagram. The value of the capacitors which connect the cells is indicated as $C_c$ in Table II.

average over several different histories, because statistics can be obtained observing a large enough number of clock cycles.

Before presenting simulation results, we need to discuss our choice of system parameters. Our goal is both to check the validity of experimental results by extending them to more complex circuits and to forecast the operation of future devices. We have thus chosen two different sets of parameters: the first has been obtained from the recent experiments that have successfully shown operation of simple QCA devices,[2,3] while the second has instead been derived from our previous work, in which we theoretically discussed the limits of clocked QCA devices.[10] In that paper, we performed a parametric study to assess the feasibility of clocked QCA devices studying different material combinations. The choice reported in the second line of Tables I and II has been ob-

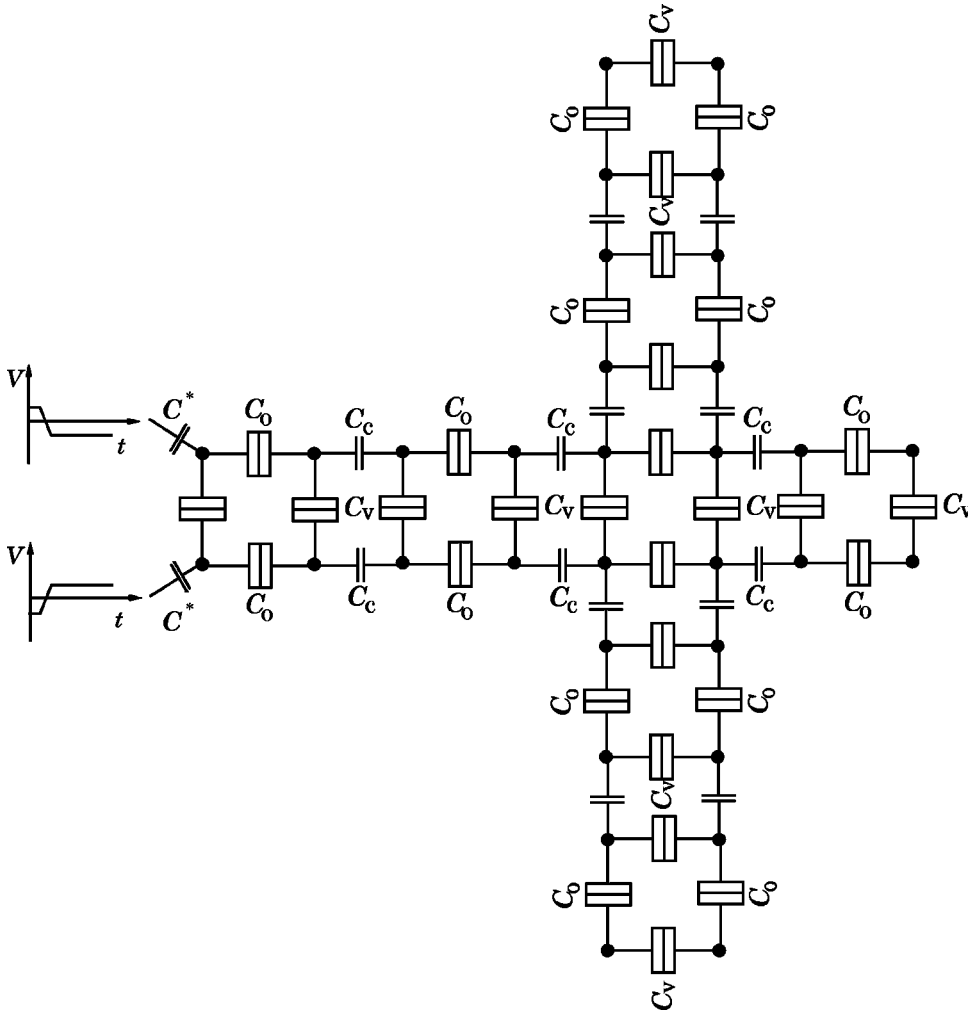

FIG. 5. A majority voting gate made up of nonclocked cells. The first cell to the left is coupled to external leads via the capacitors $C^*$. The voltage variations which cause switching of the first cell are sketched to the left. The other two input cells, at the top and bottom of the vertical arm, are kept in a constant logical state via appropriate external gates (not shown), during the whole time evolution.

TABLE I. Circuit parameters for the nonclocked case.

| | $C_o$ (aF) | $C_v$ (aF) | $C_c$ (aF) | $C^*$ (aF) | $R_T$ (kΩ) |
|---|---|---|---|---|---|
| Experimental values[2,3] | 400 | 288 | 88 | 1 | 200 |
| Theoretical prediction[10] | 5.3 | 5.3 | 2 | 0.1 | 200 |

tained as a tradeoff between miniaturization, efficiency, and technical feasibility. Such a small and precise structure is not yet realizable but it could be so in not too far a future.

## V. BINARY WIRE SIMULATIONS

This section is devoted to the study of the operation of the binary wires shown in Figs. 3 and 4. As already discussed, we start with the simulation of devices based on the parameters of experimentally realized cells. The following results have been obtained with cell parameters similar to those of Ref. 2.

The time evolution of the six cells of the chain of Fig. 3 is shown in Fig. 6. We have chosen to indicate the logical states with the symbols 1, $x$, and 0, where 1 and 0 correspond to the two valid polarization states, while $x$ indicates all the other cell states with the two electrons not aligned along one of the diagonals. The initial condition for the simulation is the chain ground state, with all the cells in the logical state 0. After a short time, we switch the first cell state to 1, by means of a change in the external voltages applied to the left end of the chain. After the switching event, the system is not in the ground state any more, and it evolves to relax into the new ground state, which is reached when all the cells are in the logical state 1 (the first cell cannot switch back to 0, due to the external bias). It is apparent from the figure that the relaxation process does not proceed in a regular and smooth way, but, rather, the system moves randomly among the various chain states. Many of these states are actually very close in energy and, due to thermal activation, states of significantly higher energy can be reached, too.

The average relaxation time to the ground state is a statistical quantity which we studied by averaging over several realizations of the time evolution. The average value of the relaxation time, $\langle t_{\mathrm{rel}} \rangle$, as a function of temperature is shown in Fig. 7. We notice that $\langle t_{\mathrm{rel}} \rangle$ decreases as temperature increases. This is due to the increased tunneling rate, but such a phenomenon is limited by the fact that beyond a certain temperature, the system no longer approaches a stable ground state, because of thermal fluctuations. In Fig. 7, we marked with a dashed pattern the approximate region whithin which the circuit is not working any more. Anyway, before entering this region we already have hints of degraded

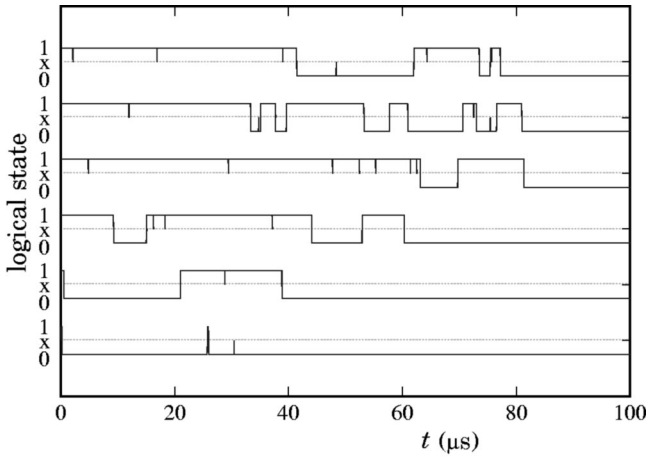


FIG. 6. Time evolution of the logical states of the six cells of a QCA chain in the nonclocked case. The values of the parameters are $C_o = 400$ aF, $C_v = 288$ aF, $C_c = 88$ aF, $C^* = 1$ aF, and $R_T = 200$ kΩ.

operation in the sudden increase of the relaxation time and in the broadening of the distribution (see $T = 0.85$ K and notice that the vertical scale is logarithmic).

Knowledge of the average relaxation time is not sufficient to assess how fast the circuit can perform, because we need to take into consideration that the distribution of relaxation times can exhibit long tails, and thus $\langle t_{\mathrm{rel}} \rangle$ is actually too conservative an estimate. This is clear from Fig. 8, where we show the relaxation time distribution for $T = 0.05$ K. We obtained quite broad distributions in all of the simulations, with long tails that are the consequence of the existence of metastable states, although they do not play a major role in a simple circuit such as the considered chain.

We notice also that, as temperature decreases, the importance of cotunneling events increases. If we define $R_{\mathrm{ct}}$ as the ratio of the number of cotunneling events to that of tunneling events, we obtain, for the case at hand, that $R_{\mathrm{ct}} = 35$ at $T = 0.025$ K, which means that cotunneling is the predominant phenomenon, while $R_{\mathrm{ct}} = 1.4 \times 10^{-2}$ at $T = 0.075$ K.

With the other parameter set, namely, the one obtained in Ref. 10, we have found a similar behavior, but on different temperature and time scales. The results of the simulation are shown in Figs. 9–10: the average relaxation time is now smaller and the operating temperature is higher, but the overall behavior is qualitatively similar to that obtained with the previous parameter choice, i.e., we still have a broad relaxation time distribution, with long tails. Performance improvements are an obvious consequence of the larger voltage imbalance achievable with smaller devices (characterized by smaller capacitance values). A larger voltage imbalance im-

TABLE II. Circuit parameters for the clocked case.

| | $C$ (aF) | $C_1$ (aF) | $C_2$ (aF) | $C_3$ (aF) | $C_4$ (aF) | $C_c$ (aF) | $R_T$ (kΩ) |
|---|---|---|---|---|---|---|---|
| Experimental values[2,3] | 420 | 300 | 25 | 80 | 200 | 50 | 200 |
| Theoretical prediction[10] | 5.3 | 1.2 | 1.2 | 3.57 | 1.48 | 1 | 200 |

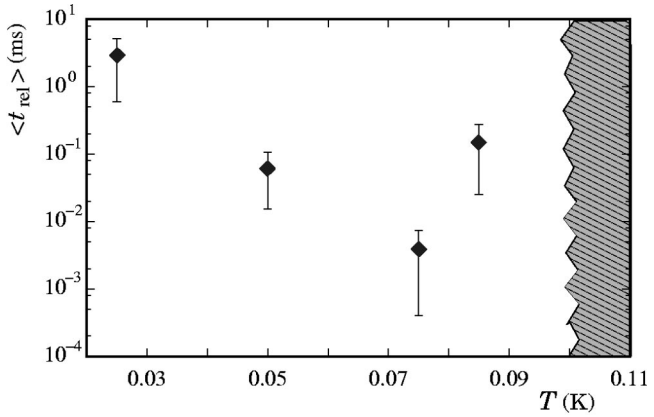


FIG. 7. Average relaxation time $\langle t_{\mathrm{rel}} \rangle$ as a function of temperature. In the dashed region, the operation is completely disrupted due to thermal fluctuations. The values of the parameters are $C_o = 400$ aF, $C_v = 288$ aF, $C_c = 88$ aF, $C^* = 1$ aF, and $R_T = 200$ kΩ.

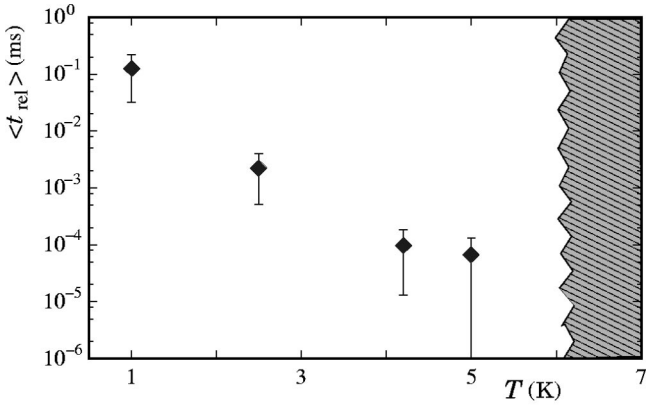


FIG. 9. Average relaxation time $\langle t_{\mathrm{rel}} \rangle$ as a function of temperature. In the dashed region, the operation is completely disrupted, due to thermal fluctuations. The values of the parameters are $C_o = 5.3$ aF, $C_v = 5.3$ aF, $C_c = 2$ aF, $C^* = 0.1$ aF, and $R_T = 200$ kΩ.

plies both a higher-tunneling rate and less sensitivity to thermal fluctuations.

Let us now move on to the clocked architecture of Fig. 4. As we discussed before, by means of an external clock driving the cells we set the rate of switching, which is not dictated by the global relaxation to the ground state any more. In this case, we need to assess whether the system relaxation to the local instantaneous ground state is fast enough to follow the changes due to the clock evolution and to result in the correct final output. A typical evolution is shown in Fig. 11, for the choice of parameters represented by the first row in Table II: in the considered time interval we can see only one propagation error. Reliability of circuit operation, as already discussed in Ref. 10, depends on clock rate and on temperature. If the clock is too fast, the cell is not able to switch and the logical state is lost. The same happens for a temperature that is too high compared to the energy imbalance. We can safely disregard cotunneling, because its contribution is far less important in the clocked case, due to the fact that the barrier modulation makes the direct transition always available. Cotunneling effects, if present, are thus not needed for reaching the ground state, as they were instead in the nonclocked case.

In order to assess the reliability of circuit operation, we performed runs over several (250) clock cycles. During these runs, we checked the logical state of the second and the sixth (last) cell of the chain, and calculated the number of times such cells are in the state expected as correct; in this way we were able to compute the relative frequency of correct output $P_{\mathrm{CO}}$ over the total number of clock cycles. By "checking the logical state," we mean observing the cell state during the time interval which corresponds to the locked condition for that cell. In such an interval, the cell should be in the expected logical state. Actually, this is strictly true only at very low temperature, because when the temperature is comparable to the energy difference between logical states, we can see the cell switching back and forth between them.

We then need to properly define the meaning of *correct logical state* for the observed cell, and this can be done by addressing the measurement process. The measurement of the electron occupancy can be performed by averaging the cell state over the locked time interval, and thus we can decide to consider a cell to be in the correct state if it remains in that state for more than a certain percentage of the time interval. We choose such a percentage as 90%.

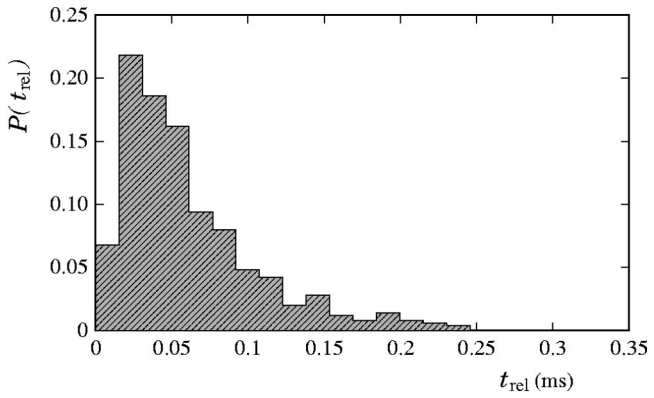


FIG. 8. Distribution of the switching time $\langle t_{\mathrm{rel}} \rangle$ for the nonclocked chain of Fig. 3, for $T = 0.05$ K. The values of the parameters are $C_o = 400$ aF, $C_v = 288$ aF, $C_c = 88$ aF, $C^* = 1$ aF, and $R_T = 200$ kΩ.

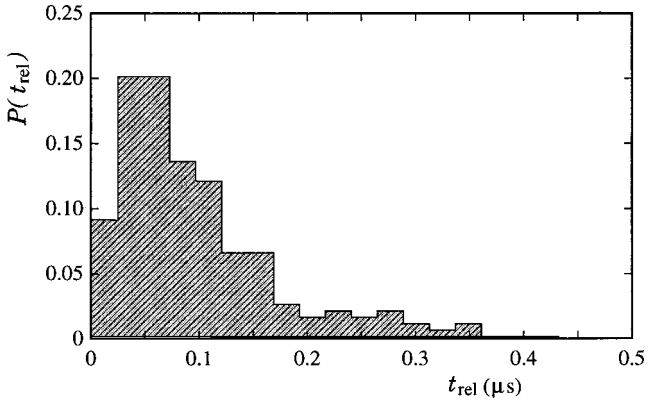


FIG. 10. Distribution of the relaxation time $\langle t_{\mathrm{rel}} \rangle$ for the nonclocked chain of Fig. 3, for $T = 4.2$ K. The values of the parameters are $C_o = 5.3$ aF, $C_v = 5.3$ aF, $C_c = 2$ aF, $C^* = 0.1$ aF, and $R_T = 200$ kΩ.

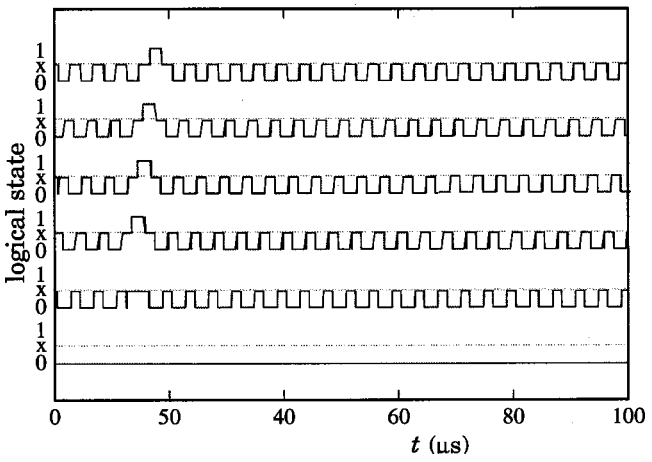


FIG. 11. Time evolution of the logical states of the six cells of a QCA chain in the clocked case. The capacitor values are: $C=420$ aF, $C_1=300$ aF, $C_2=25$ aF, $C_3=80$ aF, $C_4=200$ aF, $C_c=50$ aF. The resistance of the tunneling junctions between dots is $R=200$ kΩ, while the junctions which connect the dots to the ground have a resistance of $10^{10}$ Ω.

With this prescription, we have obtained the results shown in Figs. 12 and 13. In each figure, we show the percentage of correct output $P_{CO}$ as a function of the clock period $\tau$. The solid curves refer to the last cell, while the dashed ones refer to the second cell. We have considered two different temperatures: $T=0.01$ K (a) and $T=0.025$ K (b). Figure 12 clearly shows how circuit operation deteriorates with increasing clock frequency and temperature. Moreover, it is clear that $P_{CO}$ decreases as we proceed along the chain, due to the fact that the overall error probability increases with the number of intermediate cells. This process has been studied in Refs. 6, 7, 15, where it has been shown that the error probability increases as the logarithm of the number of cells in a linear chain.

The temperature range we studied has been chosen on the basis of the following considerations. For the present selection of parameters, we have observed that temperature effects become negligible below $T=0.01$ K; therefore, we have selected this value as the lower bound of the interval of analysis. As far as the upper bound of the interval is concerned, we have chosen a value $T=0.025$ K, because for larger temperature values thermal fluctuations completely disrupt the operation of the circuit.

We repeated the simulation with the other parameter set, obtaining the results shown in Fig. 13 for three temperatures: 1 K (a), 2.5 K (b), and 4.2 K (c). Similar comments apply to this result, although the temperature range is different and we were able to find a region of correct operation that extends down to a clock period of $10^{-7}$ s and to a temperature of 2.5 K, which could be a reasonable operating condition. This last choice of parameters is the same as that used in Ref. 10 to compute the probability of correct operation of a similar but simpler linear chain. In that case, the basic block of the chain was a semicell, namely, only half of the cell shown in Fig. 2. The total chain was thus made up of only 18 dots. Our present results are consistent with those of the previous paper and the slightly better performance of the cell of Ref. 10 can be attributed to the simpler structure of that circuit.

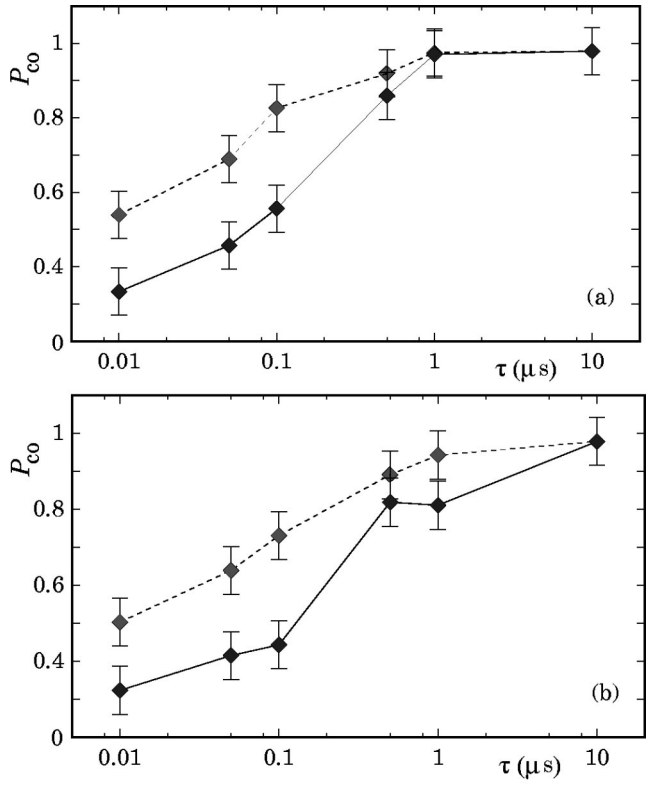


FIG. 12. Probability of correct operation ($P_{CO}$) for the second and the last cell in the clocked chain of Fig. 4 as a function of the clock period. The solid curves refer to the last cell, while the dashed ones refer to the second cell. We have considered two different temperatures: $T=0.01$ K (a) and $T=0.025$ K (b). The capacitor values are: $C=420$ aF, $C_1=300$ aF, $C_2=25$ aF, $C_3=80$ aF, $C_4=200$ aF, $C_c=50$ aF. The resistance of the tunneling junctions between the dots is $R=200$ kΩ, while the junctions which connect the dots to the ground have a resistance of $10^{10}$ Ω.

We wish to point out that the minimum clock period allowing correct operation according to our simulations is orders of magnitude larger than the intuitive estimate that could be obtained on the basis of the $R_TC$ time constant associated with the tunneling resistances and the capacitance values. Such a naive estimate would yield a typical minimum clock period around $10^{-12}$ s, which is approximately four orders of magnitude smaller than the result we get from our Monte Carlo runs.

It is instructive to discuss the origin of this discrepancy and to derive an intuitive argument justifying our numerical results. To this aim, let us consider the mechanism whereby an electron on the central dot of a semicell tunnels into the outer dot at the lower potential: tunneling into the expected dot is possible within a time interval slightly longer (due to the contribution of thermal energy) than that during which the potential of the central dot lies between those of the top and bottom dots, indicated with a bold segment in Fig. 14(a).

The voltage imbalance created between the two outer dots because of the presence of an excess electron on one of the dots in the other half of the same cell is, from our calculations, about 3 mV: considering the linearity of the ramp, we can compute, as a first approximation, the electron tunneling rate between the central dot and the outer dot at the lower potential in the condition with the central dot potential ex-

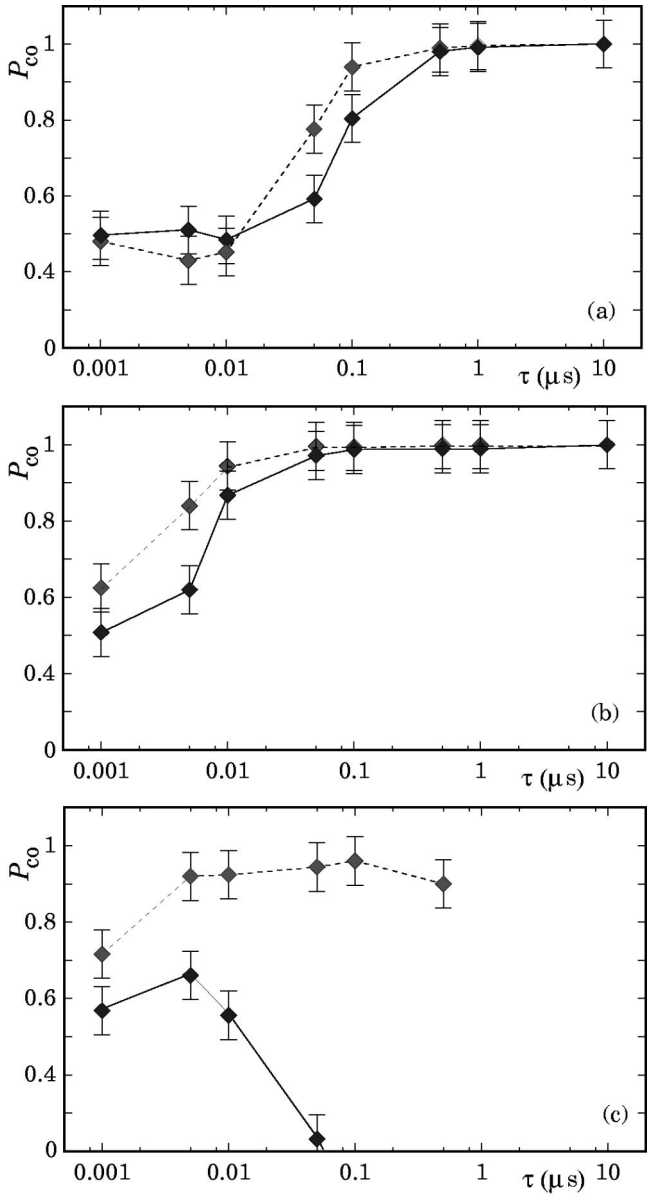


FIG. 13. Probability of correct operation ($P_{CO}$) for the second and the last cell in the clocked chain of Fig. 4 as a function of the clock period. The solid curves refer to the last cell, while the dashed ones refer to the second cell. We have considered three different temperatures: $T=1$ K (a), $T=2.5$ K (b) and $T=4.2$ K (c). The capacitor values are: $C=5.3$ aF, $C_1=1.2$ aF, $C_2=1.2$ aF, $C_3=3.57$ aF, $C_4=1.48$ aF, $C_c=1$ aF. The resistance of the tunneling junctions between the dots is $R=200$ kΩ, while the junctions which connect the dots to the ground have a resistance of $10^{10}$ Ω.

actly in the middle between those of the outer dots. Thus, we have a voltage of 1.5 mV across the 200 kΩ tunneling resistor, which leads to a current of 7.5 nA. This corresponds to an electron flux of $46.82\times10^{9}$ electrons/s. Therefore, an estimate for the average time an electron takes to move from the central dot to the expected outer dot (i.e., to the more positively biased dot) is $21.36\times10^{-12}$ s. Furthermore, intercell coupling has been chosen five times smaller than intracell coupling, in order to achieve proper operation of the cell chain, thus, the relevant average time between tunneling events triggered by the polarization state of a nearby cell is around $107\times10^{-12}$ s.

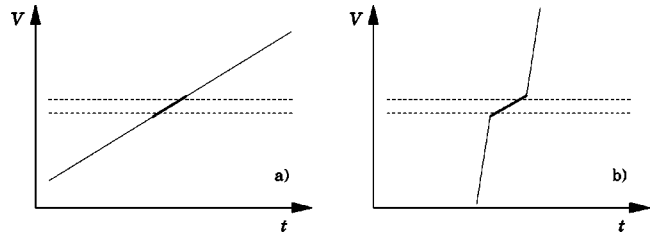


FIG. 14. Potential of the central dot vs time with the clock ramp used for the simulations, (a), and potential of the central dot vs time with a clock ramp modified to achieve a minimum clock period (b). The dashed lines represent the potential of the two outer dots and the thicker segment identifies the active region.

In order to be reasonably sure that an electron will actually tunnel out of the central dot into the expected dot, the active portion of the clock ramp must be at least ten times longer than the average time between tunneling events, therefore $1.07\times10^{-9}$ s. Assuming linear clock ramps with constant slope and recalling that the voltage excursion must be at least ten times the amplitude of the active interval (to guarantee that the lock condition will actually take place), the minimum duration of each ramp is $10.7\times10^{-9}$ s. Finally, since a clock period has a duration corresponding to that of four ramps, the expected clock period is $42.8\times10^{-9}$ s, which is of the same order of magnitude as the results from our Monte Carlo simulation. With an accurate optimization of all parameters it would be possible to achieve some improvement over these figures, but not orders of magnitude. For example, one of the best possible improvements would consist in reducing the clock period by almost a factor of 10, by designing a clock waveform that is linear or constant during the active time and then rapidly switches to the lock condition, as in Fig. 14(b). However, it would be difficult to guarantee the distribution of such a waveform to all cells without significant alterations, and the rate of change of the clock signal would in any case be limited by the adiabatic requirement.[9]

## VI. SIMULATION OF MAJORITY VOTING GATE

In the previous section, we studied a simple QCA wire, which can be considered the basic element of QCA logic. A further step consists in investigating a more complex circuit such as the majority voting gate depicted in Fig. 5 and its clocked counterpart.

This circuit is expected to provide as an output ($O$) the logical state which is present at the majority of the three input cells ($A$, $B$, and $C$). As in the previous section, we first discuss the results of the simulation of a nonclocked circuit (Fig. 5). The simulation has been performed starting from a minimum energy configuration with all the cells in the same polarization state. Then the input cell $A$ has been switched via a proper bias variation, while $B$ and $C$ have been kept in the logical state 1. The propagation of the change in polarization has been followed until the new ground state is reached, and $\langle t_{rel}\rangle$ has been obtained by averaging over several realizations.

From a practical point of view, the correct output is reached when the change in polarization of cell $A$ is correctly

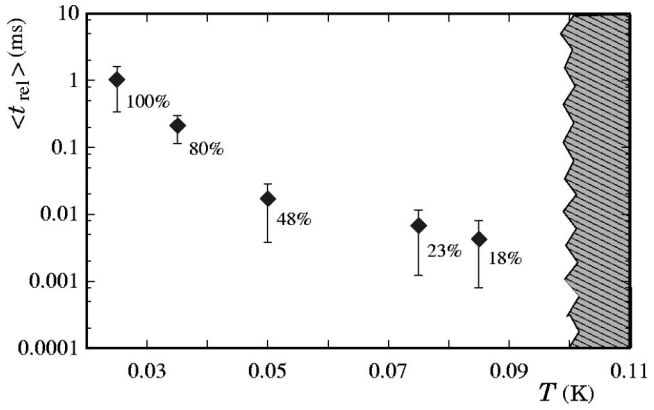


FIG. 15. Average relaxation time $\langle t_{rel} \rangle$ as a function of temperature for the operation of a nonclocked majority voting gate. In the dashed region, the operation is completely disrupted due to thermal fluctuations. The values of the parameters are: $C_o = 400$ aF, $C_v = 288$ aF, $C_c = 88$ aF, $C^* = 1$ aF, and $R_T = 200$ kΩ.

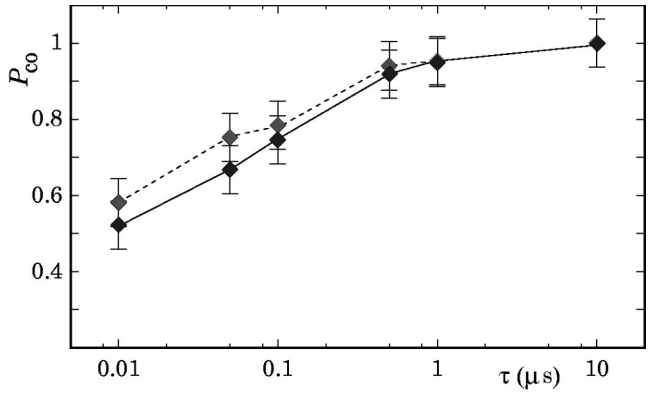


FIG. 16. Probability of correct operation ($P_{CO}$) for the output cell in a clocked majority voting gate as a function of clock period. We studied two different temperatures: $T = 1$ K (dashed line) and $T = 2.5$ K (solid line). The capacitor values are: $C = 5.3$ aF, $C_1 = 1.2$ aF, $C_2 = 1.2$ aF, $C_3 = 3.57$ aF, $C_4 = 1.48$ aF, $C_c = 1$ aF. The resistance of the tunneling junctions between the dots is $R = 200$ kΩ, while the junctions which connect the dots to the ground have a resistance of $10^{10}$ Ω.

propagated along the horizontal arm of the circuit. Cells in the vertical arms are not supposed to change polarization. However, we observed that, increasing the temperature, correct propagation along the horizontal arm was sometimes associated with incorrect polarization states appearing in the vertical arms. This means that the system was not in the correct final ground state, which would be reached in a longer time, but still in a state with the correct value at the output. We decided to compute $\langle t_{rel} \rangle$ based on just the output value, because this is probably closer to what could be done in a real experiment, but we also evaluated the occurrence of the configuration corresponding to the actual ground state, and indicated its relative frequency in the figure, with the numbers next to each data point (see Fig. 15).

By comparison, with the single chain dynamics (Fig. 7), we notice that the relaxation times, at least for low-temperature values, are shorter, as expected. Indeed, the distance between the input cell *A* and the output cell *O* is in this case shorter than in the previously studied chain. However, due to the greater circuit complexity, we have a larger number of states which are very close in energy and thus a larger error probability. This is reflected both in the increase of relaxation time at higher temperature and in the fast relative increase of the results with correct output but nonrelaxed vertical arms, as shown by the percentages indicated in the figure.

The simulation of the nonclocked majority voting gate has been also performed for the other parameter set (see second line of Table II), obtaining coherent results, which we do not show here because they are not of particular significance.

Let us now consider the simulation of a clocked majority voting gate. We adopt the same simulation strategy as in the case of the clocked chain: we monitor the output cell *O* by averaging its value over the proper portion of the clock period. If we repeat this simulation for various temperature values and clock periods, we obtain the probability of correct operation as for the case of the linear chain: results are shown in Fig. 16. If we compare Fig. 16 with Fig. 13, we notice a less pronounced dependence of $P_{CO}$ on temperature, but also an overall increased error probability, which represents a further limitation to the maximum operating speed, when a nontrivial circuit with a parameter choice reflecting a realistic QCA implementation is considered.

## VII. CONCLUSIONS

The comparison between nonclocked and clocked QCA architectures shows that the latter is better suited for computational purposes. In the nonclocked case, the relaxation to the ground state is a statistical process with a broad time distribution: we have found long tails in the relaxation time distribution, which reveal the existence of metastable intermediate states. The importance of metastable states is expected to increase once circuit complexity is increased, thus preventing operation of complex circuits at a reasonable speed.

The clocked architecture allows one to overcome these problems and to achieve much faster and more reliable operation, in addition to an improved control over the data flow. In the clocked case, the main constraint to be taken into consideration is the limitation on clock rate and thus on circuit speed, due to the finite tunneling rate between the dots which make up the device. We have shown that for a reasonable (although not yet approachable with present tecnologies) device geometry, it is possibile to operate a QCA chain and a majority voting gate at a clock period of a few microseconds and at a temperature of a few kelvins. We have also pointed out the reasons why a simple estimation of the switching speed based on *RC* time constants would yield results for the minimum achievable clock period that are much shorter than the actual values obtained from our Monte Carlo simulation.

Overall, the clocked QCA architecture appears more promising than that based on ground-state relaxation, but we wish to point out that the positive characteristics of the clocked architecture must be weighed against the much

greater complexity of the associated circuits, whose implementation is currently beyond available fabrication capabilities.

## ACKNOWLEDGMENTS

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