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Abstract. We present a Monte Carlo simulation of two implementations of Quantum Cellular Automaton (QCA) circuits: one based on simple ground state relaxation and the other on the clocked cell scheme that has recently been proposed by Tóth and Lent. We focus on the time-dependent behavior of two basic circuits, a binary wire and a majority voting gate, and assess their maximum operating speed and temperature requirements for different sets of fabrication parameters.

Keywords: QCA circuits, nanoelectronics ,Coulomb Blockade

1. Introduction

Quantum Cellular Automata (QCA) represent an original approach, first proposed by Lent *et al*. (1993), to the implementation of logic circuits, exploiting the bistable properties of a cell made up of 4 quantum dots or nodes and containing 2 excess electrons. The initial proposal of QCA circuits was based on two-dimensional arrays of such cells and on letting the system relax down to the ground state, so that the result of the computation was obtained as the state of a group of cells located along the boundary of the array. However, if ground state computation is performed with relatively large QCA arrays, the evolution of the system can get temporarily stuck in a metastable state and reach the ground state (and thus the correct logical output) only after an extremely long time (Landauer 1994). To avoid this problem, an adiabatic logic scheme has been proposed, in which the evolution of the system is driven by a multi-phase clock (Lent and Tougaw 1997). This scheme involves modulation of the interdot barriers, in order to keep each cell always in its instantaneous ground state and to lock it, i.e. freeze its state, before it is used to drive a neighboring cell.

An interesting approach to the modulation of the inter-dot barriers in a metal-dot QCA implementation has been proposed in Tóth and Lent (1999): it consists in implementing the barrier with two additional dots, whose potential can be varied by means of an external voltage.

Metastable states are no longer a problem for adiabatic logic, but we need to consider that signal propagation is limited by the switching time of single cells. In particular, proper operation can be obtained only if tunneling transition rates are large enough to allow electrons to actually tunnel into the expected dot during the active state of the cell. In Bonci, Iannaccone and Macucci (2001) we evaluated the switching time by computing the electron tunneling rates as a function of material parameters and cell geometry. Here we use such results to test the operation of circuits made up of non-clocked and clocked cells via a Monte Carlo simulation and we compare the achievable performance.

2. QCA Circuit Simulator

The numerical simulation has been performed by means of a Monte Carlo code that we have developed, based on the orthodox Coulomb Blockade theory and specifically suited to handle circuits containing clocked single-electron devices (Macucci, Gattobigio and Iannaccone to appear). Our software allows simulating circuits with voltage sources that have an arbitrary piecewise linear time dependence.

In addition, since cotunneling plays an important role in some regimes of operation of QCA circuits, it has been taken into consideration, although approximately, on the basis of the formulation in Fonseca *et al*. (1995).

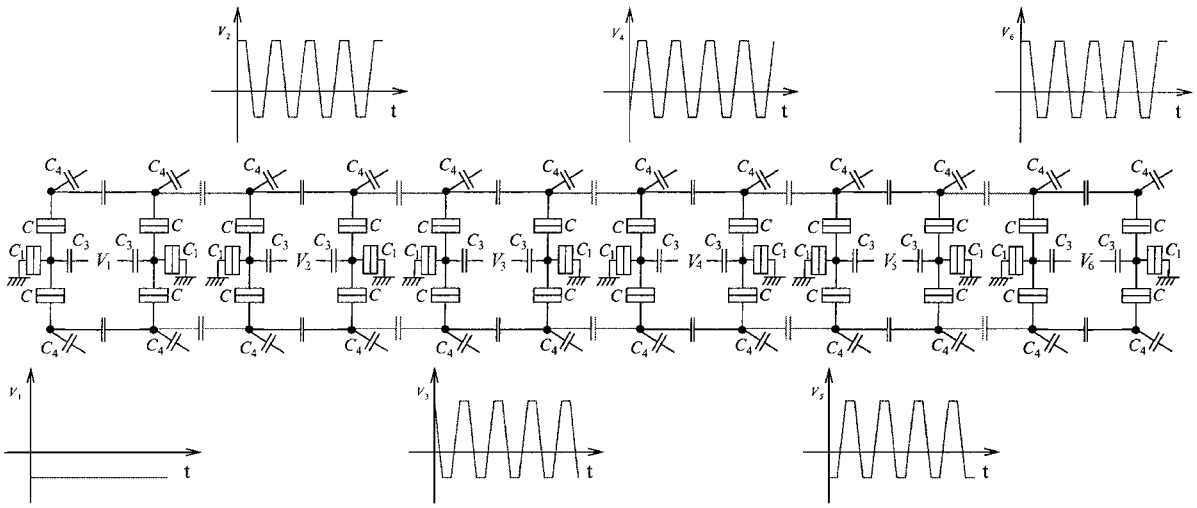

Figure 1. Chain made up of six clocked cells.

We study two different circuits: a linear chain made up of six QCA cells and a majority voting gate made up of eight QCA cells, both of them in the clocked and non-clocked version. The clocked chain, relaying on relaxation down to the ground state, is shown in Fig. 1. The non-clocked versions are much simpler: each cell is made up of a square whose sides are represented by four tunneling capacitors (C_O for the horizontal sides and C_V for the vertical sides), neighboring cells are connected via ideal capacitors C_C and the state of the first cell is enforced via C^* capacitors connected to the two outer nodes of the input cells (Bonci, Iannaccone and Macucci to be published).

In the two cases we use a different simulation strategy, due to the different principle of operation. In the non-clocked case we are strictly following the ground-state calculation paradigm: to obtain the logical output of the circuit we need to wait until the system has relaxed to the ground state. By repeating several times the simulation, we are able to verify circuit reliability (i.e. whether or not the correct logical output is achieved after a given time) and to compute the average time the circuit needs to reach the correct logical output.

In the clocked case the switching time is imposed from the outside. In order to verify circuit operation we follow the time evolution of each single cell and verify whether it is in the expected logical state during the proper time intervals. We do not need to perform an ensemble average in this case, because statistics are obtained over a large enough number of clock cycles.

We have performed calculations for two sets of system parameters. The first set has been derived from the recent experiments which have successfully demonstrated operation of simple QCA gates (Orlov *et al.* 1999, Amlani *et al.* 1999, 2000). The second one was obtained from our previous work, in which we discussed the limits of clocked QCA devices (Bonci, Iannaccone and Macucci 2001) from a theoretical point of view. The experimental and the theoretical choices of parameters are shown in the Tables 1 and 2, where, for the clocked case, C_C represents the coupling capacitor between neighboring cells. The theoretical set represents a compromise between miniaturization, efficiency and technical feasibility, at least in perspective, since fabrication of the corresponding extremely small and precise structures is not yet achievable with current technology.

Table 1. Circuit parameters for the non-clocked case.

	C_o	C_v	C_c	C^*	R_T
Experimental parameters (Orlov *et al.* 1999, Amlani *et al.* 1999, 2000, Orlov *et al.* 2000)	400 aF	288 aF	88 aF	1 aF	200 kΩ
Theoretical parameters (Bonci, Iannaccone and Macucci 2001)	5.3 aF	5.3 aF	2 aF	0.1 aF	200 kΩ

Table 2. Circuit parameters for the clocked case.

	C	C_1	C_2	C_3	C_4	C_c	R_T
Performed experiments (Orlov *et al*. 1999, Amlani *et al*. 1999, 2000, Orlov *et al*. 2000)	420 aF	300 aF	25 aF	80 aF	200 aF	50 aF	200 kΩ
Theoretical prediction (Bonci, Iannaccone and Macucci 2001)	5.3 aF	1.2 aF	1.2 aF	3.57 aF	1.48 aF	1 aF	200 kΩ

3. Binary Wire Simulations

We start by simulating a binary wire based on the experimental parameters. In the non-clocked case the relaxation time to the ground state is a statistical quantity whose average value $\langle t_{rel} \rangle$ is shown in Fig. 2, as a function of temperature. We notice that $\langle t_{rel} \rangle$ decreases as temperature increases. This is due to the increased tunneling rate, which helps driving the evolution of the system out of metastable states, but this phenomenon is limited by the fact that beyond a certain temperature fluctuations prevents the binary wire from reaching a stable ground state at all.

Knowledge of the average quantity $\langle t_{rel} \rangle$ is not sufficient to assess the speed of the circuit. We need to take into consideration the distribution of relaxation times, which is quite broad and exhibits long tails: this implies that $\langle t_{rel} \rangle$ is actually too conservative an estimate. We notice also that, as temperature decreases, the importance of cotunneling events increases.

The situation is similar if we choose the other parameter set, which we have defined as "theoretical". The overall behavior is comparable with the previous parameter choice, with the only significant difference consisting in the possibility to achieve a higher operating temperature.

Let us now consider the clocked architecture of Fig. 1: by means of an external clock signal, we enforce a well defined switching time, which is not dependent on the relaxation to the ground state any more. In this case we need to assess whether the system is fast enough to follow the clock and thereby to provide the correct final output. The error probability depends both on the clock rate and on the operating temperature. With too fast a clock the cell is not able to switch properly, and the same may happen for too large values of the temperature.

We performed runs over several (250) clock cycles and we checked the logical state of the second and of the sixth (last) cell of the chain. In this way, we were able to compute the percentage of correct output P_{co} over the total number of clock cycles. With this prescription, we obtained the result shown in Fig. 3. The deterioration of the circuit evolution with increasing clock frequency is clear; moreover P_{co} decreases as we move along the chain, due to the fact that the error probability increases as the number of cells that have processed the information increases.

We repeated the simulation with the theoretical parameter set obtaining the results shown in Fig. 4. Similar comments apply to these results, although

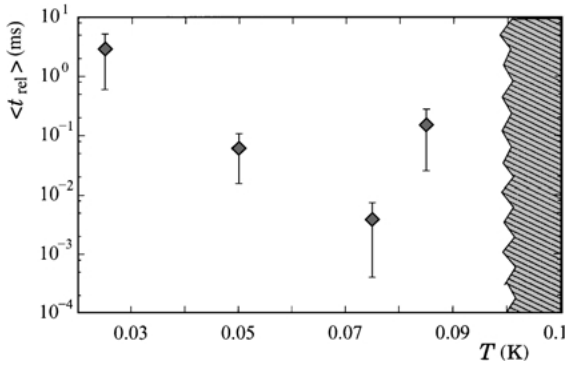

Figure 2. Average relaxation time $\langle t_{rel} \rangle$ as a function of temperature. In the dashed region the operation is completely disrupted due to thermal fluctuations. The values of cell parameters are shown in the first row of Table 1.

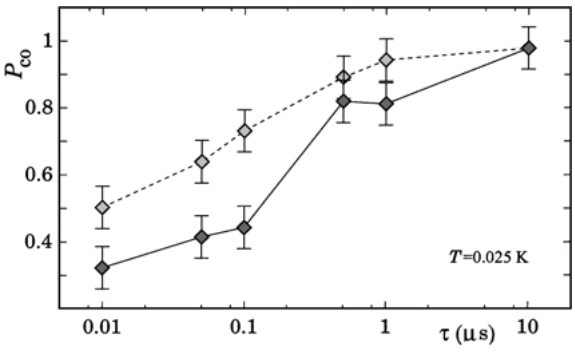

Figure 3. Probability of correct operation (P_{co}) for the second and the last cell in the clocked chain of Fig. 1 as a function of the clock period. The solid curve refers to the last cell while the dashed one refers to the second cell. The values of cell parameters are shown in the first row of Table 2.

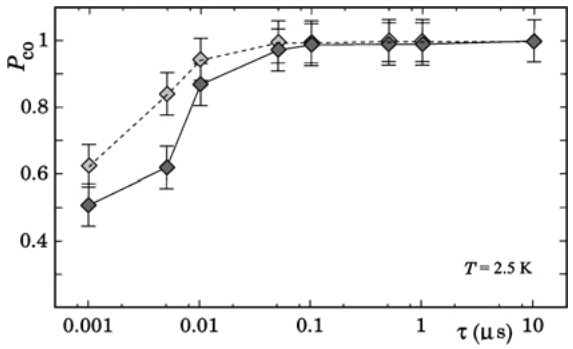

Figure 4. Probability of correct operation (P_{co}) for the second and the last cell in the clocked chain of Fig. 1 as a function of clock period. The solid curve refers to the last cell while the dashed one refers to the second cell. The values of cell parameters are shown in the second row of Table 2.

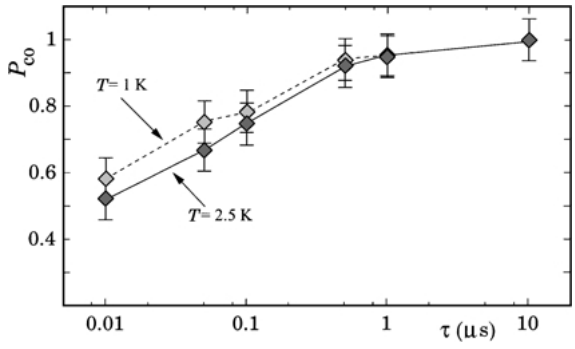

Figure 5. Probability of correct operation (P_{co}) for the output cell in a clocked majority voting gate as a function of clock period. We studied two different temperatures: $T = 1$ K (dashed line) and $T = 2.5$ K (solid line). The values of cell parameters are shown in the second row of Table 2.

the temperature range is different (we moved up two orders of magnitude). In this case we can find a region of correct operation extending down to a clock period of 5×10^{-8} s and to a temperature of 2.5 K. This could be an acceptable operating condition, at least for some niche application. This result is worth of discussion. A rough dimensional analysis, based on the $R_T C^{-1}$ time constant, would give a tipical switching time of 10^{-12} s, much shorter than the one obtained by means of numerical simulation. There are indeed several phenomena that degrade circuit operation. The actual probability for an electron located in the central dot of a cell to switch to a side dot can be obtained by considering the difference between the voltage drops on the upper and lower tunneling junctions. With our choice of parameters the voltage difference due to another electron located in the other half of the same cell is 3 mV and corresponds to a current of 2.5×10^{11} electrons per second, i.e., to a switching time 4 times larger than the previous estimate. This is true for intracell switching, but we need to consider switching due to the influence of a neighbor cell. The voltage unbalance in this case is typically 5 times smaller and thus the switching time has to be increased by the same factor. A further multiplying factor comes out from the clock time pattern. In order to inhibit unwanted transitions, the locked and null state need to have a energy difference with respect to the active state much larger than $K_B T$, therefore the active region represents only one tenth of the rising segment of the control voltage. Moreover, this segment represents 1/4th of the clock pattern and thus the active region is restricted to a time interval which is 40 times smaller than the clock period. Finally, we need to consider that a clock rate in a logical circuit can be considered safe if it is at least ten times smaller than the maximum theoretical rate.

The overall multiplying factor stemming from these considerations approaches 10^4, bringing us very close to the numerical results.

4. Simulation of a Majority Voting Gate

In the previous section we studied a simple QCA wire, the basic element of QCA logic. A further step consists in considering a circuit that performs a slightly more complex logical operation, such as a majority voting gate. This circuit is expected to provide at the output the logical state which is present at the majority of the inputs. We start with the simulation of a non-clocked circuit, computing $\langle t_{rel} \rangle$ as the average over several realizations. We find results similar to those for the binary wire, with an increase of the average relaxation time, as should be expected as a consequence of the greater circuit complexity.

Finally, we study a clocked majority voting gate and report the results in Fig. 5, for the theoretical choice of parameters. If we compare Fig. 5 with Fig. 4 we notice, as in the case of the non-clocked version, an overall increased error probability, which further limits the maximum operating speed.

5. Conclusions

We have investigated the time-dependent behavior of clocked and non-clocked QCA circuits, obtaining results for the maximum operating speed and operating temperature for two choices of parameters. In the

non-clocked circuits, relaxation to the ground state is a statistical process with a broad distribution characterized by long tails. Even with the theoretical set of parameters, which corresponds to a conceivable, although not yet feasible, implementation of QCA cells, the maximum speed that can be achieved is unsatisfactory, on the one side because of the action of intermediate metastable states into which the evolution of the system gets trapped at low temperature and, on the other side, because of the disrupting action of thermal fluctuations at higher temperatures.

The clocked architecture allows to overcome the problem of metastable states and to achieve much faster operation, with improved control of data flow. We have shown that, with a very optimistic choice of parameters, it is possible to achieve clock frequencies and operating temperatures that can be acceptable for some niche application in which the other advantages of QCA systems may play a role. The layout complexity is, however, very significantly increased moving to the clocked architecture, due mainly to the need for clock distribution lines, which makes practical implementation very challenging.

Acknowledgments

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References

Amlani I., Orlov A.O., Kummaruku R.K., Bernstein G.H., Lent C.S., and Snider G.L. 2000. Appl. Phys. Lett. 77: 738.

Amlani I., Orlov A.O., Toth G., Bernstein G.H., Lent C.S., and Snider G.L. 1999. Science 284: 289.

Bonci L., Iannaccone G., and Macucci M. 2001. J. Appl. Phys. 89: 6435.

Bonci L., Gattobigio M., Iannaccone G., and Macucci M. Simulation of the time evolution of clocked and nonclocked Quantum Cellular Automaton (QCA) circuits. J. Appl. Phys. (to be published).

Fonseca L.R.C., Korotov A.N., Likharev K.K., and Odinstov A.A. 1995. J. Appl. Phys. 78: 3238.

Landauer R. 1994. In: Welland M.E. (Ed.), Ultimate Limits of Fabrication and Measurement. Kluwer, Dordrecht.

Lent C.S. and Tougaw P.D. 1997. Proc. IEEE 85: 541.

Lent C.S., Tougaw P.D., and Porod W. 1993. Appl. Phys. Lett. 62: 714.

Macucci M., Gattobigio M., and Iannaccone G. 2001. J. Appl. Phys. 90: 6428.

Orlov A.O., Amlani I., Kummamuru R.K., Ramasubramanian R., Toth G., Lent C.S., Bernstein G.H., and Snider G.L. 2000. Appl. Phys. Lett. 77: 295.

Orlov A.O., Amlani I., Toth G., Lent C.S., Bernstein G.H., and Snider G.L. 1999. Appl. Phys. Lett. 74: 2875.

Tóth G. and Lent C.S. 1999. J. Appl. Phys. 85: 2977.

Ungarelli C., Francaviglia S., Macucci M., and Iannaccone G. 2000. J. Appl. Phys. 87: 7320.