Four-phase power clock generator for adiabatic logic circuits

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A. Bargagli-Stoffi, G. Iannaccone, S. Di Pascoli, E. Amirante, D. Schmitt-Landsiedel, *Four-phase power clock generator for adiabatic logic circuits*, Electronics Letters, **38**, pp.689-690 (2002).

left-most cells and a_{out}s in the right-most cells of the array multiplier. The second equality checker is responded for comparing b_{in}s in the upper-most cells and b_{out}s in the lower-most cells of the array multiplier. The last equality checker is responded for comparing the results C_4–C_0 obtained at the first time and those at the second time. Only one extra clock cycle is added for the concurrent error detection capability.

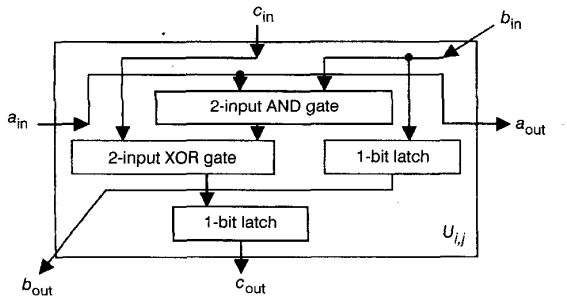

Fig. 2 *Detailed circuit of cell $U_{i,j}$ in Fig. 1*

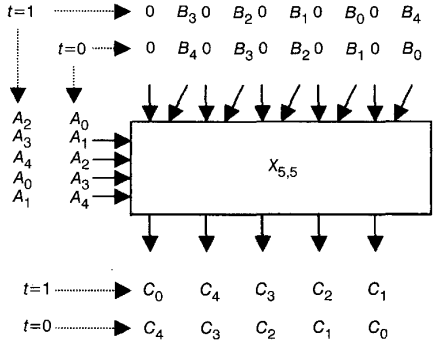

Fig. 3 *Concurrent error detection in array multiplier in Fig. 1*

A fault tolerant scheme based on the RESO method is shown in Fig. 4. The three results are voted to give the correct result. Only two extra clock cycles are required for the fault tolerant capability.

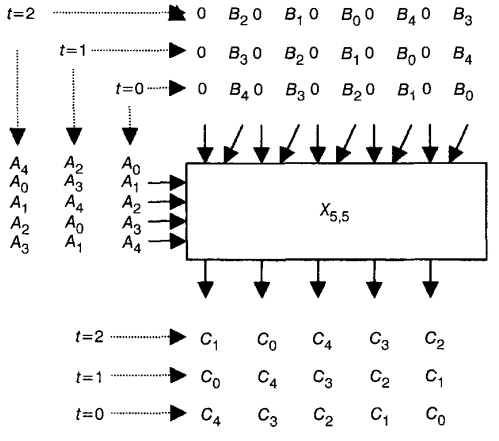

Fig. 4 *Fault tolerance in array multiplier in Fig. 1*

Conclusions: A modified version of Lee–Lu–Lee's multipliers has been presented. The concurrent error detection capability in this modified array multiplier has been described and only one clock cycle is added. The fault tolerant capability has also been described and only two extra clock cycles are required. Both permanent and transient faults can be detected.

6 November 2001
Electronics Letters Online No: 20020468
DOI: 10.1049/el:20020468

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Four-phase power clock generator for adiabatic logic circuits

A. Bargagli-Stoffi, G. Iannaccone, S. Di Pascoli, E. Amirante and D. Schmitt-Landsiedel

A circuit for a four-phase trapezoidal power clock generator for adiabatic logic circuits realised with a double-well 0.25 μm CMOS technology and external inductors is proposed. The circuit, at a frequency of 7 MHz which is within the optimum frequency range for adiabatic circuits realised with 0.25 μm CMOS technology, has a conversion efficiency higher than 80%, and is robust with respect to parameter variations.

Introduction: In recent years several low-power logic families based on a multiphase AC power supply (the power clock) have been proposed. During the rise time the clock charges the node capacitances to the voltage required for the operation of the logic circuit, and during the fall time it recovers the energy just stored in the node capacitances. If the rise and fall times of the power clock are much larger than the time constants associated to the capacitances of the circuit, such energy transfers occur almost 'adiabatically', i.e. without energy loss. Most of the proposed logic families require a two-phase or a four-phase clock, which increases the circuit complexity with respect to standard CMOS solutions.

In the literature, adiabatic logic families are usually presented by exemplifying the operating principle with simple logic circuits, and emphasising the energy savings with respect to standard CMOS circuits. Although these studies illustrate important aspects of logic families, they are not comprehensive since usually the energy dissipated in the DC/AC converter that generates the multiphase power supply is not taken in account. Only in a few papers has the converter been considered not ideal, but the designed solutions have low efficiency or generate signals that differ from the optimum waveforms [1–3].

We believe that a key aspect in the evaluation of the potential and the perspectives of adiabatic logic families is the performance of a complete system, including the power clock generator and the interface with 'conventional' logic. With this aim, in this Letter we propose a high efficiency four-phase trapezoidal power supply generator for logic circuits belonging to three different adiabatic families, namely the ECRL [2, 3], PFAL [4, 5], and 2N-2N2P [6, 7].

The main specifications for a DC/AC converter for adiabatic circuits are the capability to recover the energy stored in the load capacitances, and a high power-conversion efficiency defined as the ratio of the load power to the total DC supply power. Oscillators based on LC resonant circuits can meet these requirements and therefore ensure that the complete adiabatic system provides significant power savings with respect to its standard CMOS counterpart. A few schemes have already

appeared in the literature: the 1N or 1N1P single-phase power clock generator [1] can generate a single phase with a conversion efficiency of 70%. The 2N2P two-phase power clock generator [1–3, 8] provides a two-phase sinusoidal clock and requires only one inductor. If control signals are external, the frequency is easily enforced and, with some additional circuitry, two oscillators can be merged into a four-phase generator, with conversion efficiency of 40 to 50%.

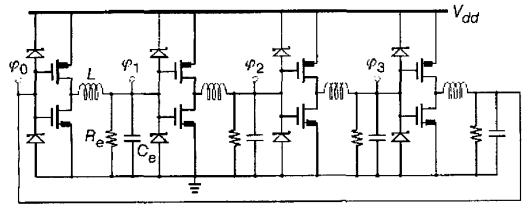

Fig. 1 *Schematic diagram of circuit of four-phase power clock generator*

Phase-shifting oscillator: We propose a four-phase oscillator consisting of a ring of four low-power 90° shifters, as shown in Fig. 1. Each stage is realised with an LC resonant circuit, so that the energy is transferred between the reactive elements while the DC power supply only delivers the energy dissipated on the resistance and on the diodes. Each output of the oscillator drives a stage of the adiabatic circuit, which is represented in Fig. 1 by its equivalent load, a resistance R_e and a capacitance C_e. The inductors L should be external to the chip. The desired phase delay is obtained with a thorough choice of the configuration of reactive elements. Therefore, when the circuit oscillates, the four outputs have the same frequency and a quarter-period shift, as required by the considered adiabatic architectures.

We have considered an implementation based on a standard double-well 0.25 μm CMOS technology, with a DC supply voltage of 1.8 V. For our simulation, R_e and C_e are chosen as the equivalent impedance seen by the power supply of 50 one-bit adders, so R_e is 2 MΩ and C_e is 500 fF. The output amplitude regulation between 0 V and V_{dc} is achieved with Schottky diodes the low V_γ of which ensures low power dissipation when diodes are in the conductive state. Since the considered adiabatic families with 0.25 μm CMOS technology have the optimal frequency between 1 and 10 MHz, we have chosen a clock frequency of 7 MHz, which requires $L = 40$ mH. The ring transfer function is the product of four identical single-stage transfer functions, therefore Barkhausen criteria is met when a single-stage transfer function has gain larger than 1 and a phase delay equal to $(2n+1)\pi/2$, with n integer. The expression of a single-stage transfer function is:

$$\frac{\varphi_1(s)}{\varphi_0(s)} = -\frac{R_e r_{ds}(g_{mp}+g_{mn})}{r_{ds}+R_e+(L+R_e r_{ds}C_e)s+R_e C_e L s^2} \quad (1)$$

where r_{ds} is the small signal output resistance of the MOSFETs, and g_{mp} and g_{mn} are the pMOSFET and nMOSFET transconductances, respectively. By enforcing a phase of $3\pi/2$, we can obtain the following expressions for the frequency and the gain:

$$f_o = \frac{1}{2\pi}\sqrt{\frac{r_{ds}+R_e}{R_e C_e L}}$$
$$\left|\frac{\varphi_1}{\varphi_0}\right| = \frac{R_e r_{ds}(g_{mp}+g_{mn})}{L+R_e r_{ds}C_e}\sqrt{\frac{R_e C_e}{(r_{ds}+R_e)L}} \quad (2)$$

The above results are based on a simplified equivalent circuit. According to our simulations the optimum gain is found between 1.5 and 3.0: for lower values the circuit does not oscillate, while with higher gain the outputs tend to square waveforms and diodes are in the conductive state for a large part of the period, thereby increasing dissipation. To reduce dissipation on the channel resistance, the pMOSFET W/L ratio is ten times larger than that of the nMOSFET. The threshold voltages of the n- and p-MOSFETs are $V_{Tn} = 0.45$ V and $V_{Tp} = -0.42$ V, respectively. Increased efficiency can be obtained with higher threshold voltage devices; for this reason, we have also considered the case of high V_T MOSFETs, with $V_{Tn} = -V_{Tp} = 0.9$ V.

Simulation results: The operation of the circuit has been simulated with PSpice. The oscillator has a conversion efficiency of 85%, with the high V_T MOSFETs, and of 77% with the 'normal' V_T MOSFETs. We have also evaluated the power conversion efficiency when parameter variations occur. With a 30% variation of the value of one capacitance with respect to its nominal value, the reduction of conversion efficiency is less than 1% and the frequency variation is less than 5%. With a 30% variation of the value of a single inductance the reduction of efficiency is 6%, and the frequency variation is 6%.

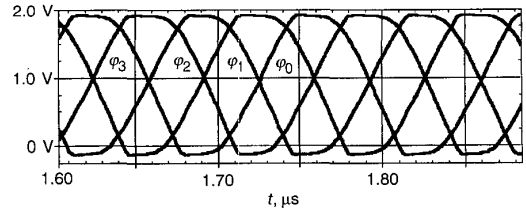

Fig. 2 *Waveforms generated by four-phase clock generator loaded with four-bit adder*

To evaluate the performance of the oscillator as a power supply of a real adiabatic circuit, we have simulated a system consisting of our power clock generator and a four-bit ripple carry adder realised with ECRL logic. The four-phase trapezoidal power clock waveforms are shown in Fig. 2. The conversion efficiency maintains its average value of around 82% with the high V_T devices and of 75% with the 'normal' V_T devices.

Conclusion: We have presented an oscillator that generates the four-phase trapezoidal power clock for three adiabatic logic families proposed in the literature. We have shown that the proposed circuit can reach a power conversion efficiency higher than 80%, with almost trapezoidal waveforms, is robust to load and parameter variations and does not require complex control circuits.

Acknowledgment: This work was supported by the German Research Foundation (DFG) under grant SCHM 1478/1-1 and SCHM 1478/1-2.

14 March 2002
Electronics Letters Online No: 20020523
DOI: 10.1049/el:20020523

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