Four-phase power clock generator for adiabatic logic circuits

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left-most cells and $a_{\text{out}}$ in the right-most cells of the array multiplier. The second equality checker is responsible for comparing $b_{\text{out}}$ in the upper-most cells and $b_{\text{out}}$ in the lower-most cells of the array multiplier. The last equality checker is responded for comparing the results $C_4-C_0$ obtained at the first time and those at the second time. Only one extra clock cycle is added for the concurrent error detection capability.

![Detailed circuit of cell $U_{ij}$ in Fig. 1](image)

**Fig. 2** Detailed circuit of cell $U_{ij}$ in Fig. 1

![Concurrent error detection in array multiplier in Fig. 1](image)

**Fig. 3** Concurrent error detection in array multiplier in Fig. 1

A fault tolerant scheme based on the RESO method is shown in Fig. 4. The three results are voted to give the correct result. Only two extra clock cycles are required for the fault tolerant capability.

![Fault tolerance in array multiplier in Fig. 1](image)

**Fig. 4** Fault tolerance in array multiplier in Fig. 1

Conclusions: A modified version of Lee–Lu–Lee’s multipliers has been presented. The concurrent error detection capability in this modified array multiplier has been described and only one clock cycle is added. The fault tolerant capability has also been described and only two extra clock cycles are required. Both permanent and transient faults can be detected.
appears in the literature: the 1N or 1N1P single-phase power clock generator [1] can generate a single phase with a conversion efficiency of 70%. The 2N2P two-phase power clock generator [1-3, 8] provides a two-phase sinusoidal clock and requires only one inductor. If control signals are external, the frequency is easily enforced and, with some additional circuitry, two oscillators can be merged into a four-phase generator, with conversion efficiency of 40 to 50%.

Fig. 1 Schematic diagram of circuit of four-phase power clock generator

Phase-shifting oscillator: We propose a four-phase oscillator consisting of a ring of four low-power 90° shifter, as shown in Fig. 1. Each stage is realised with an LC resonant circuit, so that the energy is transferred between the reactive elements while the DC power supply only delivers the energy dissipated on the resistance and on the diodes. Each output of the oscillator drives a stage of the adiabatic circuit, which is represented in Fig. 1 by its equivalent load, a resistance $R_v$ and a capacitance $C_v$. The inductors $L$ should be external to the chip. The desired phase delay is obtained with a thorough choice of the configuration of reactive elements. Therefore, when the circuit oscillates, the four outputs have the same frequency and a quarter-period shift, as required by the considered adiabatic architectures.

We have considered an implementation based on a standard double-well 0.25 μm CMOS technology, with a DC supply voltage of 1.8 V. For our simulation, $R_v$ and $C_v$ are chosen as the equivalent impedance seen by the power supply of 50 one-bit adders, so $R_v$ is 2 MΩ and $C_v$ is 500 fF. The output amplitude regulation between 0 V and $V_{dc}$ is achieved with Schottky diodes the low $V_f$ of which ensures low power dissipation when diodes are in the conductive state. Since the considered adiabatic families with 0.25 μm CMOS technology have the optimal frequency between 1 and 10 MHz, we have chosen a clock frequency of 7 MHz, which requires $L = 40$ nH. The ring transfer function is the product of four identical single-stage transfer functions, therefore Barkhausen criteria is met when a single-stage transfer function has gain larger than 1 and a phase delay equal to $(2n+1)n/2$, with $n$ integer. The expression of a single-stage transfer function is:

$$\frac{q_4(s)}{q_2(s)} = \frac{R_{d}a_{4}(s_{m} + s_{m})}{s_{m} + s_{m} + s_{m} + s_{m}}$$

where $R_{d}$ is the small signal output resistance of the MOSFETs, and $s_{m}$ and $s_{m}$ are the pMOSFET and nMOSFET transconductances, respectively. By enforcing a phase of $\pi/2$, we can obtain the following expressions for the frequency and the gain:

$$f = \frac{1}{2\pi} \sqrt{\frac{R_{d}a_{4}}{RCL}}$$

$$\frac{\psi_{1}}{\psi_{2}} = \frac{R_{d}a_{4}(s_{m} + s_{m})}{s_{m} + s_{m} + s_{m} + s_{m}} \sqrt{\frac{R_{d}a_{4}}{L + R_{d}a_{4}C_{s}}} \frac{R_{d}a_{4}C_{s}}{(R_{d}a_{4} + R_{d})L}$$

The above results are based on a simplified equivalent circuit. According to our simulations the optimum gain is found between 1.5 and 3.0; for lower values the circuit does not oscillate, while with higher gain the outputs tend to square waveforms and diodes are in the conductive state for a large part of the period, thereby increasing dissipation. To reduce dissipation on the channel resistance, the pMOSFET $W/L$ ratio is ten times larger than that of the nMOSFET. The threshold voltages of the n- and p-MOSFETs are $V_{thn} = 0.45$ V and $V_{thp} = -0.42$ V, respectively.

Increased efficiency can be obtained with higher threshold voltage devices; for this reason, we have also considered the case of high $V_f$ MOSFETs, with $V_{th} = -V_{f} = 0.9$ V.

Simulation results: The operation of the circuit has been simulated with PSpice. The oscillator has a conversion efficiency of 85%, with the high $V_f$ MOSFETs, and of 77% with the 'normal' $V_f$ MOSFETs. We have also evaluated the power conversion efficiency when parameter variations occur. With a 30% variation of the value of one capacitance with respect to its nominal value, the reduction of conversion efficiency is less than 1% and the frequency variation is less than 5%. With a 30% variation of the value of a single inductance the reduction of efficiency is 6%, and the frequency variation is 6%.

Fig. 2 Waveforms generated by four-phase clock generator loaded with four-bit adder

To evaluate the performance of the oscillator as a power supply of a real adiabatic circuit, we have simulated a system consisting of our power clock generator and a four-bit ripple carry adder realised with ECRL logic. The four-phase trapezoidal power clock waveforms are shown in Fig. 2. The conversion efficiency maintains its average value of around 82% with the high $V_f$ devices and of 75% with the 'normal' $V_f$ devices.

Conclusion: We have presented an oscillator that generates the four-phase trapezoidal power clock for three adiabatic logic families proposed in the literature. We have shown that the proposed circuit can reach a power conversion efficiency higher than 80%, with almost trapezoidal waveforms, is robust to load and parameter variations and does not require complex control circuits.

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