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Electronic properties of functional nanocrystal layers for non-volatile memory applications

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Electronic properties of functional nanocrystal layers for non-volatile memory applications

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A code has been developed for the simulation of the electronic properties of an array of semiconductor nanocrystals embedded in a thin dielectric layer. Such nanocrystal layers, stacked between the gate and the channel of a field effect transistor, can be effectively used as a storage medium for non-volatile memory applications, with perspectives of improved performance in terms of power consumption, ease of programming, and shorter write–erase times with respect to conventional non-volatile memories. Results are given from a detailed simulation based on the self-consistent solution of the Poisson–Schrödinger equation on a three-dimensional grid, focusing on the charging process and on the effect of charge stored in the nanocrystals at transistor threshold voltage. MST/5218

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Introduction

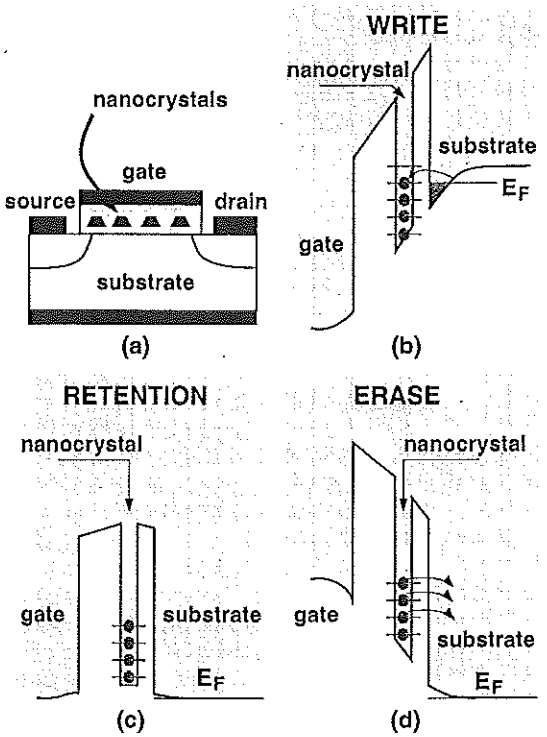
Functional nanocrystal layers for application in non-volatile and quasi-non-volatile memories have been recently proposed[1,2] and extensively studied in industrial and academic laboratories.[3–7] They can be used as a charge storage medium that promises to efficiently replace the polysilicon floating gates used in current EEPROMs (electrically erasable programmable read only memories) and flash memories.

In particular, a few electrons trapped in a nanocrystal layer sandwiched between the gate and the channel of a metal–oxide–semiconductor field effect transistor (MOSFET), as in the example shown in Fig. 1*a*, can increase significantly the MOSFET threshold voltage, and therefore store a bit of information.

The operation of a memory based on nanocrystals in sketched in Fig. 1*b–d*. The memory is programmed by applying to the gate a positive voltage of a few volts, that lowers the dielectric conduction band and enhances tunnelling of electrons from the substrate to the nanocrystals (Fig. 1*b*). Electrons get trapped in the nanocrystal, since further tunnelling to the gate is inhibited by the thick barrier. However, due to already observed Coulomb blockade effects at room temperature,[3] only a well defined number of electrons (depending on the applied gate voltage) can occupy each nanocrystal, so that charging of the nanocrystals is a self-limited process. When one electron is added to each nanocrystal the MOSFET threshold voltage increases in steps, so that both single and multibit storage is possible. The information stored in the memory is then simply read by measuring the saturation current corresponding to a given voltage applied to the gate.

When only reading voltages are applied to the gate, tunnelling barriers are sufficiently opaque to prevent electrons from leaking out and therefore information is retained (Fig. 1*c*). information is erased by applying a negative gate voltage that removes electrons from the traps (Fig. 1*d*). Given the small number of electrons involved in device operation, nanocrystal layers are very promising in terms of reduced power consumption, short program erase times, and limited degradation after many write–erase cycles. Coulomb blockade provides interesting possibilities for multibit storage.

Several materials have been investigated for the nanocrystals and the dielectric layer, as shown in Table 1. At present, silicon rich oxide deposited by LPCVD on SiO_2 (Ref. 4) and implanted Si or Ge in SiO_2 (Ref. 5) are the most promising from the point of view of compatibility with current CMOS technology, retention time, and threshold voltage shift per electron.



1 *a* **sketch of memory obtained with a nanocrystal layer stacked between gate and channel of a MOSFET;** *b* **conduction band profile along** *z* **when positive voltage of a few volts applied to the gate and pictorial view of the write operation;** *c* **conduction band profile along** *z* **during retention of information;** *d* **conduction band profile along** *z* **when negative voltage of a few volts is applied to gate and pictorial view of erase operation**

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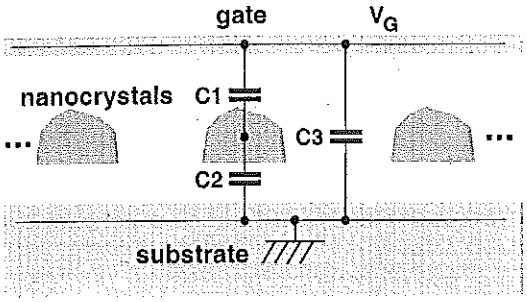


2 **Equivalent capacitance circuit of nanocrystal layer: C_1 is capacitance between nanocrystal and gate, C_2 is capacitance between nanocrystal and channel, C_3 is capacitance between channel and gate divided by number of nanocrystals**

Basic functions of the nanocrystal layer

A simplified quantitative evaluation of the operation of such memories can be carried out by considering the equivalent capacitance circuit of the nanocrystal layer (Fig. 2): each nanocrystal is coupled to the top gate by a capacitance C_1 and to the bottom channel by a capacitance C_2. A capacitance C_3 per each nanocrystal couples the gate and the channel (C_3 is the total direct capacitance between gate and channel divided by the total number of nanocrystals). The channel node is grounded. If an electron charge q is put in the nanocrystal, in order to keep the same charge in the channel node the gate voltage must be increased by a quantity

$$\Delta V_{th} = \frac{q}{C_1 + C_3(C_1 + C_2)/C_2} \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (1)$$

ΔV_{th} represents the threshold voltage shift obtained when one electron is added to each nanocrystal in the layer. As can be seen, in order to increase ΔV_{th}, one must reduce C_1, i.e. reduce the size of the nanocrystal or increase the distance between the dots and the top gate, and reduce C_3, i.e. increase the nanocrystal density.

On the other hand, the additional gate voltage required to win Coulomb repulsion and put one more electron into the dot in a state of increased energy E_0 is

$$\Delta V_G = \frac{q}{C_1} + E_0 \frac{C_1 + C_2}{C_1} \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (2)$$

again, a small value of C_1 and a strong confinement E_0 are required for obtaining a large ΔV_G.

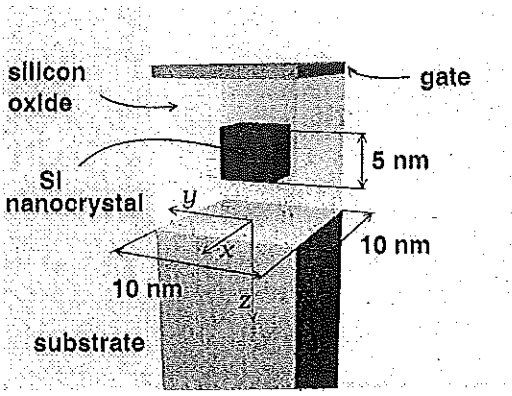
Three-dimensional model

Since the device structure is inherently three-dimensional and electrons in the dot are strongly confined (the nanocrystal diameter is usually in the range 3–10 nm), the

Table 1 List of nanocrystal layers presented in literature with measured V_T per electron and retention time

Dot/insulator material	V_T per electron, V	Retention time	Reference
Si in SiO_2	0·36	NA*	1
InAs/AlGaAs	0·25	1 h at 100 K	6
Si or Ge in SiO_2	0·3	~1 h	5
SiGe/SiO_2	0·4	1 day	7
SRO/SiO_2	~1	NA*	4
Si/Si_3N_4–SiO_2	0·48	~3 h	3

*NA not available.



3 **View of simulation domain: nanocrystal is silicon cube with 5 nm edge, the thicknesses of the top and bottom oxide are 6 and 3 nm, respectively, gate area considered is 10×10 nm^2, corresponding to a nanocrystal density of 10^{12} cm^{-2}**

circuit representation described above is not sufficient for obtaining accurate results. For this reason, a code has been developed for the self-consistent solution of Poisson and Schrödinger equations on a 3D grid, based on density functional theory with local density approximation.[8]

While nanocrystals are of course randomly distributed in the layer, the authors have considered a simplified situation where disorder is removed, that is, nanocrystals occupy a perfect two-dimensional lattice in the dielectric layer. Under this assumption, only the region that represents the elementary cell of the lattice structure is simulated, and then periodic boundary conditions on the potential are applied.

The device structure considered in the numerical simulations is a MOSFET with layer of silicon nanocrystals embedded in SiO_2 stacked between the gate and the channel. The simulation domain in shown in Fig. 3: without losing generality, we assume cubic dots with 5 nm edge and average donor doping of 10^{19} cm^{-3} (here the effect of discrete dopants is not considered). The thicknesses of the top and bottom oxide layer are 6 and 3 nm respectively. the substrate has an acceptor doping of 10^{18} cm^{-3} and the gate is metallic. The surface density of nanocrystals is inversely proportional to the area of the considered domain on the horizontal plane: the area considered is 10×10 nm^2, which corresponds to a nanocrystal density of 10^{12} cm^{-2}.

The potential profile in this domain is determined by the Poisson equation

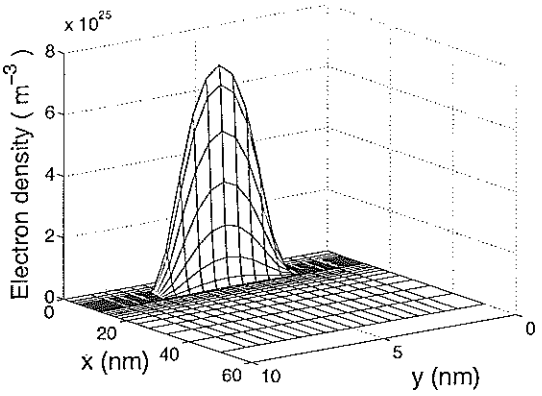
$$\nabla[\varepsilon \nabla \phi(r)] = -\rho(r) = -q[p(r) - n(r) + N_D^+(r) - N_A^-(r)] \quad (3)$$

where ε is the permitivity φ the scalar potential, p and n the hole and electron densities respectively, and N_D and N_A the concentrations of ionised donors and acceptors respectively, that depend on φ as indicated in Ref. 9. While electrons and hole concentrations in the substrate are computed with the semiclassical approximation,[9] electrons in the nanocrystal are strongly confined, and therefore their density is computed by solving the Schrödinger equation using density functional theory for each E_c minimum

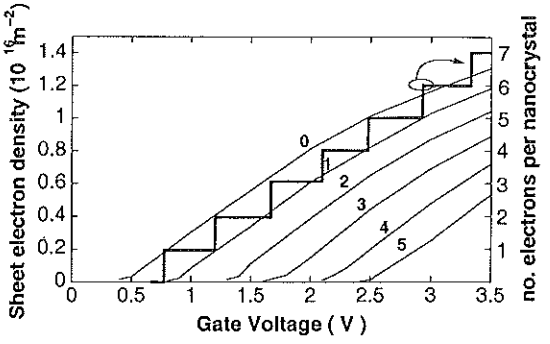
$$-\frac{\hbar^2}{2} \nabla \left(\frac{1}{m} \nabla \Psi \right) + E_c(r)\Psi - V_{xc}(r)\Psi = E\Psi \quad . \quad . \quad . \quad (4)$$

where E_c is the conduction band in the nanocrystal [$E_c = E_c(\varphi = 0) - q\varphi$] and V_{xc} is the exchange-correlation potential in the local density approximation[8]

$$V_{xc}(r) = -\frac{q^2}{4\pi^2 \varepsilon_0 \varepsilon_r} [3\pi^3 n(r)]^{1/3} \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (5)$$



4 Electron density on $x-z$ plane plane for applied gate voltage of 1·2 V and one electron in the dot



5 Sheet electron density in the channel as function of gate voltage for a number of electrons in the nanocrystal ranging from 0 to 5 (left axis): maximum number of electrons allowed in the nanocrystal as function of gate voltage (right axis)

Nanocrystals are randomly oriented, therefore the effective mass tensor for silicon is not used, but only a single effective mass m. Once the eigenfunctions φ_i and the corresponding eigenvalues E_i are obtained, the electron density corresponding to N electrons in the dot can be readily obtained as

$$n(r)=\begin{cases}\sum_{i=1}^{N/2} 2|\Psi_i(r)|^2 & \text{if } N \text{ is even}\\ \sum_{i=1}^{(N-1)/2} 2|\Psi_i(r)|^2+\left|\Psi_{(N+1/2)}(r)\right|^2 & \text{if } N \text{ is odd}\end{cases} \quad (6)$$

since we assume that the electron density in the dot is not appreciably different from that in the ground state.

The Poisson–Schrödinger equation is solved for different N and gate voltages V_G. The maximum number of electrons that can occupy a dot N_{max} is a function of V_G: if $\mu(N,V_G)$ is the chemical potential of the dot with N electrons and applied gate voltage V_G, and E_F is the Fermi energy in the subtrate, N_{max} must satisfy the condition

$$\mu(N_{max},V_G)<E_F \quad \mu(N_{max}+1,V_G)>E_F \quad . \quad . \quad . \quad . \quad (7)$$

The chemical potential is computed with Slater's transition rule as $\mu(N)=E_{N-1/2}$, where $E_{N-1/2}$ is the highest occupied eigenvalue of the system with $N-1/2$ electrons, computed by density functional theory.

By keeping fixed the number of electrons and computing the electron density in the channel as a function of V_G, one can directly obtain the value of the threshold voltage for any number of electrons in the nanocrystal.

Results and discussion

The electron density in the nanocrystal in the $x-z$ plane for an applied voltage of 1·2 V and occupancy of one electron is plotted in Fig. 4. As can be seen, the electron density has the shape of the first eigenfunction, with only one peak at the centre.

In Fig. 5 the sheet electron density in the channel is plotted as a function of the gate voltage V_G for a number of additional electrons in the nanocrystal ranging from 0 to 5 (thin solid lines). From those curves the threshold voltage can be obtained as the intercept on the horizontal axis of the line approximating each curve in the quasi-linear region. As can be seen, the threshold voltage with no electrons in the nanocrystal is $V_{T0}=0·5$ V and increases by approximately 0·4 V per each stored electron.

In the same figure, on the right axis, the maximum allowed number of electrons in the nanocrystal N_{max} is plotted as a function of V_G. Steps are not uniform, and exhibit some shell filling effects, as expected. As can be seen, the gate voltage steps required to add the third and the seventh electron are larger than those corresponding to other electron numbers.

It can be seen from Fig. 5 that several options for write and read voltages are available. For example, one could program the memory to logical 1 by applying a voltage pulse of 2 V, thereby introducing 3 electrons in the nanocrystal and obtaining a threshold voltage $V_{T1}=1·7$ V. Then a voltage $V_{GR}=0·6$ V could be chosen to read the status of the memory, since it satisfies $V_{T0}<V_{GR}<V_{T1}$ and, in addition, it is small enough not to introduce any electron in a memory not programmed.

One very important aspect for the industrial application of non-volatile memories based on nanocrystal layers is the evaluation of write, erase, and retention times. While very promising results have been obtained in experiments[3–7] this issue is beyond the scope of the present paper and will be addressed in the near future.

Acknowledgements

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