Reduction of the energy consumption in adiabatic gates by optimal transistor sizing

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Reduction of the Energy Consumption in Adiabatic Gates by Optimal Transistor Sizing

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Abstract. Positive Feedback Adiabatic Logic (PFAL) with minimal dimensioned transistors can save energy compared to static CMOS up to an operating frequency $f = 200$MHz. In this work the impact of transistor sizing is discussed, and design rules are analytically derived and confirmed by simulations. The increase of the p-channel transistor width can significantly reduce the resistance of the charging path decreasing the energy dissipation of the PFAL inverter by a factor of 2. In more complex gates a further design rule for the sizing of the n-channel transistors is proposed. Simulations of a PFAL 1-bit full adder show that the energy consumption can be reduced by additional 10% and energy savings can be achieved beyond $f = 1$GHz in a 0.13μm CMOS technology. The results are validated through the use of the design centering tool 'WiCkeD' [1].

1 Introduction

In modern technologies with high leakage currents and millions of transistors per chip energy consumption has become a major concern. Static CMOS circuits have a fundamental limit of $E_{charge} = \frac{1}{2}CV_{DD}^2$ for charging a load capacitance C. The typical way to minimize the energy consumption is to lower the power supply V_{DD}. The adiabatic circuits can break this fundamental limit by avoiding voltage steps during the charging and by recovering part of the energy to an oscillating power supply. A comparison among different adiabatic logic families can be found in [2]. Logic families based on cross-coupled transistors like Efficient Charge Recovery Logic (ECRL) [3], 2N-2N2P [4] and Positive Feedback Adiabatic Logic (PFAL) [5] show lower energy consumption than other adiabatic families. The largest energy saving can be achieved with PFAL because the resistance of the charging path is minimized. A standard-cell library for this family was proposed in [6].

In this paper, PFAL is used to determine the dependence of the energy consumption on transistor sizing. After a short description of PFAL, the different

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sources of dissipation in adiabatic logic gates are presented. Considering a simple PFAL inverter, the influence of the transistor dimensions on the energy consumption is derived and a basic design rule for transistor sizing is proposed, which allows to halve the energy consumption compared to previously used minimum sized devices. For more complex gates, this simple rule is validated through the simulation of a 1-bit full adder. To achieve higher operating frequencies, second order effects have to be considered. A further design rule is presented, which allows the 1-bit full adder to save an additional 10% of energy at f = 500MHz. The proposed design rules are validated through the design centering tool 'WiCkeD' [1]. With optimal transistor dimensions operating frequencies higher than f = 1GHz can be achieved.

2 Different Sources of Energy Dissipation

Figure 1a shows the general schematic of a PFAL gate. Two cross coupled inverters build the inner latch and two function blocks F and /F between the supply clock V_{PWR} and the output nodes realize the dual rail encoded logic function. Both logic blocks consist only of n-channel MOSFETs and are driven by the input signals In and /In. Figure 1b shows the timing of a PFAL gate. The input signals are in the hold phase while the gate evaluates the new logic value. During the adiabatic charging of the output load capacitance C the resistance R of the charging path determines the energy dissipation, according to the well-known formula [7] of the adiabatic loss:

$$E_{adiab} = \frac{RC}{T_{charge}} C\hat{V}^2 \,, \tag{1}$$

where $\hat{V}$ is the magnitude of the supply voltage and T_{charge} the charging time.

In a real circuit, leakage currents flow even when the transistors are cut off, providing a second source of energy dissipation:

$$E_{leak} = \hat{V} \cdot I_{off} \cdot T_{hold} \tag{2}$$

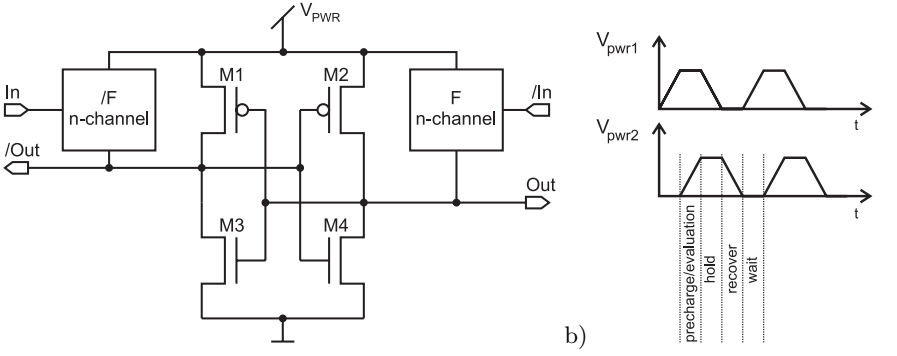

Fig. 1. a) General schematic and b) timing of a PFAL gate. The input signals In and /In are driven by the power supply V_{pwr1} which is a quarter period in advance with respect to V_{pwr2}.

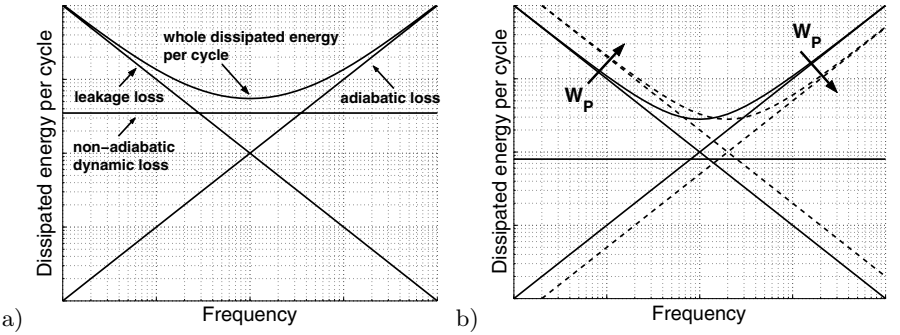

Fig. 2. a) Typical energy dissipation of quasi-adiabatic circuits in former technologies. Beside the leakage loss at low frequencies and the adiabatic loss at high frequencies, the non-adiabatic dynamic losses also affect the energy consumption. b) In modern technologies, the reduced threshold voltage lowers the non-adiabatic losses and therefore only the leakage and the adiabatic losses have to be considered. Both mainly depend on the p-channel transistor width (see figure 1a). The arrows show the expected dependence for increasing width.

where I_{off} is the average off-current and T_{hold} the hold time. In PFAL the hold time $T_{hold} = T_{charge}$. The off-current in static CMOS is comparable to the one in adiabatic logic. However, adiabatic gates dissipate less energy, as the off-current only flows during the hold time, which is typically a quarter period (see figure 7).

Additional energy dissipation is caused by several coupling effects and by partial recovery of energy. During the recovery phase the p-channel transistor cuts off when the power supply falls below the threshold voltage V_{th} and further energy recovery is inhibited. Both effects are referred as non-adiabatic dynamic losses and do not depend on the operating frequency. As the coupling effects are minimized due to the topology of PFAL, the non-adiabatic dissipation mainly depends on the threshold voltage of the p-channel transistor V_{th}:

$$E_{Vth} = \frac{1}{2} C V_{th}^2 \tag{3}$$

Figure 2a shows the different contributions to the energy dissipation versus frequency. At high frequencies, the adiabatic loss is the dominant effect, whereas the leakage current determines the dissipation at low frequencies. The non-adiabatic dynamic losses which are typical for partial energy recovery circuits can be observed at medium frequencies. In former technologies with larger threshold voltages, the minimum energy dissipation is determined by these losses, and a plateau over a certain frequency range can be noticed. On the contrary, in modern technologies like the 0.13μm CMOS technology used in this paper the intercept point of the curves for leakage and adiabatic losses is above the plateau caused by the non-adiabatic dynamic loss (see Figure 2b, solid lines). Therefore in modern technologies with reduced threshold voltage V_{th} the non-adiabatic losses can be neglected, and the curve for the whole energy dissipation shows a minimum for a particular frequency. Although PFAL belongs to the partial

energy recovery families (also known as quasi-adiabatic circuits according to the classification of [8]) its whole dissipation looks similar to the dissipation of fully adiabatic circuits.

In this work, the energy dissipation due to the generation and distribution of the trapezoidal signals was not determined. As it is possible to generate the supply voltage with high efficiency [9], the total dissipation does not significantly increase.

3 Impact of the Transistor Dimensions on the Energy Dissipation

If a high operating frequency is given and load capacitances and supply voltages cannot be changed, a minimization of the energy dissipation can only be achieved by decreasing the resistance R of the charging path. Because in PFAL this resistance mainly consists of the p-channel transistor on-resistance, wider p-channel MOSFET are expected to decrease the energy consumption as shown in figure 2b (dashed line). On the other hand, wider transistors give rise to larger leakage currents. As a result, the whole energy-versus-frequency characteristic is shifted towards higher frequencies without affecting the magnitude of the minimal energy consumption. In logic families using cross-coupled transistors, the resistance of the charging path can be optimized without significantly increasing the load capacitance driven by the former gate. The resistance of the p-channel devices (see figure 3a) mainly determines the charging path resistance in both the evaluation and the recovery phase. In the evaluation phase, the p-channel transistor and the logic block form a kind of transmission gate. Thus, the charging resistance is decreased compared to other families, which only use the p-channel MOSFET for charging the output node such as ECRL. During the recovery phase, the input signals turn off the n-channel MOSFETs MF1 and MF2 in the logic function block. The energy can be recovered through the p-channel device as long as the supply voltage does not fall below the threshold voltage V_{th}. Hence, by properly sizing the p-channel transistors a decrease of the energy dissipation is achieved without increasing the load capacitance seen

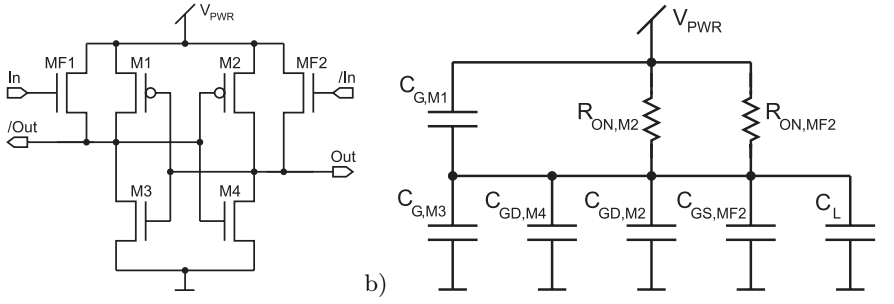

Fig. 3. a) Schematic of a PFAL inverter. b) Equivalent model of a PFAL inverter if the output node Out is charged and discharged.

by the former stage. Through the sizing of the n-channel transistors M3 and M4 no reduction of the energy consumption can be obtained. Therefore, these transistors are kept minimal in order to avoid larger leakage currents.

In the following, the optimal dimension for the p-channel devices is determined. In adiabatic circuits, conducting transistors work in their linear region because voltage steps across the channel of conducting transistors are minimized. For an estimation of the energy consumption during the charging and discharging of the output node Out, the equivalent model shown in figure 3b is taken into account. Beside the external load capacitance C_L the circuit has to drive its intrinsic load, which consists of gate capacitances C_G, gate-source capacitances C_{GS} and gate-drain capacitances C_{GD}. These capacitances are directly proportional to the width of the corresponding transistors. For simplicity the junction capacitances are neglected.

The on-resistance of the p-channel transistor M2 takes over the main part of the charging and the recovery, so that in this approach the n-channel device MF2 is not considered. In the linear region, the on-resistance is equal to:

$$R_{on}(t) = \frac{1}{\mu_P C_{OX} \frac{W}{L} \cdot [V_{GS}(t) - V_{th}]} = \frac{1}{\mu_P C_{OX} \frac{W}{L} \cdot V_{GSt,avg}} \tag{4}$$

where μ_P is the hole mobility, C_{OX} the oxide capacitance per unit area, L the channel length and $V_{GSt,avg}$ the average gate-overdrive voltage. The average gate-overdrive voltage is assumed to be independent of the transistor widths. Using equation 1 the energy consumption of a gate with the p-channel transistor width W_P amounts to:

$$E_{adiab} = \frac{L \cdot (C_{G,M1} + C_{G,M3} + C_{GD,M2} + C_{GD,M4} + C_{GS,MF2} + C_L)^2}{W_P \mu_P C_{OX} V_{GSt,avg}} \cdot \frac{\hat{V}^2}{T} \tag{5}$$

To summarize the capacitances an effective width W_{eff} is introduced. Because in the linear region $C_{GS} \approx C_{GD} \approx \frac{1}{2} C_G$ the channel widths must be weighted:

$$W_{eff} = \frac{3}{2} W_P + \sum_i \sigma_i W_{N,i} \quad \text{, where} \quad \sigma_i = \begin{cases} \frac{1}{2} & \text{for } C_{GS} \text{ and } C_{GD} \\ 1 & \text{for } C_G \end{cases} \tag{6}$$

and W_N is the width of a n-channel transistor. With this effective width equation 5 can be rewritten as:

$$E_{adiab} = \frac{L}{W_P \mu_P C_{OX} V_{GSt,avg}} \cdot (W_{eff} C'_G + C_L)^2 \cdot \frac{\hat{V}^2}{T} \tag{7}$$

where C'_G represents the gate capacitance per unit width.

The minimal energy dissipation E_{adiab} is found for the following p-channel transistor width W_{opt}:

$$W_{opt} = \frac{2}{3} \sum_i \sigma_i W_{N,i} + \frac{2}{3} \cdot \frac{C_L}{C'_G} \tag{8}$$

This procedure can also be performed with other adiabatic families. For 2N-2N2P a similar result was found, while the optimal width for ECRL is different due to the gate topology.

In the following simulations, a load capacitance $C_L = 10\text{fF}$ is used. For the $0.13\mu\text{m}$ CMOS technology according to the above formula the optimal p-channel transistor width W_{opt} is approximately equal to $4.4\mu\text{m}$ using minimal dimensioned n-channel transistors.

4 Simulation Results

The simulations were performed with SPICE parameters of a $0.13\mu\text{m}$ CMOS technology using the BSIM 3V3.2 model. For the nominal load capacitance the typical value in static CMOS $C_L = 10\text{fF}$ was chosen. The oscillating supply voltage has a magnitude of $\hat{V} = 1.5\text{V}$.

4.1 Results for the PFAL Inverter

A series of simulations was performed for the PFAL inverter varying the p-channel transistor width. Figure 4 shows a 3D-plot of the energy consumption per cycle as a function of the operating frequency and the p-channel transistor width W_P. The dark gray layer represents the theoretical minimum for static CMOS, $E = \frac{1}{2}CV_{DD}^2$, where the capacitance $C = 10\text{fF}$ and leakage currents are not taken into account. A minimum of 0.86fJ for the energy consumption of PFAL can be found at $f = 2\text{MHz}$. For the region between $f = 200\text{kHz}$ and $f = 20\text{MHz}$ the energy dissipated per cycle is less than 2fJ. With minimal dimensioned n-channel transistors and with a p-channel width of $2\mu\text{m}$ the energy dissipation is decreased by a factor of 13.1 compared to the theoretical

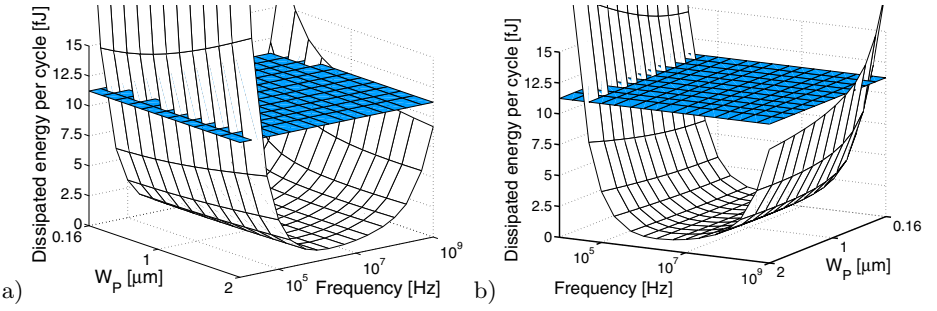

Fig. 4. Energy dissipation versus operating frequency for a PFAL inverter with a load capacitance of 10fF in a $0.13\mu\text{m}$ CMOS technology. Enlarging the p-channel transistor width the energy dissipation is reduced at high frequencies and is increased at low frequencies. The dark gray layer represents the theoretical minimum for static CMOS (11.25fJ) without the effect of leakage currents.

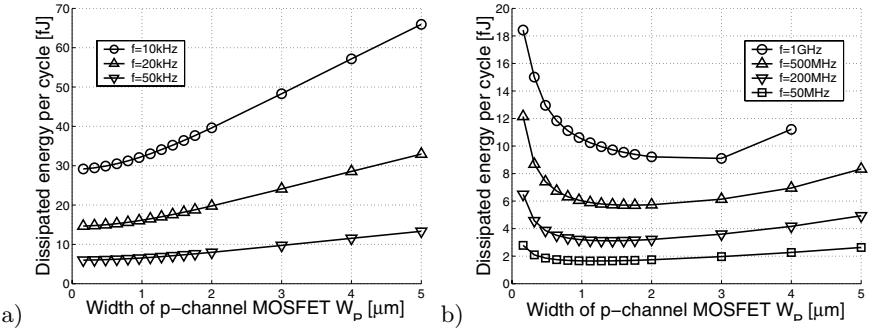

Fig. 5. Energy dissipation versus p-channel MOSFET width for a PFAL inverter in a 0.13μm CMOS technology for different operating frequencies. a) At low frequencies wider p-channel MOSFETs give rise to larger leakage losses. b) At high frequencies a minimum for the energy dissipation between $W_P = 1\mu$m and $W_P = 3\mu$m can be observed. With a p-channel transistor width $W_P = 2\mu$m the energy consumption is reduced by a factor of two.

minimum of static CMOS, which is equal to $E = 11.25$fJ for the used parameters. As expected, at low frequencies the energy consumption increases with increasing p-channel transistor width whereas at high frequencies it decreases. At $f = 1$GHz the dissipation is equal to 18.4fJ with minimal transistors, while with $W_P = 2\mu$m it is reduced to 9.2fJ. Thus, adiabatic circuits consume less energy than the theoretical minimum for static CMOS even at operating frequencies beyond 1GHz.

To determine the minimal energy dissipation in dependence of the transistor width the simulation was extended up to $W_P = 5\mu$m (see figure 5). At low frequencies wider p-channel MOSFETs give rise to larger leakage losses (see figure 5a). At high frequencies a minimum for the energy dissipation between $W_P = 1\mu$m and $W_P = 3\mu$m can be observed as shown in figure 5b. At $f = 1$GHz the gate operates correctly until $W_P = 4\mu$m. With a p-channel transistor width $W_P = 2\mu$m the energy consumption can be reduced by a factor of two in the high frequency range ($f \geq 50$MHz) with respect to the minimal sized implementation. Hence, this is the maximum width used even for the adder presented in the next section.

4.2 Results for a PFAL 1-Bit Full Adder

To investigate the dependence of the energy dissipation on the transistor sizing for more complex gates, a PFAL 1-bit full adder was simulated. The circuit schematic of the sum is shown in figure 6. According to the general schematic (figure 1a) two logic function blocks are implemented using only n-channel transistors. Only two p-channel transistors are needed for the cross-coupled inverters. Above $f = 500$MHz an adder realized with minimal dimensioned transistors dissipates more energy than the equivalent static CMOS implementation (cascaded logic blocks, see [10]). In a first approach, the p-channel transistor width is

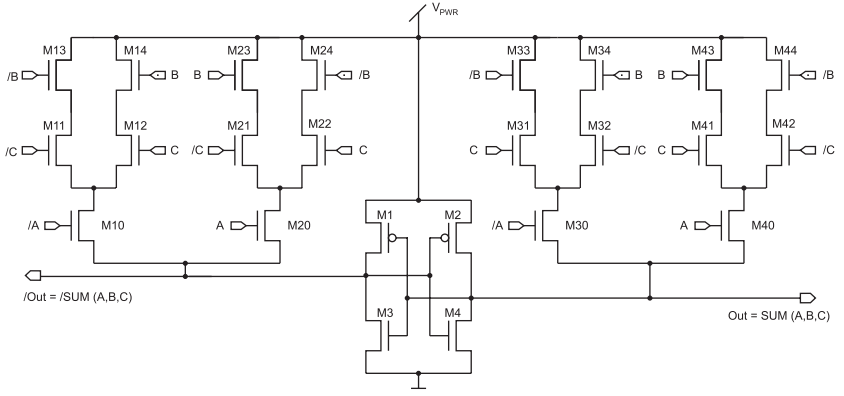

Fig. 6. Schematic of the sum generation circuit in a PFAL 1-bit full adder.

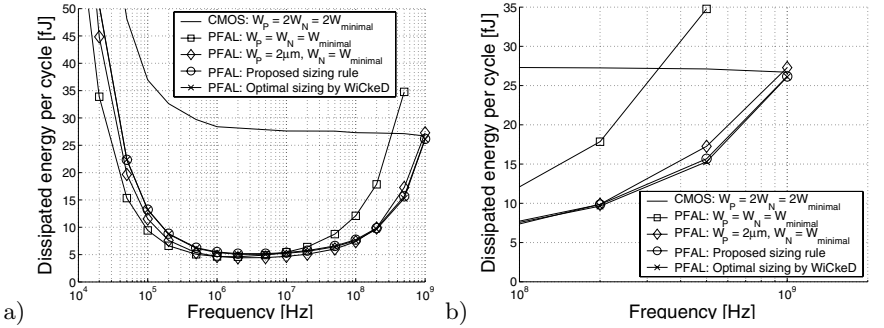

Fig. 7. PFAL 1-bit full adder: Dissipated energy per cycle versus operating frequency for different implementations. a) The whole frequency range is shown. b) Zoom in for f = 100MHz..1GHz.

increased up to $W_P = 2\mu$m while the n-channel transistors are minimal dimensioned. Compared with the realization using only minimal transistor width, the adder with $W_P = 2\mu$m dissipates half of the energy at f = 500MHz (Figure 7, diamonds). Through this additional energy savings the dissipation becomes lower than in the conventional static CMOS implementation. The maximal operating frequency in this case is $f \approx$ 1GHz.

In a further simulation, the optimal transistor dimensions are determined by means of the design centering tool 'WiCkeD' [1] for the frequency f = 200MHz. As expected, the p-channel transistor widths are chosen maximal ($W_P = 2\mu$m). In contrast to the proposed approach, the n-channel devices of the function blocks are not kept minimal. Actually the transistors at the top of the blocks (Figure 6) show the largest average width (see table 1). The transistors in the middle of the function blocks are slightly larger than the ones at the bottom. With this sizing, the RC-delay of the whole function blocks is optimized and the energy dissipation is lowered (Figure 7, cross).

Table 1. Average width of the n-channel transistors in the PFAL gate shown in figure 6 with regard to the position in the function blocks: Optimal values obtained by the design centering tool 'WiCkeD' compared to the values according to the proposed sizing rule, which uses integer multiples of the minimal width.

Position of the n-channel devices in the function blocks	Sizing by WiCkeD	Proposed sizing rule
upper transistors	0.53μm	0.64μm = $4W_{min}$
middle transistors	0.23μm	0.32μm = $2W_{min}$
lower transistors	0.20μm	0.16μm = $1W_{min}$

Regarding layout, it is better to use integer multiples of a standard width to save area and junction capacitances. Therefore, a further sizing rule for the n-channel devices in the function blocks is proposed. The width of the n-channel transistors connected to the output nodes (M10, M20, M30 and M40 in figure 6) are kept minimal ($W_{N,bottom} = W_{min} = 160$nm). The transistors in the middle of the function blocks (M11, M12, M21, M22, M31, M32, M41 and M42) have a width $W_{N,middle} = 2W_{min}$. The transistors at the top of the function blocks (M13, M14, M23, M24, M33, M34, M43 and M44) have $W_{N,top} = 4W_{min}$. For the two p-channel transistors $W_P = 2\mu$m was chosen. The simulation results (Figure 7, circle) show an additional decrease of the energy consumption compared to the proposed basic sizing rule which only considered the p-channel MOSFETs. At $f = 500$MHz the additional reduction of the energy dissipation amounts to 1.6fJ, that is approximately 10%. Compared to optimal sizing obtained by WiCkeD (Figure 7, cross) only a marginal difference is observable at $f = 500$MHz. With this extended sizing rule, energy can be saved with respect to the static CMOS implementation even at $f = 1$GHz.

5 Conclusions

By means of the Positive Feedback Adiabatic Logic (PFAL) it was demonstrated that proper transistor sizing enables adiabatic logic gates to save energy at frequencies beyond 1 GHz in a 0.13μm CMOS technology. Different sources of the energy dissipation in adiabatic circuits were analytically characterized. At high frequencies the energy consumption mainly depends on the resistance of the charging path. Enlarging the width of the p-channel transistors minimizes this resistance without affecting the input capacitances, which represent the load for the former stage. An estimation for the optimal width was presented, which can be used as a starting-point for optimization. Using p-channel transistors with a width $W_P = 2\mu$m, a reduction of the energy dissipation by a factor of 2 was achieved, which enables energy saving even at $f = 1$GHz in simple gates. In more complex gates like a 1-bit full adder, the sizing of the n-channel transistors has to be considered. By means of the design centering tool WiCkeD the optimal sizing for a PFAL 1-bit full adder was determined. In terms of layout a practicable sizing rule was proposed. With this rule the energy dissipation could

be decreased by an additional 10% compared to the circuit with minimal dimensioned n-channel transistors. Compared to the static CMOS implementation the PFAL 1-bit full adder has a gain factor of 3.5 at $f = 100$MHz and operates up to a frequency of $f = 1$GHz with energy savings. This is the highest operating frequency reported for adiabatic logic up to now.

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