QCA cell in silicon-on-insulator technology: theory and experiment

Massimo Macucci
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
M.Gattobigio
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
L.Bonci
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
Giuseppe Iannaccone
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
F. E. Prins
Institut fur Angewandte Physik, Universitat Tubingen
C. Single
Institut fur Angewandte Physik, Universitat Tubingen
G. Wetekam
Institut fur Angewandte Physik, Universitat Tubingen
D. P. Kern
Institut fur Angewandte Physik, Universitat Tubingen

M. Macucci, M. Gattobigio, L. Bonci, G. Iannaccone, F. E. Prins, C. Single, G. Wetekam, D. P. Kern, *QCA cell in silicon-on-insulator technology: theory and experiment*, Superlattices and Microstructures, **34**, pp.205-211 (2004).

ELSEVIER
Superlattices and Microstructures 34 (2003) 205–211
Superlattices and Microstructures
www.elsevier.com/locate/superlattices

A QCA cell in silicon-on-insulator technology: theory and experiment

M. Macucci[a,*], M. Gattobigio[a], L. Bonci[a], G. Iannaccone[a], F.E. Prins[b,1], C. Single[b], G. Wetekam[b], D.P. Kern[b]

[a]*Dipartimento di Ingegneria dell'Informazione, Università degli studi di Pisa, Via Caruso, I-56122 Pisa, Italy*
[b]*Institut für Angewandte Physik, Universität Tübingen, Auf der Morgenstelle 10, D-72076 Tübingen, Germany*

Available online 12 May 2004

Abstract

A prototype cell for the investigation of QCA (quantum cellular automaton) functionality in silicon-on-insulator technology has been fabricated and characterized, observing interaction between the upper and the lower double dots. A simulation code, validated by comparison with the experimental results, has been used to design a modified layout that should allow demonstration of QCA operation at temperatures above 0.3 K.

1. Introduction

The quantum cellular automaton (QCA) paradigm, first proposed by Craig Lent and coworkers in 1993 [1], has received considerable interest in the last decade, due to its potential for the implementation of logic circuits with an architecture that could in principle be scaled down to molecular dimensions. Although large-scale applications of QCA technology seems unlikely, at least in the near future, due to the extreme sensitivity to fabrication tolerances [2] and to the suboptimal behavior from the point of view of the time evolution [3], research on the fundamentals of QCA operation is still of interest, because of potential usage for some niche application and because of the possibility of future implementations with molecules or nanomagnets.

The operation of QCA circuits has been demonstrated with metal tunnel junctions by the Notre Dame group [4], and evidence of QCA cell operation has been provided for

* Corresponding author. Tel.: +39-50-568537; fax: +39-50-568522.
E-mail address: macucci@mercurio.iet.unipi.it (M. Macucci).
1 Current address: ZMD, Grenzstrasse 28, D-01109 Dresden, Germany.

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doi:10.1016/j.spmi.2004.03.010

implementations in the GaAs/AlGaAs material system [5] and in the silicon-on-insulator (SOI) material system [6]. Here we focus on this latter implementation and discuss experimental results in comparison to simulations performed with a Monte Carlo code that we have developed for the analysis of single-electron circuits. We also propose an improved structure for the demonstration of a fully functional QCA cell in SOI technology.

2. Fabrication

The prototype QCA cell was fabricated starting from a 60 nm undoped silicon-on-insulator layer, which was subsequently doped with a concentration of 5×10^{18} cm^{-3} of phosphorus, by means of thermal diffusion. The device geometry was defined with e-beam lithography on a 65 nm layer of PMMA resist, and, after development, a 10 nm chromium layer was deposited by means of evaporation, followed by lift-off. Thus, an etch mask was formed, suitable for reactive ion etching with CHF_3 and O_2. Feature sizes were further shrunk by means of thermal oxidation.

The resulting structure is shown in Fig. 1(a): four dots, each with an adjustment side gate, are connected by constrictions that act as barriers for tunneling. The dots are at the vertices of a 100 nm square and have a diameter of 30 nm, after oxidation.

3. Measurements

The DC behavior of the thus fabricated QCA cell was investigated at a temperature of 4.2 K in liquid helium. The first step consisted in adjusting the voltage applied to the substrate, acting as a backgate, in order to have active barriers only in correspondence with the geometrically defined ones. Otherwise, potential fluctuations due to randomly located dopants and to defects would lead to the formation of multiple barriers, altering the behavior of the device. By adjusting the backgate voltage, the Fermi level can be raised over such fluctuations, thereby quenching their effect. It was found that with a substrate voltage of −6 V the Coulomb gap for each pair of dots in series was around 20 mV, a value consistent with the geometry, and charging diagrams for both dot pairs indicated the characteristic behavior expected for a structure with three cascaded tunnel junctions.

With reference to the equivalent circuit diagram of Fig. 1(b), we measured the source–drain currents I_{usd} and I_{bsd} through the upper and lower dots, respectively, as a function of the gate voltages V_{t5}, V_{t6} and V_{b5}, V_{b6}, with an applied source–drain voltage of 3 mV. From the thus obtained typical Coulomb Blockade honeycomb diagram, we obtain, following standard procedures [7], values for the capacitances in the equivalent circuit, if we assume the total capacitance of a single island to be around 50 aF (based on measurements on single-dot structures with analogous dimensions). The tunneling capacitances are of the order of 20 aF, while the regular ones are of the order of 1 aF. The observed relative homogeneity of interdot capacitance values is further evidence that the barriers are of geometrical origin and are not due to random fluctuations of the potential. The tunnel resistance per barrier turns out to be around 80 MΩ.

QCA action is based on the interaction between the upper and the lower pairs of dots: if proper bias voltages are applied, the transition of one electron from one dot to the other

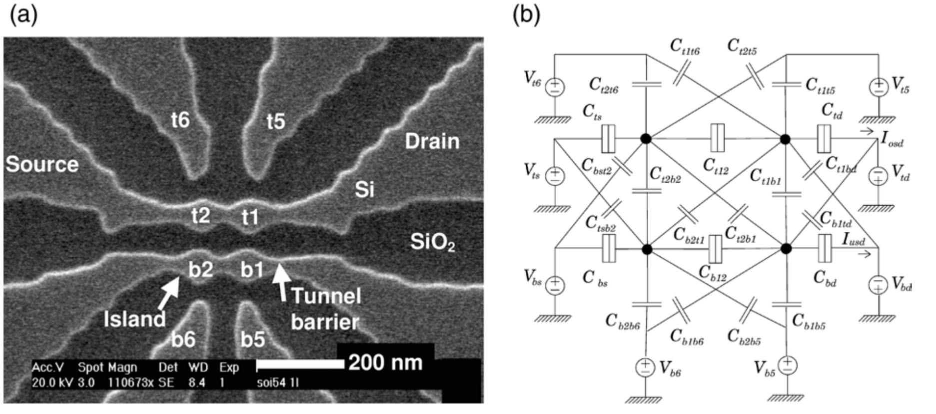

Fig. 1. (a) Layout of the SOI QCA cell, with the indication of the dots and biasing gates; (b) equivalent circuit for the QCA cell.

in one of the dot pairs will produce an electrostatic action on the other pair, such as to favor an opposite transition between its dots. Looking at the results of the measurements, we can observe partial QCA action in Fig. 2: we notice that, in correspondence with the peaks in the bottom current (solid curve), and, therefore, of the transfer of an electron from one bottom dot to the other, a secondary peak appears in the current through the top dots (dashed curve). This corresponds to a shift in the gate voltage V_{b5} by approximately 30 mV. Complete QCA action would have corresponded to a "locking" of the peaks in the current in the lower pair to those in the current of the upper pair.

4. Simulations

In order to better understand the experimental results and to improve the design with the objective of observing full QCA action in an SOI cell, we have set up a single-electron circuit simulator based on a Monte Carlo technique that is suitable for treating the time evolution of a circuit like the one shown in Fig. 1(b). The simulator is based on an evaluation, at each time step, of the free energy F of the circuit (which includes both the electrostatic energy and the work done by the outside voltage sources) and on the application of the transition rates

$$\Gamma = \frac{1}{e^2 R_T} \frac{\delta F}{1 - e^{-\frac{\delta F}{k_B T}}}, \tag{1}$$

where δF is the free energy variation, R_T is the tunneling resistance, e the electron charge, k_B the Boltzmann constant and T the temperature. Transition rates are computed at each time step for all possible events, and then one of them is chosen, based on the relative probabilities. Cotunneling effects can be included, but have not been considered in the present calculations, because we are mainly interested in the behavior in the region around the current peaks, where cotunneling contributions are negligible. The estimator for the

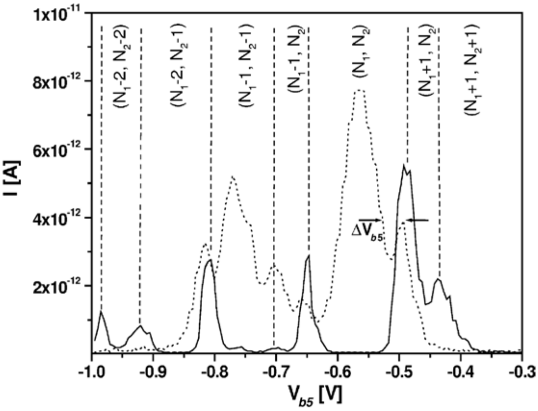

Fig. 2. Source–drain current in the upper (dashed curve) and lower (solid curve) double dots as a function of the voltage applied to the lower right gate.

current in a branch is obtained as the ratio of the number of carriers that have flowed through the junction in that branch to the simulation time. The external voltages are assumed to vary quasi-statically, i.e. over a time scale that is much longer than that over which tunneling events through the junctions take place.

For the specific problem at hand, which includes a large number of capacitors, our simulator allows a more straightforward definition of the circuit and better numerical precision, in comparison with the available public domain versions of other codes for the simulation of single-electron circuits.

In Fig. 3 we show a comparison between the current through the upper and the lower dot (upper and lower left panels, respectively) obtained experimentally and the results of the simulations (upper and lower right panels) as a function of the gate voltages V_{b5} and V_{b6}: the current is represented in a gray scale, with black corresponding to a zero value and white to the maximum value. We see that the periodicities are correctly reproduced, confirming the validity of the model.

We notice that the infinite periodicity with gate voltages appearing in the theoretical results is maintained only over a limited range of gate voltages in the actual results, because only within such a limited range the actual tunneling barriers correspond to those that are geometrically defined.

If we repeat the simulations at the lower temperature of 0.3 K, we observe a significant decrease of the broadening of current peaks, confirming its mainly thermal origin and suggesting that observation of QCA effects in these cells will be easier if the temperature is lowered into the hundreds of millikelvin range.

If we try varying circuit parameters, the simulation results show that, in order to obtain a QCA switching effect such as the one presented in [8], the capacitances between the upper and the lower dots should be increased to values of the same order of magnitude as those characteristic of the tunneling barriers. Results for a simulation at 0.3 K with a choice of 20 aF for the C_{bs}, C_{ts}, C_{bd}, C_{td} capacitors and of 27 aF for the interdot tunneling capacitors are shown in Fig. 4 as source–drain currents in the upper (dotted curves) and

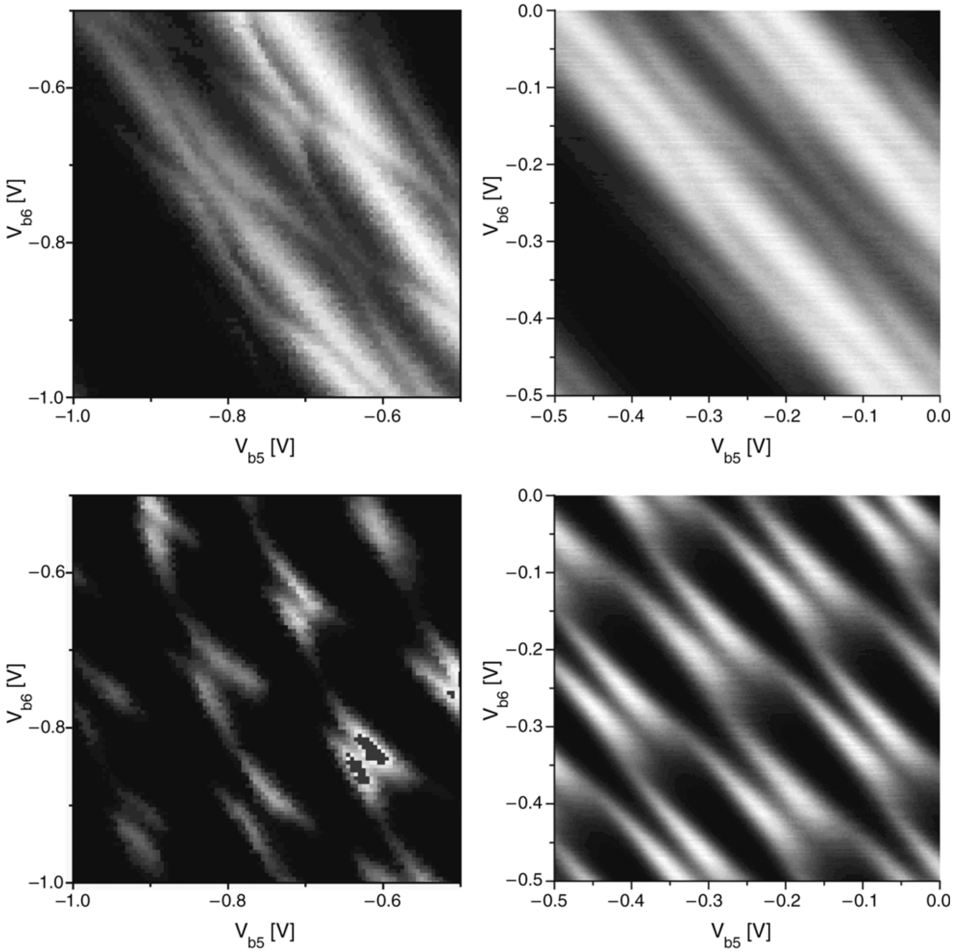

Fig. 3. Comparison between the experimental (left panels) and simulation (right panels) results for the current in the top (top panels) and bottom (bottom panels) double dots, as a function of the voltages applied to the two bottom adjustment gates.

lower (solid curve) double dots: the plots in Fig. 4(a) have been obtained for coupling capacitances between the upper and the lower dots of 2 aF (as in the presented experiment), while for the plots of Fig. 4(b) the coupling capacitances have been raised to 10 aF, leading to clear peak pairing [8].

Increased coupling between the upper and lower double dots could in principle be achieved in several different ways: reducing the capacitances of the tunnel barriers, creating tunnel junctions also between the upper and lower dots, fabricating an asymmetric cell with a reduction of the separation between the upper and lower double dots.

A reduction of the capacitance of the tunnel barriers would be very valuable from the point of view of raising the operating temperature, but is extremely challenging from the

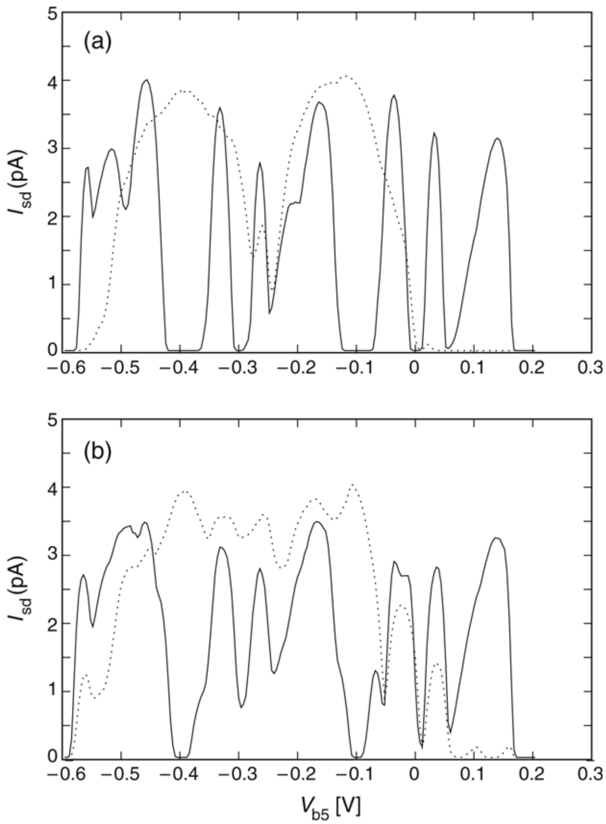

Fig. 4. Source–drain current in the upper (dotted curve) and lower (dashed curve) double dots as a function of V_{b5}, with V_{b6} being kept at 0.2 V, at a temperature of 0.3 K, for coupling capacitances of 2 aF (a) or of 10 aF (b).

technological point of view. Creation of tunnel junctions between the upper and lower double dots would lead to further difficulties in the combined adjustment of the backgate and lateral gate voltages, in order to achieve simultaneous operation of all junctions.

Therefore the most promising approach consists in reducing the distance between the upper and the bottom dots, while keeping constant the horizontal separation. In this way, the cross capacitances such as C_{t1b2}, which affect adversely the cell behavior, will not undergo too significant an increase, while the coupling capacitances will reach a value sufficient for correlated switching.

5. Conclusions

We have presented the results from the DC characterization of a QCA cell fabricated in silicon-on-insulator technology, and compared it with those from simulations performed with a purposely developed Monte Carlo code for the analysis of single-electron circuits.

Using the capacitance and tunnel resistance values extracted from measurements, a good agreement is achieved between experimental and simulation results. The simulator has then been used to test a modification to the cell layout, which should enable demonstration of full QCA action in SOI technology.

Acknowledgements

This work was supported by the European Commission through the QUADRANT project (within the MEL-ARI initiative) and by the Italian National Research Council (CNR) through the "5% Nanotecnologie" program.

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