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Perspectives and challenges in nanoscale device modeling

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Perspectives and challenges in nanoscale device modeling

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Abstract

In this paper, we discuss the role of adequate modelling tools in the development of nanoelectronic technology and devices, including both down-the-roadmap Complementary Metal-Oxide-Semiconductor (CMOS) technology and alternative nanodevices. Such tools can enable understanding of the relevant physical mechanisms on the one hand, and performance evaluation and optimization of device structures, on the other hand. Relevant examples are discussed, drawn by our recent activity, including ballistic strained-silicon Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs), stress-induced leakage currents, nanocrystal memories, and silicon nanowire transistors.

Keywords:: Nanoelectronics; Semiconductor device modelling; TCAD; Nanotechnology

1. Introduction

I would like to focus on the following question: what should technology developers reasonably expect from device modelling? The answer is not obvious, since typically Technology Computer Aided Design (TCAD) tools—including both process and device simulators—are accurate, or 'predictive', only for a sufficiently stable and 'mature' technology, and after a lengthy calibration procedure [1]. This poses the issue of the relevance (or irrelevance) of device modelling for the development of a new technology node, in which new processes and/or materials are introduced, that are not under complete control until the technology is finally released, and for which doping profiles and geometry are not known with sufficient accuracy. Such problems become even more serious for nanoscale MOSFETs and alternative nanodevices, whose electrical properties are extremely sensitive to the presence of single defects and impurities, and to the finest details of the geometry.

I do not want to shed a negative light on TCAD. The positive aspect is that device modeling can be very useful even if it is not fully 'predictive', because it can still provide optimization guidelines, explanations of the characterization results, and insights of the transport mechanisms. Let me underline the fact that in many cases, even for just reproducing the qualitative behaviour, it is necessary to implement a very sophisticated and specific models.

In the following, I will show a few examples of significant insights that can be gained from detailed simulations of nanoscale devices, both 'secular' MOSFETs and alternative structures. Examples will be drawn from recent activities pursued at the University of Pisa and will only briefly mentioned here. The reader interested in a more complete description of the examples is referred to the cited papers.

2. Advantages of strained-silicon MOSFETs in the ballistic regime

The first example I would like to describe concerns the use of strained silicon as MOSFET channel material that is currently pursued to obtain a significant increase of electron mobility. One issue that we wanted to address is whether such performance advantage to be gained from strained silicon would remain also in the ballistic transport regime, when mobility, as such, has no physical meaning [2]. In order to evaluate this aspect we have used a two-dimensional device simulator (NANOTCAD2D), developed by Gilberto Curatola and myself, consisting of a

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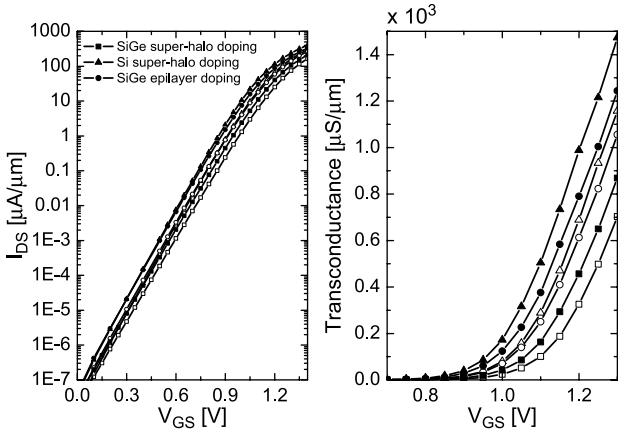

Fig. 1. Transfer characteristics (left) and transconductance (right) of the silicon ballistic bulk MOSFET with superhalo doping (triangles), the SiGe ballistic MOSFET with superhalo doping (squares), and the SiGe ballistic MOSFET with epitaxial layer doping (circles). White symbols correspond to $V_{DS}=0.1$ V, and solid symbols correspond to $V_{DS}=1$ V (Figure 4 of Ref. [2]).

self-consistent solver of the Poisson equation, Schrödinger equation, and the continuity equation in the ballistic transport regime [3].

Then, we have focused on the so called 'Well tempered MOSFET' with channel length of 25 nm [4]. We have considered devices fabricated on a SiGe heterostructure with the same geometry and two different doping profiles: one with the same profile as the bulk silicon device, and the dose adjusted in order to fit the bulk device C–V characteristics, and the other with an epitaxial doping chosen, again, in order to fit the C–V characteristics of the bulk MOS.

The code takes into account the effect of strain on silicon bandstructure, in particular on the electron affinity and the effective mass, given that we stick to the parabolic approximation. Simulations performed with NANOTCAD2D provide the results shown in Fig. 1. It can be seen that the transfer characteristics and the transconductance curves are very similar for the three devices, with as slight horizontal shift, mainly due to a slightly different drain-induced barrier lowering, which is reduced in the SiGe superhalo device, that has the higher doping density.

Such very simple simulation does not claim to be complete nor extremely detailed. Nevertheless, it highlights an important aspect: the present advantage of strained silicon in terms of current drive (due to the increased mobility) is expected to shrink and eventually to vanish when (and if) the devices approach the ballistic transport regime.

3. The nature of SILCs

Stress-induced leakage currents (SILCs) are the main single cause of failure of Flash memories, the fastest growing segment in the semiconductor market. Understanding their nature is therefore of paramount importance. Recent studies [5–8] agree in identifying trap-assisted tunnelling (TAT) as the physical mechanism responsible for stress-induced leakage currents (SILCs) through thin SiO_2 MOS capacitors: high electric fields, applied to MOS structures, generate traps in the oxide which introduce localized energy levels in the oxide gap. On the contrary, the issue is still controversial as far as trap properties are concerned: both the energy distribution of traps and their microscopic nature are a matter of discussion.

A perfect fitting between numerical results and experimental data, as far as DC current–voltage characteristics are concerned, is not sufficient to determine the trap distribution in a unique way: for this reason, an investigation of other features of SILCs is needed. For example, the study of SILC transient components leads to the result that the SILC DC component is due to traps located in correspondence with the silicon electrode gap [6]. We have based our investigation on the following consideration: Pauli exclusion principle and Coulomb repulsion prevent two electrons from occupying the same trap, and therefore introduce a correlation in the motion of carriers. This causes the suppression of the power spectral density of shot noise, related to SILC current, with respect to the full value $S=2qI$, obtained for current through fresh oxides, and typical of uncorrelated motion of electrons.

Alessandro Nannipieri and I have used our model of trap-assisted-tunnelling to extract a trap distribution that would allow us to fit both the DC and the noise properties of a MOS capacitor with a 6 nm silicon oxide layer [9]. A one-dimensional self-consistent Poisson–Schrödinger solver was used for computing the (direct) not assisted current, modelling the trap-assisted tunnelling current at low electric fields and extracting traps' distributions in the oxide. We have found that for such oxide thickness both the I–V characteristics and the shot noise suppression can be fully described in terms of a distribution of traps uniform in space, and Gaussian in energy, located in correspondence of the silicon energy gap, with a peak 0.5 eV below the position of the silicon conduction band and a standard deviation of 82 meV. Comparison of the theoretical curves with experiments from Ref. [8] is shown in Fig. 2. The distribution obtained is also compatible (though not identical) with previous works [5,6] and is able to fit experimental results from the literature [9]. In this case, accurate modeling, combined with electrical characterization, allows performing a physical characterization of oxide traps.

4. Electron storage in nanocrystal memories

Nanocrystal memories represent a very promising device structure for obtaining ultrascalable non-volatile memories. Charge storage occurs is a layer of silicon oxide in which a high density ($\sim 10^{12}\,\mathrm{cm}^{-2}$) of silicon nanocrystals with

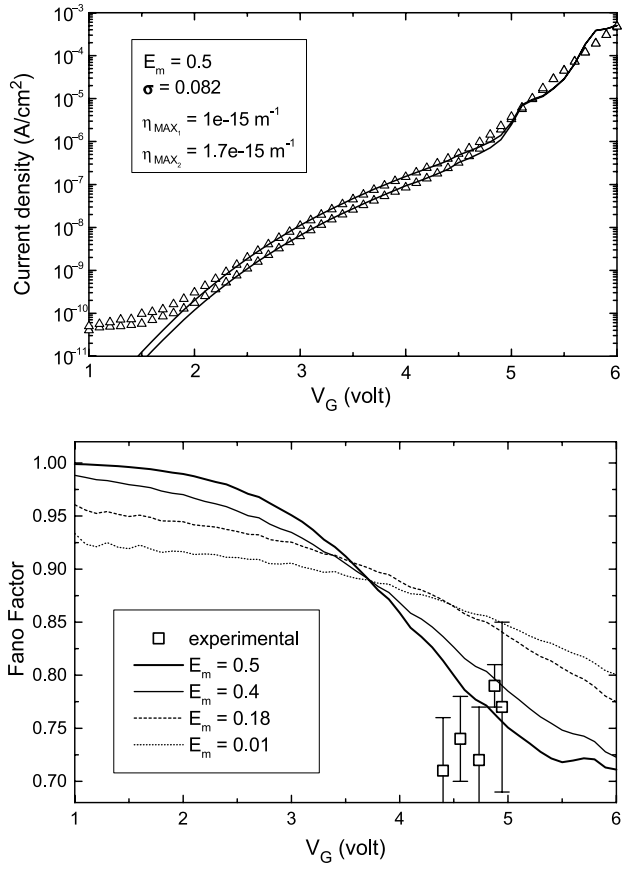

Fig. 2. Comparison of the theoretical and experimental DC characteristics (above) and noise suppression factor (below) for a MOS capacitor with 6 nm thick oxide. Figures are from Ref. [9].

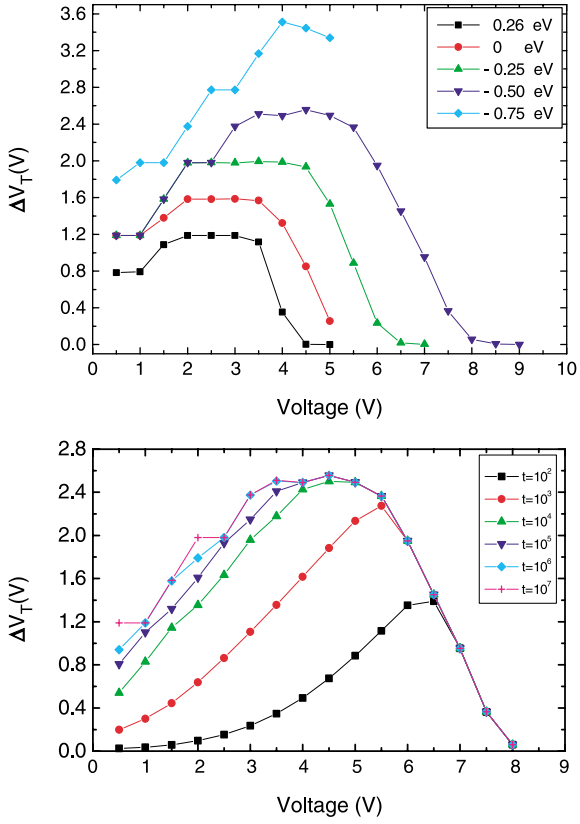

Fig. 3. Threshold voltage shift as a function of the gate voltage for different values of the trapping energy. Profiles corresponding to the stationary regime (a) and parameterized with different program times (b).

diameter of few nanometres is embedded. As far as this type of device is concerned, a debated issue is whether electrons are actually trapped in the electron states defined by the hard confinement due to the silicon–silicon oxide barrier in the conduction band, or in traps located at the interface between the silicon nanocrystal and the dielectric [10,11].

Michele Schirinzi and I have addressed this issue with detailed simulations of one-dimensional device cuts, using our Poisson–Schroedinger solver and a model for trap-assisted tunnelling described in [8]. We have implemented a master equation based on the generation and recombination rates computed in stationary conditions and as a function of time. The reference device, used for our calculations and as a term of comparison with the experimental results, is the one described in Ref. [12].

First, we have computed the threshold voltage shift ΔV_T as a function of the program voltage in stationary conditions, for a trap energy corresponding to the first Kohn–Sham orbital in the silicon dots (0. 26 eV above the conduction band). The plot is shown in Fig. 3(a) and exhibits a significant discrepancy with respect to the experimental results: while in the experiments the peak of the threshold voltage shift is obtained for a control gate voltage close to 7 V, in the simulations the peak is obtained for about 3 V, while, increasing the gate voltage, ΔV_T rapidly goes to zero. By simply adjusting the parameters of the gate stack, and the dimensions of the nanocrystals, we have verified that one cannot recover the experimental results.

We have therefore investigated how the behaviour changes if we decrease the trap energy, moving it also in the silicon gap. Results are again shown in Fig. 3(a): the lower the trap energy, the higher the gate voltage corresponding to the peak of ΔV_T. For a trap energy positioned 0.5 eV below the silicon conduction band, i.e. close to the middle of the energy gap, the situation is closer to the experiments.

For such energy we have also performed time dependent simulations, that yield the results shown in Fig. 3(b), where ΔV_T is plotted versus the gate voltage with the program time used as a parameter. By comparing such results with the experiments shown in Figure 10 of Ref. [12], we see that the agreement is reasonable.

We know, of course, that the technology for the deposition of the silicon nanocrystal memory is not mature, that process deviations are significant, and that nanocrystal size and oxide thickness are subjected to significant fluctuations. In this situation, we cannot expect to reproduce accurately the experimental results, and to extract fine

information. What can we say then, from our simulations? That the hypothesis of trap energy corresponding to the bound states in the nanocrystal conduction band is not compatible with the experiments, while trap energies located near the middle of silicon gap are. To technologists this is an important information, since it means that if one wants to improve the trapping properties of the device, she should focus on the nanocrystal–dielectric interface, and not just on the size and shape of the nanocrystals. Results are not definitive, as can be imagined, but, combined with other experimental evidence [10,11], contribute to build a coherent picture of the storage mechanisms.

5. Silicon nanowire transistors

Finally, I would like to present briefly some work we are doing on the evaluation of perspectives of silicon nanowire transistors for technology nodes at the end of the present ITRS Roadmap, starting from the 32 nm node [13]. In these days, simulations of such devices cannot be performed with commercially available TCAD tools. Gianluca Fiori and I have developed a code that allows us to solve in a self-consistent way the 3D Poisson–Schrödinger equation with density functional theory, and the continuity equation considering either drift-diffusion or ballistic transport in each one-dimensional subband [14]. At present, the main limit of the code is that it does not allow us to take into account inter-subband scattering, so that it can only be used for nanowires with very small cross-section (few nanometres).

Silicon nanowire transistors are considered interesting devices for the possibility of strongly reducing short channel effects without resorting to new materials for the dielectric and for the gate. Several issues can be understood with the help of modelling tools, such as for example the relevance of drain-to-source tunnelling, the subthreshold behaviour, and the Drain-induced Barrier Lowering (DIBL).

For the device structure shown in Fig. 4, with a nanowire cross-section of 5 nm×5 nm, oxide thickness of 1.5 nm, metal gate, and a channel length of 7 nm, the transfer characteristics are shown in Fig. 5, computed for different transport regimes: drift-diffusion within each subband, ballistic transport with semiclassical electron motion (no tunnelling), ballistic transport including source-to-drain tunnelling.

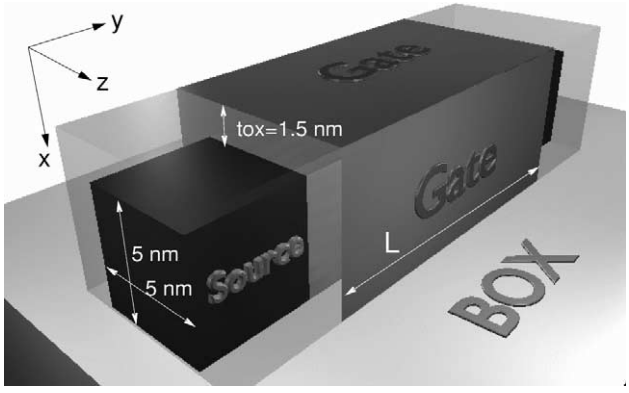

Fig. 4. Structure of the silicon nanowire transistor considered in the 3D simulations. Figure is from Ref. [14].

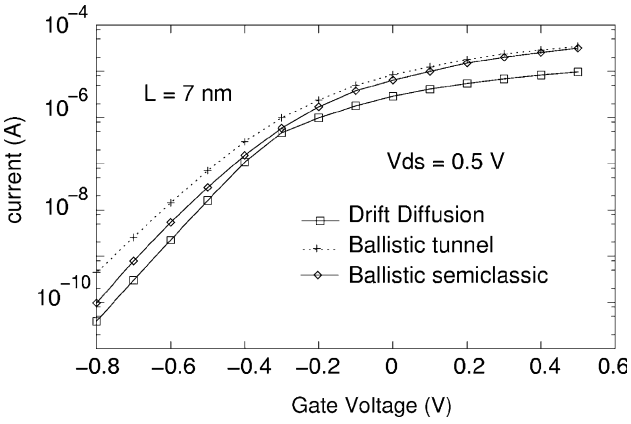

Fig. 5. Transfer characteristics of a silicon nanowire transistor with the structure shown in Fig. 4 and a channel length of 7 nm. Results are obtained with the 3D and different transport mechanisms: drift-diffusion and ballistic (including tunnelling and only semiclassical electron motion). Figure is from Ref. [14].

A few general considerations may be drawn. First, short channel effects are significant but still acceptable. Depending on the transport regime, the subthreshold voltage swing is between 120 and 130 mV/decade, while DIBL is between 300 and 400 mV/V. In addition, source-to-drain tunnelling is significant both in subthreshold and in strong inversion. This last aspect has not been noticed before, and is mainly due to the fact that the barrier for electrons in the silicon nanowire is rather shallow. Even in strong inversion, tunnelling currents accounts for between 10 and 20% of the total drain current.

For longer channels, the situation rapidly becomes almost ideal. For example, for a 25 nm nanowire transistor with the same transversal structure, the substhreshold swing is about 65 mV/decade, the DIBL is about 30 mV/V and the tunnelling current component is really negligible.

Several other issues may be investigated with the same model, such as the impact of geometry and doping of the source and drain contacts on device characteristics, the impact of corner rounding, the effect of random impurity distribution on the distribution of threshold voltages and transconductances. For all such issues, modelling can provide important insights, even if it is not ‘predictive’ in the sense that some optimist would expect.

6. Conclusion

In this paper, I have presented a few issues in which detailed physical modelling of nanoscale devices can

provide very useful insights of device behaviour, helping us to understand what are the physical aspects that are relevant to particular issues, what are the main trends, and on which aspects we have to focus in order to improve device behaviour. This can be the critical mission of nanoscale device modeling, requiring not huge do-it-all tools, but simulation tools with different degrees of sophistication, tailored to the particular problem at hand. The realm of 'predictive' simulation tools will probably be limited to mature technology and brute force calibration, and the problem of 'yesterday's technology modelled tomorrow' [1] will probably remain unsolved for quite some time.

I would like to extend these considerations to modelling and simulation of micro- and nanosystems, that represent the main focus of the European Micro and Nanotechnology Conference. In this domain, advanced modeling tools are even less used, probably because a complete tool would be even more complicated, the developers being forced to include multiple physical mechanisms. Also in this case, I believe the focus of modelling tools should be on solving very specific problems, and not on building the ultimate TCAD tool. In such a way, one can really provide precious inputs to technology developers, and—in time—build the appropriate hierarchy of abstraction levels that can lead to versatile and effective modelling tools.

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