Dependence of the programming window of silicon-on-insulator nanocrystal memories on channel width

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Dependence of the programming window of silicon-on-insulator nanocrystal memories on channel width

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In this letter, we investigate the observed dependence of the programming window of silicon-on-insulator (SOI) nanocrystal memories on the width of the channel. Indeed, experiments show that the obtained threshold voltage shift after programming strongly increases with decreasing channel width. We show that such behavior is due to the preferential injection of electrons, during the program operation, from regions close to the edges of the SOI channel, where the electric field is stronger. As a consequence, charge is mostly stored in the dots in the oxide region surrounding the edges, and therefore is more and more effective as the channel width is decreased. Our conjecture is verified through dedicated three-dimensional simulations and checked against other mechanisms proposed in the literature. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1884263]

The concept of storing information in nanocrystals[1] is promising for nonvolatile memories, because it would significantly improve their scalability with respect to conventional double-poly Flash EEPROMs, and therefore would allow to achieve higher operating frequency, lower power consumption, and higher density.[2–6]

Scalability would mainly be a consequence of the presence of discrete and electrically insulated storage nodes, that make information retention less vulnerable to isolated defects in the tunnel oxide.

In recent experiments on a silicon nanocrystal floating gate memory with ultranarrow channel,[7,8] an increase of the threshold voltage shift achieved after programming has been observed with decreasing channel width, when all other parameters are kept constant. Such behavior has been related to the presence of percolating paths in the channel[7,8] in the subthreshold region.

However, the experiments we have performed on very narrow SOI nanocrystal memories, show that the same behavior still appears if the threshold voltage is measured in strong inversion, when the whole channel is densely populated, and therefore percolation cannot be a significant transport mechanism. In this work, we provide an alternative physical explanation which is consistent with the results obtained both in strong inversion and in the subthreshold region.

Figure 1 shows the longitudinal and transversal sections of the fabricated devices [Figs. 1(a) and 1(b), respectively]. The 15-nm-thick (100)-oriented channel with varying width W and length L of 50 nm is defined by electron beam lithography (EBL) and reactive ion etching (RIE). The SiO_2 tunneling layer has a thickness of 2.5 nm and is grown by rapid thermal oxidation.

The layer of silicon dots, with a density of about 5×10^{11} cm^{-2} and average dot diameter of 6 nm, is obtained by the phase separation of a silicon rich oxide ($SiO_{0.5}$) layer through an annealing step at 1050 °C for about 3 min under N_2.[9] The dot layer is then covered with a deposited 20 nm control oxide and, finally, polysilicon gates are defined by EBL and RIE.

In Fig. 2(a) we show typical measured written/erased transfer characteristics, while in Fig. 2(b) the threshold voltage shifts as a function of the channel width, obtained in the strong inversion and in the subthreshold regime, for a single device and for a writing voltage of 10 V and a programming time of 10 s.

As can be seen, the effect is also present in strong inversion, when the Debye length is about 3 nm,[10] for an electron concentration $n=2\times10^{18}$ cm^{-3}; percolating paths then cannot be the main source of the observed effect, since for such electron density charged dots are not able to deplete the channel underneath.

In order to investigate the decrease of the threshold voltage shift as a function of the channel width, we have performed detailed simulations of six different devices with same L (50 nm), but with W varying from 30 to 80 nm, by means of an in-house developed three-dimensional Poisson/Schrödinger solver.[11] The longitudinal and the transversal

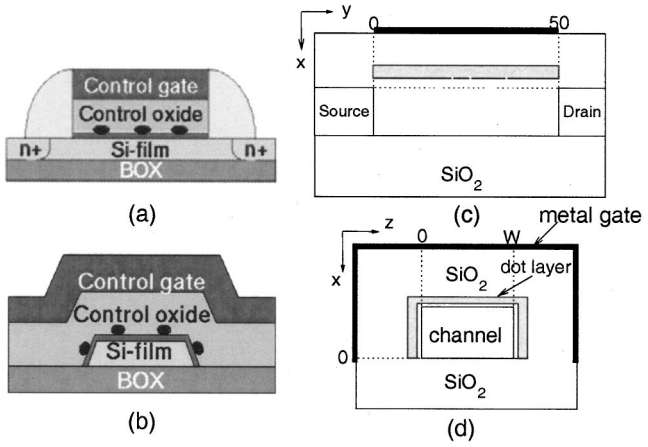

FIG. 1. (a),(b) Sketch of the fabricated nanomemory (longitudinal and transversal views, respectively); (c),(d) simulated three dimensional simplified structure (longitudinal and transversal sections, respectively).

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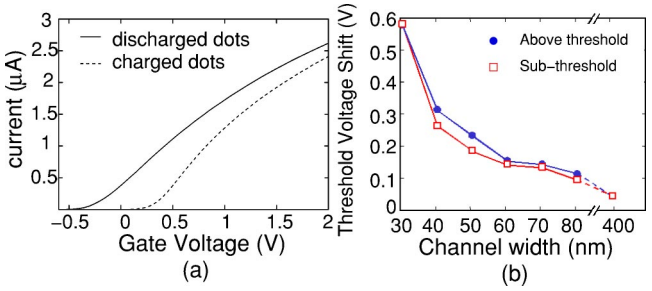

FIG. 2. (a) Experimental transfer characteristics of a nanomemory (L=50 nm, W=30 nm, V_{ds}=100 mV) in the erased and programmed states; (b) measured threshold voltage shift as function of the channel width, in the strong inversion and in the subthreshold regime, as obtained with a writing voltage of 10 V and a programming time of 10 s.

sections of the simplified structure used in the simulation of the nanocrystal memory are shown in Figs. 1(c) and 1(d): the channel section is rectangular rather than trapezoidal, the gates are metallic, and the charged dots have been modeled by a layer of fixed charge with a thickness of 4 nm. The threshold voltage has been computed with a simplified drift/diffusion transport model, with constant mobility and valid for small drain-to-source voltage.[12] In particular, in the subthreshold regime, the threshold voltage has been defined as the gate voltage at which the drain-to-source current is equal to 1 nA; in the strong inversion regime it has been defined as the intercept with the gate voltage axis of the line that fits the transfer characteristic in strong inversion. As a first attempt, in order to reproduce by simulations the effect observed in Fig. 2, we have considered a uniform and continuous distribution of fixed charge in the dot layer, corresponding to two electrons per dot and to an experimental dot density of 5×10^{11} cm^{-2}. In Fig. 3 the threshold voltage shift computed in the subthreshold and in the strong inversion regime is plotted as a function of W. As can be noticed, simulation results are in evident contrast with experiments, since the shift slightly increases with increasing W. The same contrast is observed if a discrete distribution of fixed charge in the dot layer is considered. We have computed the threshold voltage shift over a sample of twelve devices (as in the experiments) with the same nominal dot density, but with a different discrete distribution of charged dots. Results in the subthreshold regime are shown in Fig. 4. Even in this case, the threshold voltage shift is almost independent of channel width.

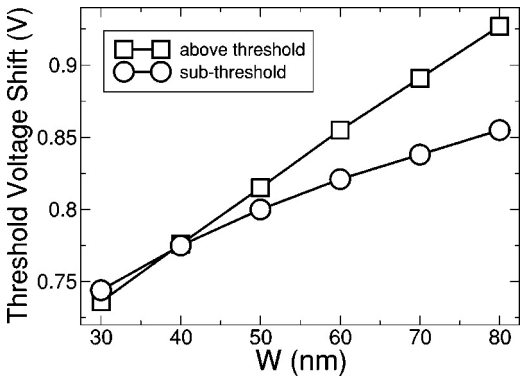

FIG. 3. Simulated threshold voltage shift as function of the channel width for a continuous fixed charge in the dot layer, computed in the subthreshold and in the strong inversion regime.

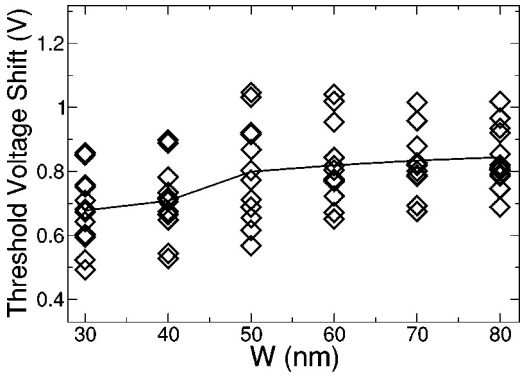

FIG. 4. Threshold voltage shift as function of the channel width for a random discrete distribution of storage nodes, computed in the subthreshold regime.

We have therefore critically addressed our initial assumption of uniformly distributed stored charge. Indeed, the electrostatics of the structure is such that close to the channel edges the electric field in the oxide is higher and the tunnel barrier lower, as extracted from simulations and shown in Figs. 5(a) and 5(b). As a consequence, the direct tunneling current[13] through the oxide is about two orders of magnitude larger at the edges than at the center of wire and, since storage nodes are discrete, charge is preferentially stored in dots close to the edges of the channel. The narrower the channel, the more effective the charge stored near the edges on the device behavior. In the limit of infinitely large channel, electrons stored in dots near the edges have no effect, and the

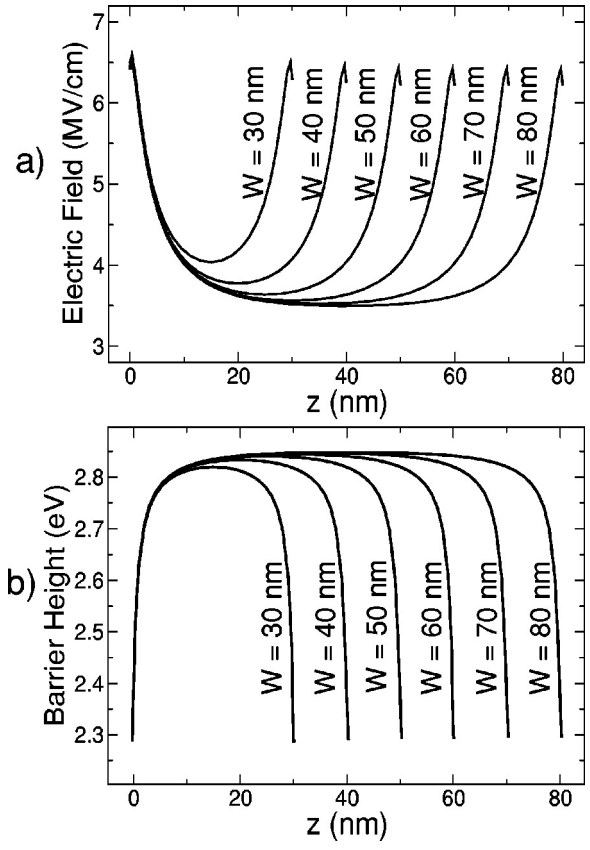

FIG. 5. (a) Electric field in the direction perpendicular to the Si/SiO_2 interface and (b) local barrier height seen by the electrons in the channel as a function of transversal position in the channel [shown in Fig. 1(d)] for different values of W.

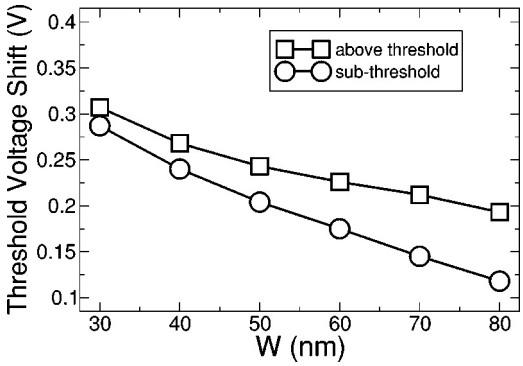

FIG. 6. Threshold voltage shift as a function of the channel width for a charge density in the dot layer proportional to the local tunnel current, computed in the subthreshold and in the strong inversion regime.

threshold voltage shift is only due to the smaller amount of charge injected in the middle of the channel.

To test this hypothesis, we performed a new simulation assuming a locally stored charge proportional (for simplicity) to the local tunnel current. Results are shown in Fig. 6. As can be noticed, simulations are now able to reproduce the experimental behavior.

We want to point out that this effect is also present if the structure does not have sharp edges, but only round edges, and that the presence of a curvature is sufficient to ensure preferential injection. For example, we consider the limit in which the sharp square edges are replaced by the arc with the minimum curvature compatible with the device structure, shown in Fig. 7(a). To this purpose, we have performed a two-dimensional simulation of the cross section, which corresponds to a device with an infinite channel length. Results in the strong inversion and in the subthreshold regime are shown in Fig. 7(b): also this structure is able to reproduce the observed dependence of the programming window on the channel width. Indeed, also in this case, tunneling is strongly enhanced through the thin oxide in the curved regions, and therefore the dots in the regions of higher curvature are the most charged. For completeness, the same kind of plot of Fig. 7(b) is shown in Fig. 7(c) for a rectangular cross section.

In conclusion, we have studied the dependence of the programming window of SOI nanocrystal memories on the channel width. As confirmed by the experiments, the observed effect can be explained by preferential injection of charge in correspondence of channel edges, due to the reduced barrier height and increased electric field in the tunnel oxide near the channel edges.

In addition, in our case the threshold voltage shift is always proportional to the stored charge, for all the channel widths. Therefore, the threshold voltage shift is expected to decay exponentially with time as observed in experiments in Ref. 7. In the subthreshold regime, percolating paths proposed in Ref. 7 can represent an additional mechanism, that, together with the main mechanism explained in this work, can reinforce such effect.

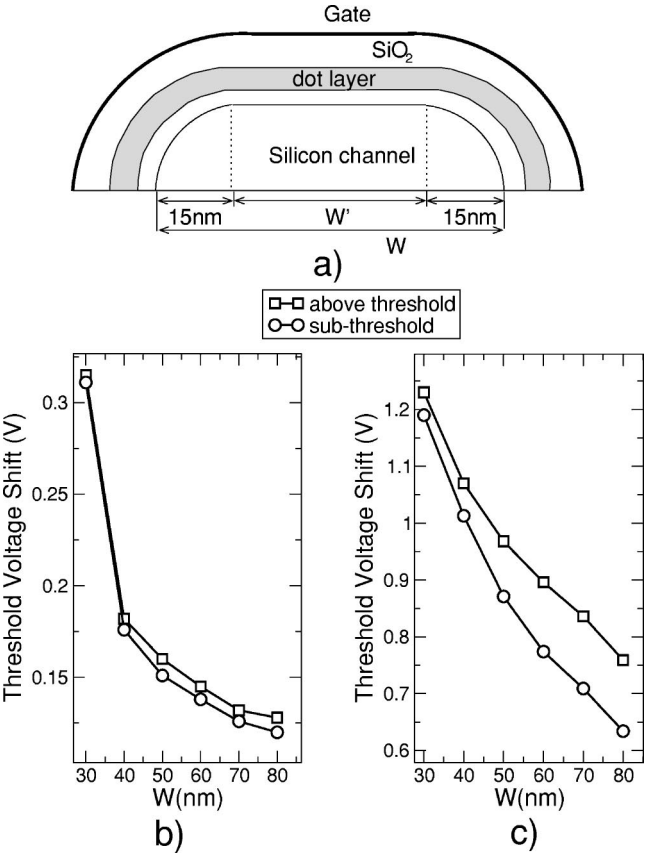

FIG. 7. (a) Structure of the "round" edge device; threshold voltage shift as a function of the channel width for a fixed charge in the dot proportional to the direct tunnel current for the "round" structure (b) and for a rectangular cross section; (c) channel lengths tends to infinity in both cases.

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