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An Ultra-Low-Power temperature compensated voltage reference generator

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An Ultra-Low-Power, Temperature Compensated Voltage Reference Generator

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***Abstract*—A CMOS voltage reference, based on the difference between the gate-source voltages of two NMOS transistors, has been realized with AMS 0.35 µm CMOS technology (V_{thn}=0.45 V and V_{thn}=0.75 V at 0 °C). The minimum and maximum supply voltages are 1.5 V and 4.3 V, respectively. The supply current at the maximum supply voltage and at 80 °C is 2.4 µA. A temperature coefficient of 25 ppm/°C and a line sensitivity of 1.6 mV/V are achieved. The power supply rejection ratios without any filtering capacitor at 100 Hz and 10 MHz are larger than -74 and -59 dB, respectively. The occupied chip area is 0.08 mm^2.**

I. Introduction

THE widespread use of battery-operated systems, the relatively slow progress of battery performance/cost ratio and the need to minimize simple maintenance procedures, such as battery replacement, are pushing the design of very low voltage and low power systems, both digital and analog. Here we focus on a ubiquitous component of such systems, the voltage reference generator, which in turn has to be "power-scaled", in order to be able to operate with a very small fraction of the total power budget.

Many solutions exist in literature to generate a reference voltage. A typical approach consists in using a bandgap reference, which can be implemented in any standard CMOS technology exploiting the parasitic vertical BJTs [1, 2]. Other voltage references exploit the principle of threshold voltage difference, which can be based on a selective channel implant [3, 4], flat-band voltage difference obtained by different gate materials [5] and work function difference obtained by different gate dopings [6]. Such solutions can not be implemented in a standard CMOS technology because they require additional fabrication steps.

An additional type of voltage reference, implemented with a standard CMOS technology, is based on weighted gate-source voltage difference between an NMOS and a PMOS transistor [7, 8].

In this paper we present a voltage reference, which can be implemented in any standard CMOS technology, based on the weighted gate-source voltage difference between two NMOS transistors. Such solution leads to a perfect cancellation of the effect of the temperature dependence of carrier mobility.

In Sections II-V the circuit implementation is discussed in detail. In Section VI the experimental results are shown.

II. Circuit Description

The proposed voltage reference generator is shown in Fig. 1. It consists of a circuit that generates a current I_0 almost independent of the supply voltage V_{DD}; such current is then amplified and injected into an active load to generate the reference voltage. A low temperature drift voltage reference is obtained by compensating the temperature dependence of the generated current with the temperature dependence of the NMOS threshold voltage. The particular configuration used allows us to suppress the effect of the temperature dependence of mobility. The proposed voltage reference was implemented in AMS 0.35 µm CMOS IC technology.

A. Current Generator Circuit

In the current generator circuit a current mirror imposes equal currents in the two branches of the circuit. In order to reduce the channel modulation effect that causes a mismatch between the currents in the two branches, the channel lengths of the two transistors M_5 and M_6 are chosen large enough. Transistors M_1 and M_2 are biased in the subthreshold region, while transistors M_3 and M_4 work in the saturation region. Such behavior is achieved through careful biasing: the gate-source voltage of M_3 (M_4) must be larger than the gate-source voltage of M_1 (M_2). As a consequence, since the four transistors have the same drain current, the W/L ratio of M_1 (M_2) has to be larger than that of M_3 (M_4). The I-V characteristics of a MOS transistor that operates in the saturation and in the subthreshold region can be approximated by (1) and (2), respectively,

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{GS}-V_{th}\right)^2 = \frac{k}{2}\left(V_{GS}-V_{th}\right)^2, \qquad (1)$$

$$I_D = \mu V_T^2 \frac{W}{L}\exp\left(\frac{V_{GS}-V_{th}}{mV_T}\right)\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right], \qquad (2)$$

where μ is the carrier mobility in the channel, V_T is the thermal voltage, V_{th} is the threshold voltage, W and L are the channel width and length, respectively. Assuming that the currents in the two branches of the current circuit generator are equal, the current I_0, in Fig. 1, becomes

$$I_0 = \frac{m^2 V_T^2 k_4}{2}\left(\frac{N}{N-1}\right)^2 \ln^2\left(\frac{W_2/L_2}{W_1/L_1}\right), \qquad (3)$$

where $N = \sqrt{k_3/k_4}$. The proposed configuration of the current generator allows us not to use a resistance to generate the

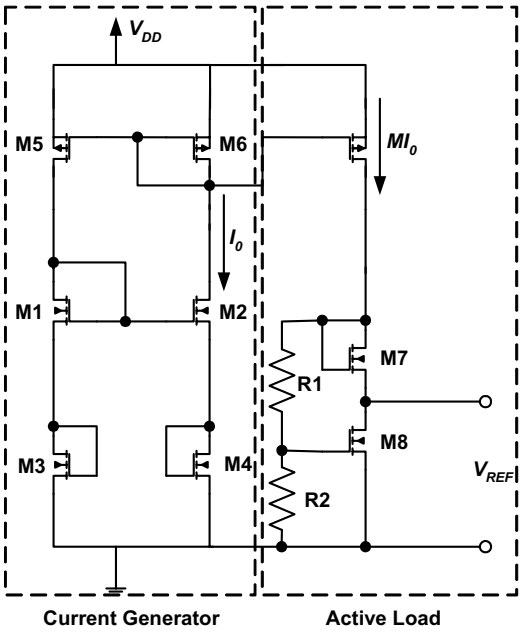

Fig. 1: Proposed Voltage Reference Circuit.

current I_0, as it usually happens in such kind of circuits [8, 9]. This is particularly important if the current to be generated has to be very small, to drastically reduce the power consumption of the voltage reference circuit. In such case a large resistance would be required causing a large area occupation on the chip. Furthermore, as will be clearer later, the use of M_3 and M_4 allows us to fully suppress the effect of the temperature dependence of mobility, leading to excellent temperature compensation. Moreover, since the two transistors M_1 and M_2 operate in the subthreshold region, the effect of channel length modulation is negligible provided that their drain-source voltages are much larger than the thermal voltage, as evident from (2). On the other hand, the channel length modulation effect of M_3 and M_4 is negligible since they are long-channel devices, and since their drain-source voltages have very small variations, when the supply voltage is varied, because they are equal to their gate-source voltages, which, for small variation of the current I_0, are almost constant. Almost all the variation of the supply voltage drops 1) on the drain-source voltage of M_2, without causing large variations of the current I_0, since it works in the subthreshold region, 2) on the drain-source voltage of M_5. In the latter case, in order to drastically reduce the channel length modulation effect, the channel length of M_5 has to be quite large.

Since the reference voltage generator has two stable states, corresponding to the current given by (3) and to zero current, a start-up circuit is used to ensure that the former stable state is achieved. Such a circuit compares the current I_0 with a much smaller known current. If I_0 is zero, it provides a start-up current to change the stable state.

B. Active Load

The active load used to generate a reference voltage with a low temperature drift consists of two NMOS transistors biased by a current obtained by mirroring the current I_0 and amplifying it by a factor M. Both transistors M_7 and M_8 operate in the saturation region. The output voltage reference has the expression shown below,

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) V_{GS8} - V_{GS7} . \quad (4)$$

As will be clearer later, in order to ensure the correct temperature compensation, it is necessary that most of the bias current MI_0 flows through the transistor M_7 and M_8 rather than through the resistances R_1 and R_2. As a consequence, once we fix the maximum resistance values acceptable for a reasonable area occupation on the chip, we determine the minimum value of the bias current that ensures the correct operation of the voltage reference generator, from the condition

$$MI_0 >> \frac{V_{DS8} + V_{GS7}}{R_1 + R_2} . \quad (5)$$

Equation (5) limits the minimum power consumption of the voltage reference generator. The resistances will be implemented by using high resistive poly to minimize the area occupation on the chip.

III. Supply Voltage Dynamic

The minimum supply voltage is imposed by the current generator circuit. In particular, we have to ensure that the transistor M_2 has a drain-source voltage of at least 100 mV so that the effect of the drain-source voltage in (2) and then the channel length modulation of M_2 can be neglected. Consequently, the following expression has to be satisfied,

$$V_{DD} > |V_{GS6}| + V_{DS2MIN} + V_{GS4} . \quad (6)$$

Then the supply voltage must be larger then 1.5 V in the AMS 0.35 µm CMOS process. The maximum supply voltage is imposed by the maximum drain-source voltage allowed for MOS transistors, as shown below,

$$V_{DD} < |V_{DS5MAX}| + V_{GS1} + V_{GS3} . \quad (7)$$

Since in the AMS 0.35 µm CMOS process the maximum value for the drain-source voltage of a MOS transistor is 3.3 V, the maximum value of the supply voltage is about 4.3 V.

IV. Temperature Compensation

As a first approximation we can consider that the threshold voltage of an NMOS transistor decreases linearly with the temperature, as shown below,

$$V_{th}(T) = V_{th}(T_0) - K_{t1}(T - T_0) , \quad (8)$$

where K_{t1} is a BSIM3v3 coefficient that models the temperature dependence of the threshold voltage. In the case of the AMS 0.35 µm CMOS IC technology, such parameter is 0.33 mV/°C for an NMOS transistor and 0.45 mV/°C for a PMOS transistor. Let us define h as,

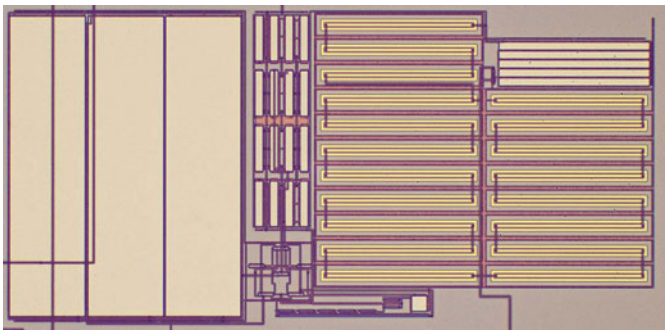

Fig. 2: Die Photograph (core).

$$h = Mm^2 \frac{W_4}{L_4}\left(\frac{N}{N-1}\right)\ln^2 \frac{W_2/L_2}{W_1/L_1}. \quad (9)$$

From (3), (4) and (9), and assuming that (5) is fulfilled, we can derive the following expression for the reference voltage,

$$V_{REF} = \left(1+\frac{R_1}{R_2}\right)\left(V_{th} + \sqrt{\frac{h}{W_8/L_8}}V_T\right) - V_{th} - \sqrt{\frac{h}{W_7/L_7}}V_T . \quad (10)$$

Differentiating (10) with respect to the temperature and taking into account (8), one obtains

$$\frac{\partial V_{REF}}{\partial T} = \left(1+\frac{R_1}{R_2}\right)\left(-K_{t1} + \sqrt{\frac{h}{W_8/L_8}}\frac{k_B}{q}\right) + + K_{t1} - \sqrt{\frac{h}{W_7/L_7}}\frac{k_B}{q}, \quad (11)$$

where k_B is the Boltzmann constant and q is the electron charge. Equating (11) to zero, we obtain

$$\frac{R_1}{R_2} = \frac{\sqrt{h}\frac{k_B}{q}\left(\frac{1}{\sqrt{W_8/L_8}} - \frac{1}{\sqrt{W_7/L_7}}\right)}{K_{t1} - \sqrt{h}\frac{k_B}{q}\frac{1}{\sqrt{W_8/L_8}}}. \quad (12)$$

Therefore, if (12) is satisfied, we obtain that the temperature coefficient (11) is zero for any temperature. It is clear that this is true within the approximation done in (8) and the simplified transistor characteristics expressions (1) and (2). Since the temperature dependence of the threshold voltage is not perfectly linear, a temperature dependent error will appear at the output of the reference voltage generator as we move away from the reference temperature at which the coefficient K_{t1} was computed.

Once the two transistors M_7 and M_8 are dimensioned for the minimum value of the bias current, given by (5), from (12) we can derive the ratio between the two resistance values, in order to achieve the best temperature compensation.

If we take into consideration an error in the resistor ratio R_1/R_2, from (11) it is clear that when the resistor ratio increases (decreases) with respect to its nominal value the temperature coefficient becomes positive (negative). Anyway, since in our design the value of the resistor ratio is much smaller than unity, an error on the resistance ratio is drastically reduced by summing it to 1 in (10). This allows us not to use trimming procedures.

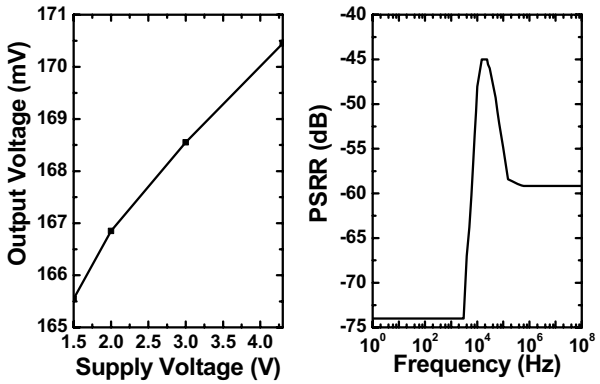

Fig. 3: Experiments: a) Output Voltage vs. Supply voltage at room temperature, b) PSRR at room temperature and for a supply voltage of 2 V.

V. Line Sensitivity

Because of the channel modulation effect, when the supply voltage varies, the bias current I_0 varies as well, causing the variation of the output reference voltage. By calculating V_{GS7} and V_{GS8} from (1) and substituting them in (4), we can derive the following expression for the output voltage,

$$V_{REF} = \left(1+\frac{R_1}{R_2}\right)V_{th8} - V_{th7} + \sqrt{MI_0}\left[\left(1+\frac{R_1}{R_2}\right)\sqrt{\frac{2}{k_8}} - \sqrt{\frac{2}{k_7}}\right]. \quad (13)$$

As shown in (13), only one term of the output reference voltage weakly depends on the bias current (via a square root). Furthermore, such term has a very small weight in (13), due to the fact that a variation of the bias current varies the gate-source voltages of M_7 and M_8 in the same direction, even if by a different amount; and, as can be better seen in (4), V_{REF} is obtained from the weighted difference of such two voltages, further suppressing the dependence on I_0 of the reference voltage.

VI. Experimental Results

The proposed voltage reference has been realized with a standard 0.35 µm CMOS process from AMS. The die photograph is shown in Fig. 2. Measurements show that the proposed voltage reference generates a mean reference voltage of about 168 mV with a variation of ±2.3 mV at room temperature when the supply voltage varies from 1.5 V to 4.3 V, as shown in Fig. 3a. Fig. 4 shows the output voltage dependence on temperature for different values of the supply voltage. The measured temperature coefficient at V_{DD}=2 V and V_{DD}=3 V is 25 ppm/°C and increases to 37 and 39 ppm/°C at V_{DD}=4.3 V and V_{DD}=1.5 V, respectively, corresponding to the maximum and minimum allowed supply voltage. At 80 °C the current drawn at the maximum supply voltage is 2.4 µA and at the minimum supply voltage is 1.5 µA. At room temperature,

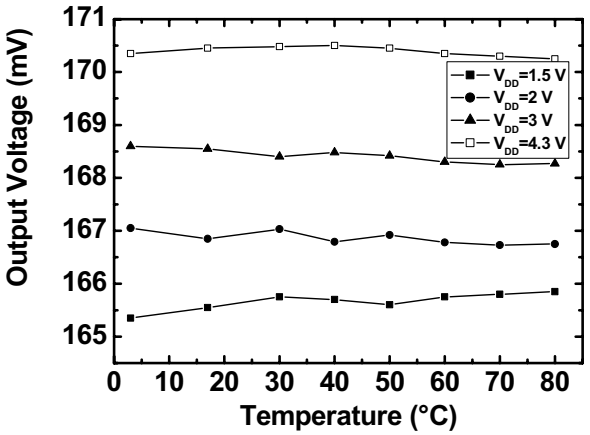

Fig. 4: Measured output voltage vs. temperature for 4 values of the supply voltage.

instead, the current drawn at the maximum supply voltage is 2.1 µA and at the minimum supply voltage is 1.2 µA. The power supply rejection ratio, without any filtering capacitor, is -65 dB at 100 Hz and -57 dB at 10 MHz, for the smallest supply voltage. At larger supply voltage the power supply rejection ratio increases to -74 dB at 100 Hz and to -59 dB at 10 MHz, as shown in Fig. 3b. The occupied chip area is 0.08 mm^2.

VII. Comparison with the State of the Art

A comparison with other voltage reference reported in literature is summarized in Table I. In such comparison only the solutions that can be implemented in a standard CMOS process are taken into consideration excluding the solutions that require technologies with low threshold voltage, native NMOS transistor, DTMOST or BiCMOS processes. From Table 1 it is possible to note that the proposed voltage reference has the smallest power consumption and the highest PSRR with a very good performance in terms of temperature coefficient. The occupied chip area and the line sensitivity are comparable to other solutions presented in literature.

VIII. Conclusion

A 25 ppm/°C voltage reference with a supply current of only 1.2 µA, at 1.5 V, has been presented. The proposed voltage reference has been implemented with a standard 0.35 µm CMOS process. The design conditions and possible optimizations have been studied in detail. Particular attention has been put at minimizing the power consumption, achieving at the same time very good PSRR and temperature compensation, without any trimming procedure, thanks to the suppression of the effects of mobility temperature dependence. The occupied chip area and the line sensitivity are comparable with other solution already reported in literature.

TABLE I: Comparison With Voltage Reference Generators Available in the Literature

	This work	Leung et al. [8]	Leung et al. [2]	Banba [9]
Technology	0.35 µm CMOS	0.6 µm CMOS	0.6 µm CMOS	0.4 µm CMOS
Supply Voltage (V)	1.5 to 4.3	1.4 to 3	0.98 to 1.5	2.2 to 4.4
Supply Current (µA)	1.5@1.5V 2.4@4.3V	<9.7	<18	>2.2
V_{ref}	168 mV	309.3mV	603 mV	515 mV
TC	25 ppm/°C	36.9 ppm/°C	15 ppm/°C	117 ppm/°C
Line Sensitivity	1.6 mV/V	0.26 mV/V	4.4 mV/V	1.1 mV/V
PSRR @100 Hz @10 MHz	V_{DD}=1.5V -65 dB -57 dB	V_{DD}=1.4 -47 dB -20 dB	V_{DD}=0.98 -44 dB -17 dB	N.A.
Chip Area (mm^2)	0.08	0.055	0.24	0.1

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