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Ultra-low power PSK backscatter modulator for UHF and microwave RFID transponders

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Ultra-low power PSK backscatter modulator for UHF and microwave RFID transponders

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Abstract

An integrated circuit implementation of a PSK backscatter modulator for passive radio frequency identification (RFID) transponders is proposed. Such modulator offers a significant reduction of the power consumption with respect to other schemes already presented in the literature. Furthermore, the topology of the proposed modulator allows us to control its output resistance so that only a negligible fraction of the active power at the antenna goes to the modulator.

Keywords: Backscatter modulation; Transponder; RFID; Low power

1. Introduction

RFID systems with passive transponders typically use modulation of the backscattered radiation for the downlink (transponder-to-reader) since it eliminates the need for the transponder to provide the power of the signal to be transmitted. Among possible backscatter modulations, BPSK allows the realization of a very simple transmitter, and is to be preferred even to ASK, since it ensures, for a given modulation depth, a larger power transferred to the transponder, that is the critical quantity limiting the range of passive systems [1]. Furthermore, such modulation allows constant power supply to the transponder.

The PSK backscatter modulation consists in modulating the imaginary part of the impedance seen by the antenna, in order to vary the phase of the reflected wave, and is usually obtained by varying a capacitive impedance. Few solutions have been presented in the literature [1,2] to perform a PSK backscatter modulation. The most important requirements for such modulators are low power consumption, since they are used in passive systems, and small area occupation on the chip to maintain their cost as low as possible. In this letter we present a PSK backscatter modulator with small power consumption and area compared to other modulator schemes presented in the literature.

2. Circuit description

The scheme of the proposed modulator is shown in Fig. 1. Transistor M_1 is a MOS varactor that operates in inversion or in cutoff, depending on the input signal, causing the variation of the capacitance seen at the output of the modulator. Transistor M_2, instead, does not affect the output capacitance, since it has a small width with respect to M_1, but determines the resistance at the output of the modulator, which is, essentially, its drain-source resistance. As a consequence, the channel length of M_2 has to be large enough so that the output resistance of the modulator is much larger than the antenna resistance. Such choice ensures that only a negligible fraction of the power at the antenna goes to the modulator, as required for the correct operation of the transponder. C_{OUT} is the capacitance seen at the output of the modulator and is due to the interconnections, the antenna and the input capacitance of the other stages which the modulator is connected to. As it will be clearer later, the capacitance C_{IN} has to be larger than the gate-source and gate-drain capacitance of M_1, in order not to degrade the variation of the output capacitance of the modulator. Once the value of C_{IN} is chosen, as previously described, the two transistors M_3 and M_4 of the inverter have to be dimensioned to fix the switching time of the varactor so that the channel bandwidth occupation of the backscattered signal complies with the requirements set by the standard. Referring to Fig. 1 and to the BSIM3v3

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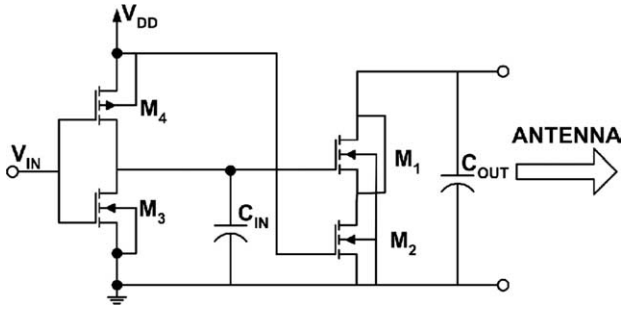

Fig. 1. Scheme of the proposed PSK backscatter modulator.

transistor model [3], the output capacitance, C_V, of the modulator is given by,

$$C_V = C_{DB} + C_{JD} + C_{JS} + C_{DM2} + (C_{GS} + C_{GD})||(C_{IN} + C_{GB} + C_{INV}), \quad (1)$$

where C_{XY} is the capacitance seen between the terminals X and Y of M_1, C_{JD} and C_{JS} are the drain–bulk and source–bulk junction capacitances, C_{DM2} is the capacitance seen from the drain of M_2 to ground, C_{INV} is the capacitance seen from the output of the inverter formed by M_3 and M_4. When the input signal varies, only the capacitances C_{GS}, C_{GD}, C_{DB} and C_{GB} vary, while the other capacitances remain constant. Thus, it is clear that, if C_{IN} is not sufficiently larger than C_{GS} and C_{GD}, the variation of the output capacitance is drastically reduced, since it predominantly depends upon the gate-source and gate-drain capacitances. In such condition, the variation ΔC of the output capacitance of the modulator can be well approximated as:

$$\Delta C \cong C_{DB} + (C_{GS} + C_{GD})||C_{IN} - (C_{GSov} + C_{GDov})||C_{IN} \quad (2)$$

where C_{GDov} and C_{GSov} are the overlap gate-drain and gate-source capacitances of M_1. Referring to Fig. 1, in each period of the input signal, since the drain and the source of M_1 are always pulled down to ground, we do not need to charge and discharge the output capacitance and the equivalent drain-ground and source-ground capacitances. Thus, the power P_{MOD} dissipated by the modulator is given by:

$$P_{MOD} \cong (C_{GS} + C_{GD} + C_{IN}) f V_{DD}^2 \quad (3)$$

From (2) it is clear that the choice $C_{IN} >> C_{GS} + C_{GD}$ maximises the modulation depth but leads to a high power consumption when modulating. Since in passive RFID systems it is very important to maintain the power consumption as small as possible, the value of the capacitor C_{IN} has to be chosen as to minimize the power consumption for a given modulation depth. Since all the capacitances of M_1 are proportional to the channel width, W, of M_1, therefore from (2), for a given modulation depth, we can derive $W(C_{IN})$. Substituting such relation in (3) and deriving the power with respect to C_{IN}, we can find the value of C_{IN} that allow us to minimize the power consumption and that ensures the modulation depth previously fixed.

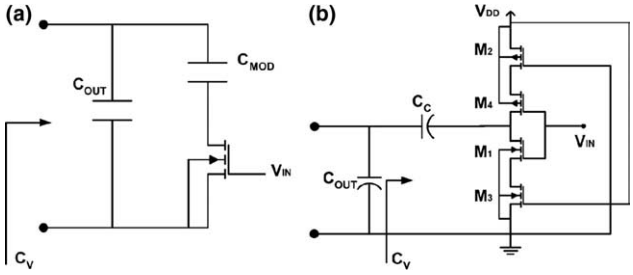

Fig. 2. Schemes of the comparison PSK backscatter modulators: (a) from [2]; (b) modified from [1].

3. Comparison with other topologies

Now, we can compare the performances of the proposed modulator with that of two other schemes appeared in the literature, on the basis of an implementation with a typical 0.35 μm CMOS process from AMS, and a supply voltage of 0.6 V, compatible with subthreshold operation of the digital section. In the modulator shown in Fig. 2a [2], the capacitor C_{MOD} is dimensioned to obtain the desired variation ΔC of the output capacitance. The great disadvantage of such scheme is the area occupation on the chip, especially when a very low supply voltage is used, as can happen in passive RFID systems. From Fig. 3 it is possible to verify that the area occupation on the chip of the modulator, shown in Fig. 2a, is much larger than that one of the proposed modulator. The modulator shown in Fig. 2b is a modified version of that proposed in [1]: here the modulation is obtained by exploiting the output capacitance of the inverter formed by M_1 and M_4 rather than the capacitance of a varicap placed between the input and the output of the inverter, as done in [1]. In such a way, although the operation principle is not changed, we have a reduced number of components (two inverters and one of the two coupling capacitors are removed) and therefore a reduced power consumption and area occupation for the same modulation depth. Anyway, also with such improvement, the modulator shown in Fig. 2b occupies an

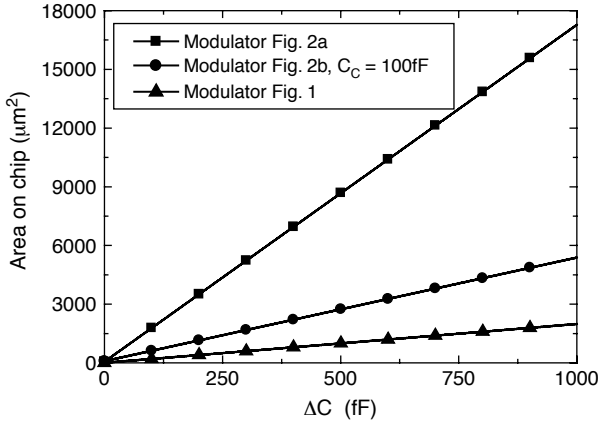

Fig. 3. Area occupation on the chip vs. modulation of the output capacitance ΔC.

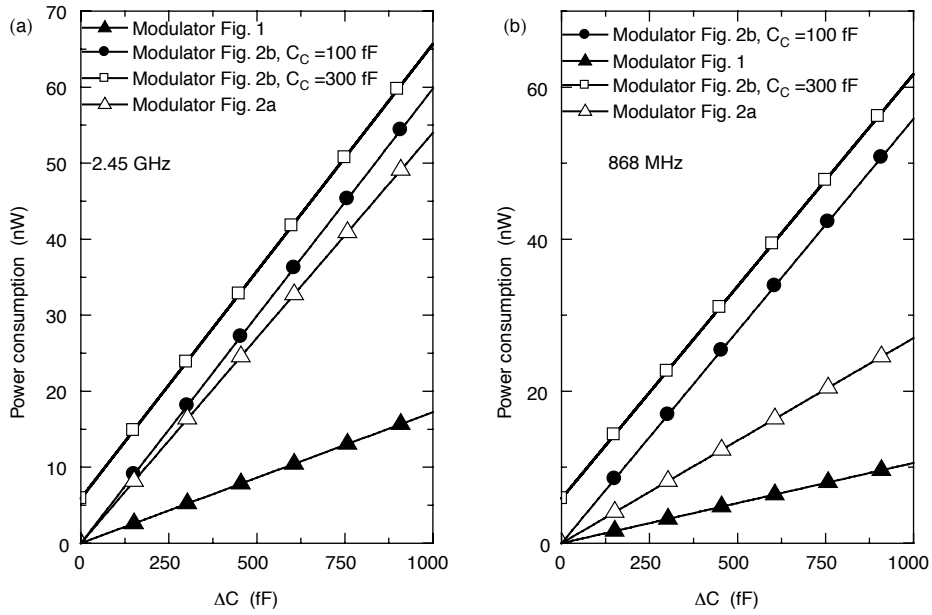

Fig. 4. Power consumption of modulators shown in Figs. 1 and 2 vs. the variation of the output capacitance for an operating frequency of 2.45 GHz and 868 MHz.

area on the chip between two and three times larger than our modulator, as can be seen in Fig. 3. In such modulator transistors M_1 and M_4 determine the output capacitance while M_2 and M_3 allow us to increase the output resistance of the modulator. In order to obtain a given modulation of the output capacitance and minimum area occupation, M_1 must have minimum width while M_4 is dimensioned to obtain the desired ΔC. Transistors M_2 and M_3 have minimum width, in order to obtain a large output resistance in both states. The great disadvantage is that the capacitance seen at the output of the modulator has to be charged and discharged in each period of the input signal; as a consequence the power consumption for a given variation of the output capacitance of the modulator shown in Fig. 2b is much larger than that of the proposed modulator, as can be seen in Fig. 4. Similar conclusions are drawn also from comparison at higher supply voltages.

The choice of ΔC must be done in order to maximize the operating range, achieving a trade off between minimum probability of error at the reader and maximum power transfer to the transponder. Analysis show that a range of 4 m can be achieved at 2.45 GHz with $\Delta C = 130$ fF and a range of 10.5 m can be achieved at 868 MHz with $\Delta C = 174$ fF, for a data rate of 40 kbps and a DC power consumption of the transponder of 1 μW [4].

4. Conclusion

An ultra-low power PSK backscatter modulator for long range passive RFID systems has been proposed. It can be fully integrated, using a low-cost CMOS IC technology, with a smaller area occupation and power consumption with respect to other solutions proposed in the literature.

Acknowledgements

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