Ultra-Low-Power Series Voltage Regulator for Passive RFID Transponders with Subthreshold Logic

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A series voltage regulator for long-distance passive microwave RFID (RadioFrequency IDentification) transponders, based on subthreshold CMOS circuits, is presented. It is shown that for a voltage regulator that supplies power to subthreshold circuits, temperature compensation would actually represent a disadvantage, while a proper built-in nonzero temperature coefficient can strongly suppress the temperature dependence of the overall subthreshold circuit performance. Implementation and experimental results are discussed.

Introduction: Long-range passive microwave transponders ('tags') for RFID systems do not have an on-board battery and therefore must draw the power required for their operation from the electromagnetic field transmitted by the reader [1]. The practical adoption in the commercial arena of passive UHF and microwave RFID transponders for identification and ambient intelligence applications [2] is strongly affected by their operating range, which is determined by the maximum power transmitted by the reader, limited by European regulations to just 500 mW, and by the power at the transponder antenna required for its operation. A focused effort in the attempt to drastically reduce power consumption of the transponder to few µW is therefore required to achieve operating ranges of several metres [3]. For such reason, the digital section is a finite state machine implemented in subthreshold 0.35 µm CMOS logic with a supply voltage of 0.6 V. Therefore, the voltage regulator must be able to supply a DC power of only few µW and must have a very small quiescent current, in the order of few tens of nA. The voltage regulator has a negative temperature coefficient to compensate the temperature dependence of the subthreshold current, ensuring that the current in the logic gates, and therefore the delays and the power consumption of the subthreshold logic circuits, and the frequency of the clock generator, are practically independent of temperature.

Circuit description: The schematic of the reference voltage generator is shown in Fig. 1. It consists of a circuit that generates a current I_0 almost independent of the supply voltage, which is in turn injected into a diode, to generate the reference voltage [4]. By assuming identical currents in the two branches, the current I_0, in Fig. 1, reads,

$$I_0 = \frac{2}{R^2}\left(\frac{1}{\sqrt{k_1}} - \frac{1}{\sqrt{k_2}}\right)^2 \tag{1}$$

where $k_i = \mu C_{ox} W_i / L_i$ for transistor M_i (integer i), μ is the mobility, C_{ox} is the oxide capacitance per unit area, W_i and L_i are the channel width and length of M_i, respectively. When considering the channel length modulation effect of M_1 and M_2, the relative variation of the current I_0, when V_{DDhigh} varies between its minimum value $V_{DDhighMIN} = 1.5$ V and its maximum value $V_{DDhighMAX} = 6.3$ V can be well approximated by

$$\frac{\Delta I_0}{I_0} = \lambda \frac{V_{DDhighMAX} - V_{DDhighMIN}}{\sqrt{k_2/k_1} - 1} \tag{2}$$

where λ is the channel length modulation coefficient. From (2) we notice that in order to have a small dependence of the current I_0 on the supply voltage and therefore a small PSRR the ratio k_1/k_2 cannot be too close to 1 and the channel length is determined by the desired value of λ. On the other hand, the ratio k_1/k_2 cannot be too small, otherwise from (1) an excessively large resistance R would be required to have a small I_0. A good trade-off is found by setting $k_1/k_2 = 0.5$ and $R = 2$ MΩ. Since the reference voltage generator has two stable states, corresponding to the current given by (1) and to zero current, a start-up circuit (formed by M_{1S}-M_{3S}) is used to ensure that the former is reached. The series voltage regulator consists of a PMOS differential amplifier that compares the output voltage with the reference voltage and provides an error signal driving the gate of the NMOS transistor M_U, in order to keep the output voltage equal to the reference voltage [5, 6]. The voltage V_{DDlow} is generated by a single stage voltage multiplier. To ensure the correct operation of the voltage regulator, a supply voltage V_{DDlow} few tens of mV larger than V_{REG} is sufficient. However, such voltage would not be sufficient to ensure the correct operation of the error amplifier and to generate the reference voltage V_{REF}. As a consequence, in the voltage multiplier, a second stage is added to generate the higher voltage V_{DDhigh} that has only to provide the very small power required for the error amplifier and the voltage reference generator. In such a way, power efficiency can be maximised [3]. Stability is a critical aspect for such kind of circuits, especially in the case of small load current when the pole associated with the output node, given by g_{mu}/C_u, could become comparable with the pole at the output of the differential amplifier. As a consequence, frequency compensation is required, and is obtained by placing a capacitance C_C of 50 pF at the output of the differential amplifier. In such a way, the pole associated with the capacitance C_C is about 70 Hz and is more than two orders of magnitude lower than the output pole for a load current one hundredth of the maximum value (5 µA), ensuring a dominant pole behaviour. The temperature coefficient of the output regulated voltage is about -2 mV/°C, given by the *p-n* junction used to generate the reference voltage. As will be clearer later, such temperature coefficient allows us to keep the performance of digital subthreshold circuits almost constant when temperature is varied. To validate such an approach we consider a ring oscillator implemented with three NAND gates in subthreshold CMOS logic and compare the performance obtained when the circuit is supplied by a DC voltage $V_{DD} = 0.6$ V, independent of temperature (Fig. 2*a*), with that obtained when it is supplied by the proposed voltage regulator (Fig. 3*b*).

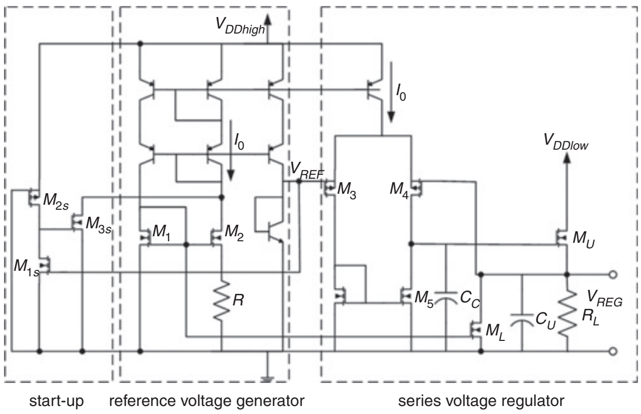

Fig. 1 *Schematic of voltage regulator*

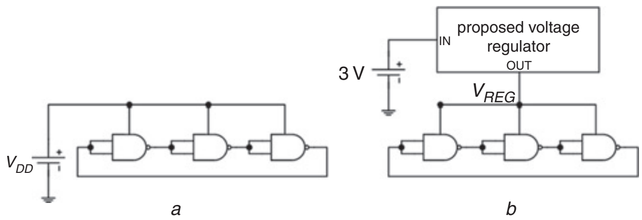

Fig. 2 *Ring oscillator supplied by temperature independent supply voltage and ring oscillator supplied by proposed voltage regulator*

a Supplied by temperature independent supply voltage
b Supplied by proposed voltage regulator

Experimental results: The proposed voltage regulator has been successfully implemented in AMS 0.35 µm BiCMOS. The die photograph is shown in Fig. 3. The measured performance is summarised in Table 1. The minimum drop-out voltage at the maximum output current of 5 µA is only 30 mV and the quiescent current is 34 nA. The oscillation frequency of the two circuits of Figs. 2*a* and *b* is plotted against temperature in Fig. 4. For the circuit of Fig. 2*a* the oscillation frequency has a large relative variation with temperature of about 4%/°C and the power consumption has the same relative variation of about 4%/°C. In the case of Fig. 2*b*, the oscillation frequency has a very small dependence on the temperature of only -0.08%/°C and the power consumption has a relative variation of about -0.74%/°C. As can be seen, the use of our non-compensated voltage regulator ensures an overall temperature compensated performance of the subthreshold circuit.

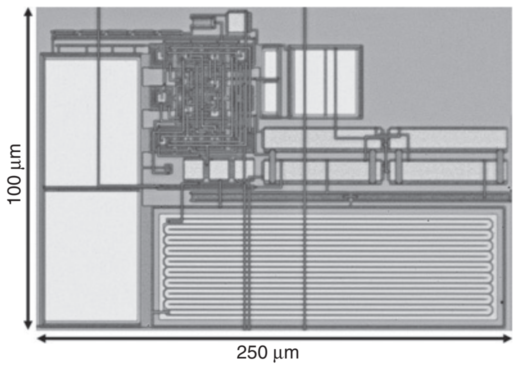

Fig. 3 *Die photograph (core)*

Table 1: Performance summary of proposed voltage regulator

Output voltage	605 mV
Maximum output current	5 µA
Quiescent current	34 nA
Line sensitivity	±0.8 mV/V
DC output resistance	100 Ω
PSRR at DC (RF)	−58.5 dB (−54 dB)
Load current pulse settling time (0 → 5 µA)	480 µs with $\Delta V_{REG} = 45$ mV
Supply voltage pulse settling time (0 → 3 V)	1.5 ms
Temperature coefficient	−2 mV/°C
Chip area	0.025 mm^2

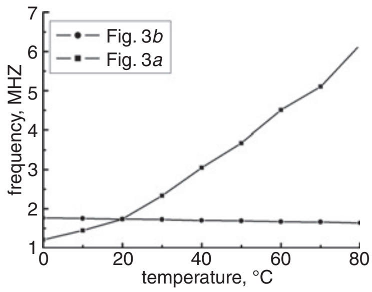

Fig. 4 *Oscillation frequency against temperature for ring oscillators of Fig. 3*

Conclusion: A series voltage regulator for UHF and microwave passive RFID transponders with a subthreshold digital section is presented and its design constraints and criteria are described. Experiments confirm that it provides a very low regulated voltage, extremely low quiescent power consumption, and a very good PSRR at DC and RF. The designed regulator can be used as a power supply of CMOS circuits operating in subthreshold or weak inversion also beyond the case of RFID systems.

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