Università di Pisa

Silicon-on-insulator non-volatile memories with second-bit effect

Luca Perniola
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni,
Università di Pisa and IMEP-ENSERG, Grenoble
Giuseppe Iannaccone
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni,
Università di Pisa

L. Perniola, G. Iannaccone, *Silicon-on-insulator non-volatile memories with second-bit effect*, Journal of Computational Electronics, **5**, 3, pp.137-142 (2006).

J Comput Electron (2006) 5:137–142
DOI 10.1007/s10825-006-8833-2

Silicon-on-insulator non-volatile memories with second-bit effect

L. Perniola · G. Iannaccone

© Springer Science + Business Media, LLC 2006

Abstract In this paper we propose an analytical approach to investigate the electrostatic impact of very small charged regions in the gate dielectric of dual bit non-volatile memories (NVMs) Silicon-On-Insulator (SOI) cells. This original model is based on the surface potential approach and allows to investigate the behavior of NVMs in subthreshold working condition. It is particularly accurate for charged region, as small as $L_2 = 10$ nm and up to a charge density of $Q = 10^{13}$ cm^{-2} and it is complementarity to another approach proposed for bulk devices [1]. Relevant consequences of the asymmetric charging of the storage layer on the electrical characteristics of discrete-trap memories are thoroughly analyzed: the importance of Short Channel Effects (SCEs) for the performance of these cells is highlighted. Moreover a method for extracting an "effective" distribution of charges from the transfer characteristics is derived.

1. Introduction

Non-uniform injection in discrete-trap memories has recently attracted much attention in the literature for the possibility of encoding more than one bit for each memory cell. Channel Hot Electron (CHE) is typically used as a non-uniform injection mechanism, where, electrons are injected near the drain in the trapping medium, which can consist of an amorphous layer as in NROM [2] and SONOS [3], or of a nanocrystal layer [4].

Due to the non-uniform distribution of injected charges, the threshold voltage of the cell depends on the reading procedure applied. If the drain is positively biased and the source is kept grounded (i.e., we perform a *forward* reading, $V_{ds} > 0$), the electrostatic effect of trapped electrons on the channel is neutralized by the pinchoff region near the drain junction and the current is only poorly affected. On the other hand, if the source is positively biased and the drain is kept grounded (i.e., we perform a *reverse* reading, $V_{ds} < 0$) the electrostatic effect of trapped charge on the channel is much larger, therefore the drain current is more strongly suppressed. As a consequence, the threshold voltage during forward read, V_{th-F}, is lower than the threshold voltage during reverse read, V_{th-R} [5, 6].

Another important consequence of such non-uniform charge distribution, often highlighted in the literature [5–7], is the *subthreshold slope degradation*, clearly visible in both reading conditions for small V_{ds} (order of hundreds of mV), or only in reverse read for larger V_{ds} (few *V*). Such effect is visible if the charged portion of the cell is comparable to or smaller than the thickness of the gate stack.

Here we are able to provide a complete analytical description of the surface potential and of the electrical characteristics I_{DS}-V_{GS} in subthreshold, with only one *physically-based* parameter. The main results of this new model are validated through comparison with detailed numerical simulations performed with a 2D-TCAD package (ATLAS from Silvaco [8]).

L. Perniola (✉)
Università degli Studi di Pisa, Dipartimento di Ingegneria dell'Informazione, Via Caruso 16, 56122, Pisa, Italy, and IMEP-ENSERG, Avenue des Martyrs 32, 38016 Grenoble, France

G. Iannaccone
Università degli Studi di Pisa, Dipartimento di Ingegneria dell'Informazione, Via Caruso 16, 56122, Pisa, Italy and IEIIT-CNR, Via Caruso 16, 56122, Pisa, Italy

2. Analytical model

Our study is based on the computation of the profile of the surface potential Ψ_S along the active channel. It is of paramount

importance to reproduce the 2D behavior near the junctions, as they are the regions where trapped charges in the dielectric have the most impact. First, our model computes the surface potential profile of the fresh cell, then it adds the impact of the charges as a second step. Such approach is applicable if the Poisson equation is linear in the active channel, i.e. when the mobile charge is negligible with respect to the fixed charge. As a consequence, we shall see that this model provides reliable results when the device is in subthreshold condition or in weak inversion, and has an increasing error as the mobile charge becomes significant. The model is particularly suited to very small charged region, where the gate voltage sweep in subthreshold can be performed without inducing a significant inversion layer under the uncharged portion of the cell. This model is clearly complementary to our work of Ref. [1], which was suitable for larger charged regions.

We have made the assumption that the trapped charge is uniform in a localized region of the trapping medium next to the drain contact, while the region over the rest of the channel is free of charges. We believe that the simplified step-function distribution allow us to understand the programming behavior in terms of two effective parameters, such as the *effective charged length* L_2 and the *effective charge density* Q.

2.1. Fresh cell

The surface potential behavior along the channel can be computed as described in Ref. [9]. Here we briefly review the procedure to obtain the analytical expression of Ψ_S for SOI cells. The way to find an analytical expression of the surface potential Ψ_S along the active channel (y-direction), is to write the flux of the electric field through the faces of an ideal box delimited by the front and back Si/SiO$_2$ interfaces. We make the hypotheses of fully depletion and null electric field at the back interface, because the buried oxide is much thicker than the silicon film, then the main differential equation reads:

$$\epsilon_{si}\frac{t_{si}}{\eta}\frac{d^2\Psi_S(y)}{dy^2}+\epsilon_{ox}\frac{V_g-V_{fb}-\Psi_S(y)}{t_{eox}}=qN_{sub}t_{si}. \quad (1)$$

The boundary conditions are $\Psi_l = V_{bi} + V_s$ and $\Psi_r = V_{bi} + V_d$, where V_{bi} is the built-in voltage at the *pn* junctions between the silicon film and drain and source contacts, V_s is the source voltage, and V_d is the drain voltage. In (1), $\epsilon_{si}(\epsilon_{ox})$ is the dielectric constant of the silicon (oxide), t_{si} is the silicon film thickness in a SOI cell, η is the only fitting parameter, V_g is the gate voltage, V_{fb} is the flat band voltage of the fresh cell, t_{eox} is the equivalent oxide thickness, q is the absolute value of the electron charge, N_{sub} is the doping level of the SOI channel. The solution of (1) is a linear combination of hyperbolic sines:

$$\Psi_S(y)=(\Psi_r-\Psi_L)\frac{\sinh(y/\lambda)}{\sinh(L/\lambda)}+(\Psi_l-\Psi_L)\frac{\sinh[(L-y)/\lambda]}{\sinh(L/\lambda)}+\Psi_L. \quad (2)$$

The reference potential is the flat-band voltage. Ψ_L is the long channel surface potential, i.e. the surface potential value of the corresponding large MOS capacitor, while λ is the *natural length* involved in the problem:

$$\Psi_L = V_g - V_{fb} \pm \frac{qN_{sub}t_{si}}{C_{ox}} \quad (3)$$

$$\lambda \equiv \sqrt{\frac{\epsilon_{si}t_{eox}t_{si}}{\epsilon_{ox}\eta}}. \quad (4)$$

where in (3) the plus sign is referred to depleted-mode SOI cells, while the minus sign is referred to enhancement-mode SOI cells, C_{ox} is the oxide capacitance per unit area.

Clearly λ is a crucial parameter to describe Short Channel Effects (SCEs), as it describes the influence of the *pn* junctions at the source and drain terminals on the behavior of Ψ_S. The higher the value of λ, the weaker is the coupling between gate and channel, the higher is the difference between V_{th-for} and V_{th-rev}. We understand from this analytical approach that SCEs are vital for the dual-bit performance, bacause if we drastically reduce SCEs, we would reduce λ and the forward/reverse reading of a charged cell would not be clearly detached. The parameter λ is influenced by the choice of η, and the physically-based method to chose the value of η is based on the comparison of the surface potential behavior obtained from the numerical simulation with that obtained from the analytical model. Let us highlight that such a value is evaluated only once, for the fresh cell, and is valid for all values of L_2 and Q of the charged region.

2.2. Electrostatic effects of the trapped charge

As a second step, the electrostatic effect of charges is considered via the superposition principle. Indeed, when the overall channel is under weak inversion, the amount of mobile charge is so small that the Poisson equation can be considered linear. We stress the fact that the region of the channel under the uncharged dielectric goes in strong inversion before the region under the trapped charges. This affects seriously the results in the sense that the analytical results are accurate only if the gate voltage is so low that the channel is safely depleted. As plotted in Fig. 1, in the 2D sample structure the impact of one ideally infinite charged line is integrated along the vertical direction x, and longitudinal direction y, and results in a

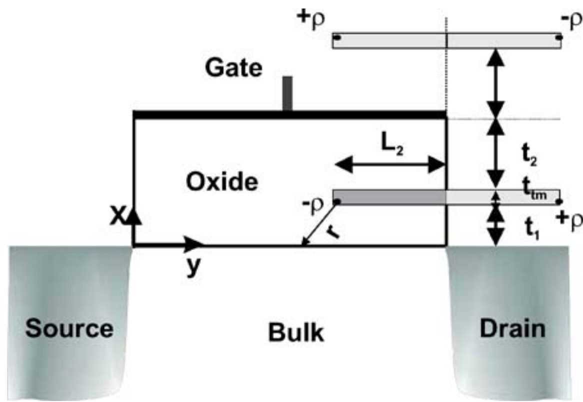

Fig. 1 Plot of the actual and image charges to be considered for the calculation of the surface potential Ψ_{Stot}, caused by the presence of the drain junction and the gate contact: they are considered as infinite plates of metal. The image charges highlighted in this plot would be considered in any simple bulk structure

perturbative potential Ψ_{Sp} of the following type [10]:

$$\Psi_{Sp}^{(A)}(y) = -\frac{\rho}{\pi\epsilon_0(\epsilon_{si}+\epsilon_{ox})}\int_{L_1}^{L_1+L_2} d\tilde{y} \cdot \int_{t_1}^{t_1+t_{tm}} \ln(\sqrt{(y-\tilde{y})^2+x^2})dx, \tag{5}$$

where t_{tm} is the trapping medium thickness, ρ is the density of injected charge per unit volume and the apex A refers the integration to the actual pocket of charge. Equation (5) has a closed form solution. The boundary conditions of the Poisson equation are simplified as shown in Figs. 1 and 2,

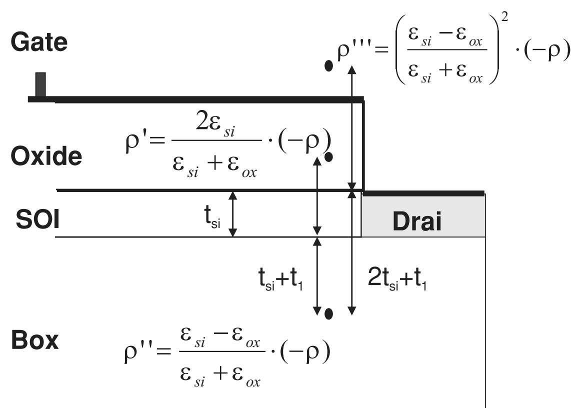

Fig. 2 Plot of the actual and image charges to be considered for the calculation of Ψ_{Stot} due to the presence of the front and back interfaces Si/SiO_2. In principle we have to consider an infinite number of charges, but the series is truncated to the first three terms. ρ' is the charge due to the top Si/SiO_2 interface [10]; ρ'' is the imaged charge of ρ', due to the presence of the bottom Si/SiO_2 interface; ρ''' is the imaged charge of ρ'' due to the presence of the top Si/SiO_2 interface. The image charges due to the metal contacts at the gate and at the drain are omitted, but they follow the same criterion of Fig. 1. ($[\rho] = C/cm^3$, absolute value of injected charge)

and can be taken into account by a proper configuration of image charges. The gate and drain contacts can be considered as perfect metals, and force Dirichlet boundary conditions, therefore the "real" charges must be suitably mirrored as indicated in Fig. 1. The Si/SiO_2 front and back interface of an SOI cell cause a change of permittivity from ϵ_{ox} to ϵ_{si} and this effect multiplies each pocket evidenced in Fig. 1 by three other pockets, as highlighted in Fig. 2 [10]. The two parallel interface planes would require an infinite series of image charges in the vertical direction, however only the three closest are considered. To keep Fig. 2 readable, we do not show the series of charges imaged by the gate and the drain (that are included in the calculations). Every pocket of charge plotted in Figs. 1 and 2 has an integral equivalent to (5) to be analytically solved.

After calculating the perturbative potential, the surface potential is:

$$\Psi_{Stot} = \Psi_S + \Psi_{Sp}, \tag{6}$$

2.3. Drain current

In this section, we derive a simple expression for the drain current of depletion n-MOS SOI devices as a function of the surface potential, on the basis of reasonable assumptions. The electron concentration in the silicon film is [11]:

$$n(x, y) = N_{sub}\exp\left(\frac{q(\Psi_{tot}(x, y) - V(y))}{KT}\right), \tag{7}$$

where $V(y)$ is the quasi-Fermi energy for electrons in the channel. Due to the fully depleted body, the band bending of the silicon film (see Fig. 3) is maximum at $qN_{sub}t_{si}^2/(2\epsilon_{si})$.

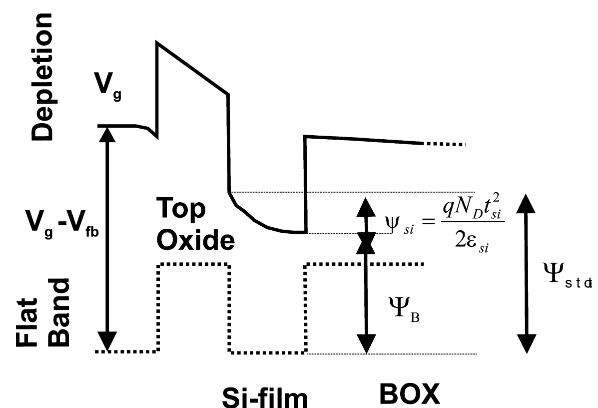

Fig. 3 Qualitative plot of the energy band bending in depletion mode SOI devices. The surface potential Ψ_S is computed with respect to the flat band condition. The silicon film is supposed to be fully depleted and the electric field at the back face is believed to be zero. The enhancement-mode SOI band diagram, omitted, is similar and relies on the same hypotheses

As a consequence, the surface potential Ψ_S is the sum of the contribution due to the silicon film and the rigid translation of the potential at the back-face Ψ_B. Moreover, if we make the hypothesis of negligible electric field at the back Si/SiO$_2$ face (already used in (1)) we obtain:

$$\Psi(x, y) = \Psi_B(y) - \frac{q N_{sub} x^2}{2\epsilon_{si}}. \tag{8}$$

In order to find the charge per unit area, Q_{inv}, at the top Si/SiO$_2$ surface, we integrate the electron concentration along the vertical x coordinate:

$$Q_{inv}(V) = \int_0^{t_{si}} q N_{sub} \exp\left(\frac{q(\Psi(x) - V)}{KT}\right) \mathrm{d}x \tag{9}$$

The drain current is then found integrating on the quasi-Fermi energy level, bearing in mind that in subthreshold Ψ_S is a function of the gate voltage and not of the quasi-Fermi energy level V:

$$\begin{aligned} I_{DS} &= \mu_{eff} \frac{W}{L} \int_0^{V_{ds}} Q_{inv}(V) \mathrm{d}V \\ &= KT \mu_{eff} N_{sub} \frac{W}{L} \frac{\sqrt{\pi} \cdot \mathrm{Erf}\left(\sqrt{\frac{q^2 N_{sub}}{2\epsilon_{si} KT}} t_{si}\right)}{2\sqrt{q^2 N_{sub}/(2\epsilon_{si} KT)}} \\ &\quad \cdot \exp\left(\frac{\Psi_{Smin} + \frac{q N_{sub} t_{si}^2}{2\epsilon_{si}}}{KT/q}\right)\left(1 - \mathrm{e}^{\frac{-qV_{ds}}{KT}}\right). \end{aligned} \tag{10}$$

where μ_{eff} is the effective mobility of electrons in the channel, n_i is the intrinsic electron concentration, W and L are the width and the length of the cell. A similar reasoning can be followed for the derivation of the drain current in a enhancement-mode n-MOS SOI cell:

$$\begin{aligned} I_{DS} &= KT \mu_{eff} \frac{n_i^2}{N_{sub}} \frac{W}{L} \frac{\sqrt{\pi} \cdot \mathrm{Erfimm}\left(\sqrt{\frac{q^2 N_{sub}}{2\epsilon_{si} KT}} t_{si}\right)}{2\sqrt{q^2 N_{sub}/(2\epsilon_{si} KT)}} \\ &\quad \cdot \exp\left(\frac{\Psi_{Smin} - \frac{q N_{sub} t_{si}^2}{2\epsilon_{si}}}{KT/q}\right)\left(1 - \mathrm{e}^{\frac{-qV_{ds}}{KT}}\right), \end{aligned} \tag{11}$$

where Erfimm is the immaginary error function.

2.4. Domain of validity of the analytical model

We will focus on very small charged region, and will perform the analysis for very low V_g, when the channel is in subthreshold or weakly inverted. The behavior of the transfer characteristics at very low values of V_g can be extrapolated to higher values of I_{DS}. It must also be mentioned that in reverse read the body effect enhances the value of the threshold voltage of the region free of trapped charge, and this allows us to obtain from the model reliable results especially on reverse I_{DS}-V_{GS} in a wider region of gate voltages.

Provided this issue on the Poisson solution, we exploit this new model in a domain of charged length smaller than $\sim$70 nm.

In order to assess the viability of this model, the 2D numerical TCAD tool ATLAS has been used [8]. The device under investigation is an idealized typical NROM depleted-mode SOI device. The width and length of the cell are 0.16 and 0.28 μm respectively, drain and source n-doping is at $N_d = 10^{20}$ cm^{-3}, the n-channel doping is $N_{sub} = 10^{18}$ cm^{-3}, the bottom oxide thickness is $t_1 = 7$ nm, the top oxide thickness $t_2 = 9$ nm. Concerning the trapping layer, for the sake of simplicity, we have considered an SiO$_2$ layer $t_{tm} = 3.6$ nm, equivalent, from an electrostatic point of view, to a layer of silicon nitride of 7 nm. The silicon film thickness $t_{si} = 18$ nm, while $t_{BOX} = 400$ nm is the buried oxide thickness, which is large enough to reduce the coupling effect from the bulk. From TCAD simulations, it has been verified that the electric field at the back face is negligible. In Fig. 4 we compare TCAD and analytical results for $L_2 = 17.5$ nm, $L_2 = 35$ nm and $Q = 7 \times 10^{12}$ cm^{-2} (case A) and 1.4×10^{13} cm^{-2} (case B). A strong degradation of the subthreshold slope during reverse reading is apparent.

Another issue, typical of this kind of depletion mode devices, appears in the low-V_g region of the reverse

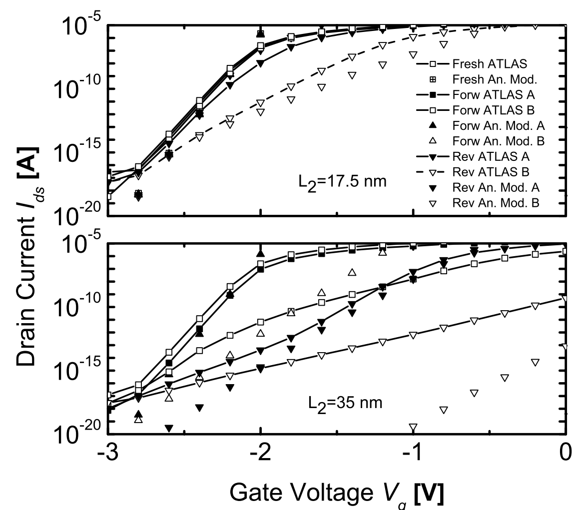

Fig. 4 Comparison between numerical and analytical results on the I_{DS}-V_{GS} characteristics for a depleted-mode SOI device whose features are defined in Section 2.4. The distribution of charge has $L_2 = 17.5$ nm (upper plot) and $L_2 = 35$ nm (lower plot) and $Q = 7 \times 10^{12}$ cm^{-2} (case A) 1.4×10^{13} cm^{-2} (case B). While in the upper plot we have a fine agreement between the analytical and the numerical results; in the lower plot the parasitic effect, due to the inability of the gate to pinchoff the channel, strongly degrades the drain current. For $Q = 7 \times 10^{12}$ cm^{-2} a fine agreement with the numerical results exists for high value of V_g, for $Q = 1.4 \times 10^{13}$ cm^{-2} the slope is completely lost. Such effect is not considered in our model

characteristic. If the channel is strongly doped, the gate voltage is not able to pinchoff completely the channel with low V_g values (i.e. incomplete depletion), because the concentration of minority carriers becomes comparable to the doping level and reduces the gate coupling to the channel [12]. In this case the drain current is weakly driven by the gate and the subthreshold slope is highly degraded (see results in Fig. 4 for very low value of the gate voltage). This problem is even more pronounced by raising the level of injected charge in the trapping medium. For this reason the maximum charge density for which our model is applicable to SOI devices is about 10^{13} cm^{-2}. In the case of enhancement-mode SOI cells, through the comparison with numerical result, we have deduced an identical safe maximum limit for the concentration of trapped charges.

3. Contour plot of ΔV_{th-tot} and S with respect to L_2 and Q

In the previous section, the behavior of the forward read transfer characteristics has not been mentioned. Given that the present model is tailored specifically for very short charged length L_2, the forward read would provide an I_{DS}-V_{GS} curve basically identical to that of a fresh cell.

With the help of this model, we can concentrate, indeed, on the behavior of the subthreshold slope and on the behavior of the total threshold voltage shift, focusing on the transfer characteristics of the fresh cell and of the written cell in the reverse read.

In Fig. 5 we provide two contour plots of ΔV_{th-tot} and S with respect to L_2 and Q. From experiments we can have information on the threshold voltage in the fresh read ($V_{th-fresh}$), reverse read (V_{th-R}) and the value of the subthreshold slope factor S. We identify one cross point on the map of Fig. 5 and we deduce the features of the effective charge distribution trapped near the drain, L_2 and Q. As we can see, in order to have a clear degradation of the subthreshold slope in reverse read, we need to inject a localized pocket of charge as small as $L_2 = 30-40$ nm and with $Q \gtrsim 5 \times 10^{12}$ cm^{-2}. On the other hand, if L_2 becomes large, the subthreshold slope gains the value of the fresh cell and also $V_{th-for} \approx V_{th-rev}$.

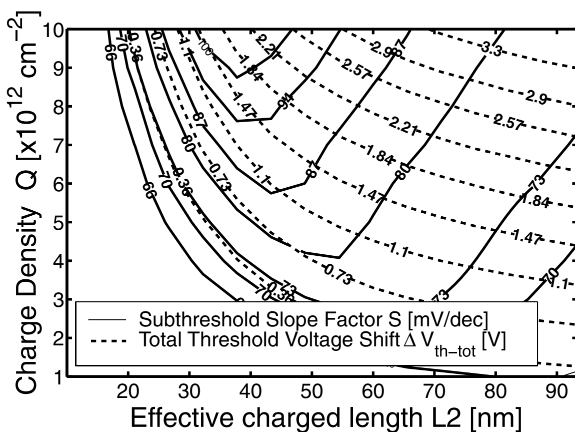

Fig. 5 Contour plots of ΔV_{th-tot} (dashed line) and S (solid line) as a function of the effective charged region L_2 and the density of charge Q. Features of the cell are those mentioned in Section 2.4, $|V_{ds}| = 1.5$ V. From the experimental data, we find the cross point between ΔV_{th-tot} and S values, and we are able to extract information on the charge distribution injected in the trapping medium through L_2 and Q

In order to test the validity of such map, we have compared results from our model with numerical simulations. We have extracted from the map Q and L_2, for some ΔV_{th-tot} and S, and used them in the 2D TCAD simulator to see if simulated electrical characteristics are in agreement with the given values of ΔV_{th-tot} and S. The results of such comparison are in fine agreement, confirming the validity of our model.

4. Conclusion

We have presented an analytical model that provides a simple electrostatic view of dual-bit memory electrical behavior in SOI depleted-mode and enhancement-mode cells. The reverse mode read and forward mode read of a programmed cell with non-uniform distribution of injected charge are analytically computed. The main issues such as the higher threshold voltage in reverse read than in forward read, the subthreshold slope degradation in reverse read and the importance of SCEs for dual-bit performance are all successfully addressed. In particular, the subthreshold slope degradation is caused by a very small pocket of charge with very high density of charge. The overall reasoning needs only one physically-based η parameter, which depends on the features of the fresh cell and is completely independent of the effective distribution of the pocket of charge. The proposed model complements the range of validity of the approach presented in [1], as it pushes the limits of the analysis to a distribution of charges with $L_2 \lesssim 10$ nm.

We consider this model as an effective tool for the comprehension of dual-bit memory behavior of non-volatile memories such as SONOS, NROM or nanocrystal.

Acknowledgments This work was partly supported by the EU through the ADAMANT Project (IST-2001-34234) and the Network of Excellence “SINANO” (IST-506844), and by the Italian National Research Council (CNR) through the FIRB project “Sistemi miniaturizzati per elettronica e fotonica”.

The authors thanks G. Ghibaudo from IMEP/CNRS (Grenoble), B. De Salvo and G. Molas, from CEA/LETI (Grenoble), for helpful discussion on technological issues of nanocrystal memory cells.

References

1. Perniola, L., Bernardini, S., Iannaccone, G., Masson, P., Salvo De, B., Ghibaudo, G., Gerardi, C.: Analytical model of the effects of a non-uniform distribution of stored charge on the electrical characteristics of discrete-trap non-volatile memories. *IEEE Trans. on Nanotech.* **4**, 360 (2005)
2. Eitan, B., Pavan, P., Bloom, I., Aloni, E., Frommer, A., Finzi, D.: NROM: A novel localized trapping, 2-Bit nonvolatile memory cell. *IEEE Electron Device Lett.* **21**, 543 (2000)
3. Swift, C.T., Chindalore, G.L., Harber, K., Harp, T.S., Hoefler, A., Hong, C.M., Ingersoll, P.A., Li, C.B., Prinz, E.J., Yater, J.A.: An embedded 90nm SONOS nonvolatile memory utilizing hot electron programming and uniform tunnel erase. Int. Electron Device Meeting (IEDM) Tech. Dig. 2002, p. 927
4. Salvo De, B.: & al. How far will Silicon nanocrystals push the scaling limits of NVMs technologies? Int. Electron Device Meeting (IEDM) Tech. Dig. 2003, p. 597
5. Lusky, E., Diamand, Y.S., Bloom, I., Eitan, B.: Characterization of channel hot electron injection by the subthreshold slope of NROM^{TM} Device. IEEE Electron Device Lett. **22**, 556 (2001)
6. Larcher, L., Verzellesi, G., Pavan, P., Lusky, E., Bloom, I., Eitan, B.: Impact of programming charge distribution on threshold voltage and subthreshold slope of NROM memory cells. IEEE Trans. Electron Devices **49**, 1939 (2002)
7. Shappir, A., Diamand, Y.S., Lusky, E., Bloom, I., Eitan, B.: Subthreshold slope degradation model for localized-charge-trapping based non-volatile memory devices. Solid State El. **47**, 937 (2003)
8. SILVACO-ATLAS User's Manual, vol.I–II
9. Liu, Z.H., Hu, C., Huang, J.H., Chan, T.Y., Jeng, M.C., Ko, P.K., Cheng, Y.C.: Threshold voltage model for deep-submicrometer MOSFET's. IEEE Trans. Electron Devices **40**, 86 (1993)
10. Landau, L.D., Lifshitz, E.M., Pitaevskii, L.P.: Electrodynamics of Continous Media (Butterworth-Heinemann, ch. 2, 1984)
11. Taur, Y., Ning, T.H.: Fundamentals of Modern VLSI Devices, p. 128 (Cam. Univ. Press, 1998)
12. Tsividis, Y.: Operation and Modeling of the MOS Transistor, p. 74. (Columbia Univ., 1999)