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Modeling and Simulation of Electron Devices

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Editorial: Modeling and simulation of electron devices

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The development of novel devices at the nanometer scale with potential for large-scale integration and room temperature operation is a formidable task. Over the years, many ideas have been proposed on the basis of very qualitative reasoning or simplified physical models: typically, the demonstration of working prototypes is achieved, while the fabrication of complex logic circuits proves to be unfeasible.

There are often fundamental problems, such as the extreme sensitivity of device operation to the presence of defects, stray charges, and other parasitics, or the need of prohibitively tight fabrication tolerances. In other cases the switching times are inherently slow, or the physical effect is so weak that room temperature operation is prevented.

Many of the difficulties and of the limits of candidate technologies for nanoelectronics and molecular electronics could be predicted, anticipated and, hopefully, solved if detailed modeling tools of realistic devices and structures were available. The same modeling tools could be used to design more robust devices, and to select molecules and device structures with potential for use in large-scale integrated circuits.

As far as more "mundane" CMOS technology is concerned, the importance of Computer Aided Design (CAD) tools in the development of industrial semiconductor technology was well outlined in the 1997 edition of the SIA National Technology Roadmap for Semiconductors—Technology Needs (page 6): *"Modeling and simulation is the only tool available for engineers to design processes, material use, transistors, and structures; there is no viable alternative. The major challenge is getting predictive model results from atomic scale through electrical performance; to accurately model new technologies a priori, resulting in development cost reduction; and faster time to market."*

In these years, research in silicon technology is making an unprecedented effort in experimenting alternative materials and device architectures to keep the regular pace of increasing integration that has been described in the terms of "Moore's law". New materials are considered for the channel (such as strained silicon, SiGe, germanium, and even carbon nanotubes), for the gate dielectrics (hafnium oxide and other so-called "high-K" dielectrics), and for the storage layer of non-volatile memories (such as layers of silicon nanocrystals embedded in SiO_2 or high-K dielectrics). As far as device architectures are considered, several solutions have been proposed with the main aim of improving the electrostatics of ultra short devices, including FinFETs, double-gate MOSFETs, tri-gate and silicon nanowire transistors, gate-all-around MOSFETs.

This is a particularly important time for the modeling and simulation community, which can play an important role in selecting the best options when a vast amount of experimental data on all possible combinations of alternatives is still missing. "Ab-initio" or atomistic modeling, in particular, may be extremely precious in the evaluation of alternative materials.

It is therefore a great pleasure for me to introduce the special issue of the Journal of Computational Electronics dedicated to the workshop on Modeling and Simulation of Electron Devices held in Pisa, Italy, 4–5 July 2005. The workshop is a continuation of the well established series of workshops on semiconductor device simulation. Previous meetings were held in Lille (1983, 1991, 1999), Leeds (1985, 1993), Duisburg (1986, 1994, 2000), Leuven (1988), Torino (1989, 1997), Eindhoven (1996), Ilkley (2002), and Barcelona (2003).

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Originally, the workshop mainly focused on technology and devices in the III-V material system. For the 2005 edition we enlarged the scope to include nanoelectronic and microelectronic devices. In practice, such move shifted the focus to silicon technology at the end of the International Technology Roadmap for Semiconductors and even beyond.

The workshop was also supported by the European Network of Excellence SINANO ("Silicon-based nanodevices"), which gathers 47 european academic and industrial partners. A significant portion of participants came from SINANO partners, which contributed to shift the focus to silicon devices.

This is also for me a chance to thank the "Università di Pisa" and the "CNR-Istituto di Elettronica e di Ingegneria Informatica e delle Telecomunicazioni" for supporting the workshop organization, our industrial sponsor "Silvaco", the members of the Program Committee and of the Organizing Committee, all the participants and authors.

This issue of the Journal of Computational Electronics contains a few of the papers derived from talks given at the workshop. A very broad range of devices is considered: in the III–V material system few examples are terahertz devices, HEMTs, and quantum cascade lasers; in silicon technology, devices include several nanoscale architectures for MOSFETs, silicon nanocrystal memories, and MEMS devices; among the so called "emerging research devices", carbon nanotubes transistors and quantum dots are considered.

The range of modeling approaches proposed is extremely vast, including compact and analytical modeling, semiclassical semiconductor simulations based on drift-diffusion transport, Monte Carlo solutions of the Boltzmann Transport Equation, quantum semiconductor simulations based on the effective mass approximation, and atomistic simulations.

This issue therefore provides a very nice snapshot of current hot research in device modeling, that makes a very interesting read. I hope you will enjoy it.