Evaluation of threshold voltage dispersion in 45 nm CMOS technology with TCAD-based sensitivity analysis.

Valentina Bonfiglio and Giuseppe Iannaccone
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa, Via Caruso 16, 56122 Pisa, Italia email:valentina.bonfiglio@iet.unipi.it

Abstract— **We propose an approach based on sensitivity analysis to evaluate threshold voltage variability of nanoscale MOSFETs due to line edge roughness (LER) and to random discrete dopants (RDD). It requires a very limited number of TCAD simulations, corresponding to computational load much smaller than that required for statistical simulations. We apply our approach to 45 nm CMOS technology, and show that with only few tens of device simulations one can obtain results comparable to those of statistical simulations, with an improved understanding of the impact of physical parameters on the variability of electrical characteristics.**

(Keywords: mismatch, parameter fluctuations, variability, MOSFET)

I. Introduction

Managing the statistical dispersion of transistor characteristics is one of the main requirements in the development of current and next CMOS technology nodes. To this purpose, one needs *i)* full understanding of variability sources and *ii)* tools and methods for a quantitative evaluation of parameter fluctuations at the device design and manufacturing stage.

Regarding the latter issue, statistical simulations are now the preferred approach [1,2]. As far as threshold voltage is concerned, the main sources of variability have been clearly identified and understood: random dopant distribution (RDD), line-edge roughness (LER), oxide-thickness variations [3], and polysilicon or metal-gate random grain distribution (RGD) [4].

In the literature, some analytical models of threshold voltage dispersion due to RDD [5,6] and to LER [7] have been proposed. Typically, they can be used only in the case of idealized structures and/or very simple doping profiles. However, analytical and semianalytical models have two important advantages: they are way faster than statistical simulations, and can help to clearly identify and understand the role of key physical parameters on the variability electrical parameters.

Here, we propose an approach based on sensitivity analysis and a limited number of TCAD simulations that provides the advantages of speed and physical understanding that is typical of analytical models, and the possibility of considering realistic doping profiles and geometry provided by TCAD simulations.

We focus on threshold voltage variability due to LER and RDD, considering the case of 45 nm bulk CMOS nMOSFETs for which data from statistical simulations to be used as a comparison are available [4].

Limited to the effect of LER, we have already demonstrated - for a different device structure - that our methodology allows us to obtain quantitatively very similar results as a 3D statistical simulation, which requires much larger computational resources [8].

II. Approach

The approach we propose requires us, as a first step, to translate all variability sources (process and geometry) in terms of dispersion of a set of synthetic parameters. Then, we have to identify a set of independent variability sources and synthetic parameters. Finally, we have to evaluate through sensitivity analisys the contribution to the dispersion of electrical parameters (e.g. the threshold voltage V_{th}) of each independent source. The last step is based on the assumption that the effect of each source of variability is sufficiently small that linearization is applicable.

The considered device is a minimum size nMOSFET, with polysilicon gate length of 42 nm, oxide thickness 1.7 nm, width of 45 nm. Further data can be found in Ref. [4]. TCAD simulations and scripts have been performed with Sentaurus [9].

A. Effect of random dopant distribution

In the case of RDD, the source of threshold voltage dispersion is the fluctuation of the dopant distribution in the active area. What matters is not only the total number of dopants in the active area, but also their position. However, we do not need to know with atomistic precision the effect of dopant distribution on threshold voltage.

First, we can acknowledge that the mechanism is mainly due to electrostatics, therefore impurity position along the width direction is not relevant. This allows us to simplify our analysis considering only 2D device structures. Then, we can assume that the effects of fluctuations of the number of dopants in different regions are small enough to add up linearly.

This work has been supported by the FP7 Network of Excellence NANOSIL (contract n. 216171) and by the ENIAC project 12003 MODERN.

For a given variation of dopant distribution $\Delta N_A(x,y,z)$ with respect to the nominal value we can write the following expression:

$$\Delta V_{th} = \int K(x,y)\Delta N_A(x,y,z)dxdydz \quad (1)$$

Where ΔV_{th} is the resulting variation of the threshold voltage, and $K(x,y)$ has the role of a propagator. The expression requires the linearity assumption to hold. The first assumption implies that K does not depend on z.

To conveniently compute the propagator K, we can assume that K is a smooth function of x and y, and move from the continuum to a discrete space, partitioning the active area in small rectangular boxes, as shown in Fig. 1a. Now we can write:

$$\Delta V_{th} = \sum_i \Delta V_{th_i} = \sum_i K_i \Delta N_i \quad (2)$$

The sum runs over all boxes, ΔN_i is the variation of the number of dopants in box i, and ΔV_{thi} is the threshold voltage variation if only dopants in box i are varied.

In practice, we multiply doping in box i by a factor $(1+\alpha)$ and compute ΔV_{thi} with TCAD simulations. Therefore we have

$$\Delta N_i = \alpha N_i \quad \Delta V_{th_i} = \alpha K_i N_i \quad (3)$$

so that (2) becomes,

$$\Delta V_{th} = \sum_i \left(\frac{\Delta V_{th_i}}{\alpha}\right) \cdot \alpha = \sum_i \left(\frac{\Delta V_{th_i}}{\alpha}\right) \cdot \frac{\Delta N_i}{N_i} . \quad (4)$$

We know need another reasonable assumption: doping variations in different boxes are non independent Poissonian processes. Therefore from (4) we can write

$$\sigma^2_{V_{th}} = \sum_i \left(\frac{\Delta V_{th_i}}{\alpha}\right)^2_i \cdot \frac{\sigma^2_{N_i}}{N_i^2} , \quad (5)$$

Since N_i is a Poisson process is $N_i = \sigma_{N_i}$ we finally have

$$\sigma^2_{V_{th}} = \sum_i \left(\frac{\Delta V_{th_i}}{\alpha}\right)^2 \cdot \frac{1}{N_i}$$

The threshold voltage dispersion due to RDD only requires a single TCAD simulation for each box, and an integral of the doping profile in each box. Box partitioning is shown in Fig. 1 and is smaller than the whole active area, because one can easily check that far from the channel the impact of doping fluctuations on V_{th} rapidly goes to zero.

To evaluate what is the granularity of partition required to obtain reasonably accurate results we have used different partitions, shown in Fig. 2: 10x1 a), 10x2 (b), 10x5 (c), 20x 10 (d), 40x20 (e). The table in Fig. 2 shows the standard deviation of the threshold voltage obtained at V_{ds} = *50 mV*, and Vds = 1.1 V. If the device is symmetric with respect to a source-drain swap, for low V_{ds} we can reduce to half the number of simulations required, since the propagator too is simmetric.

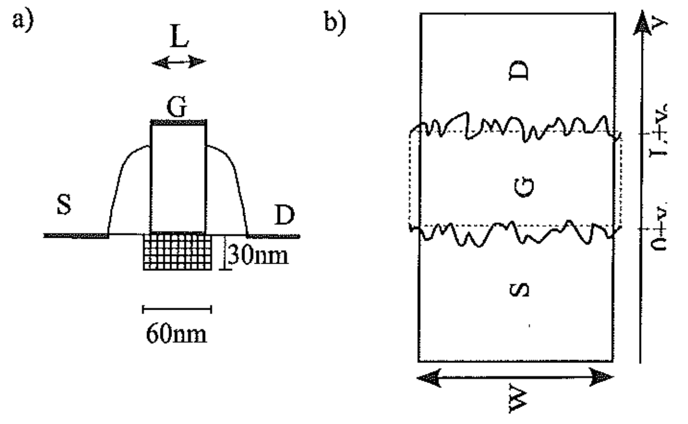
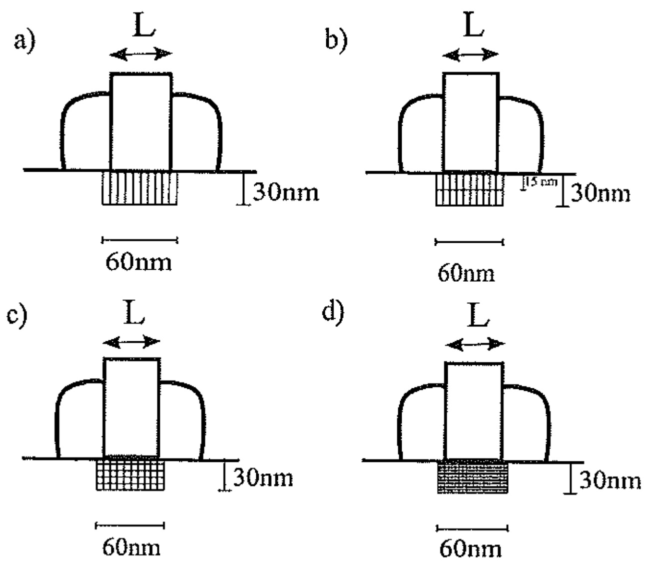
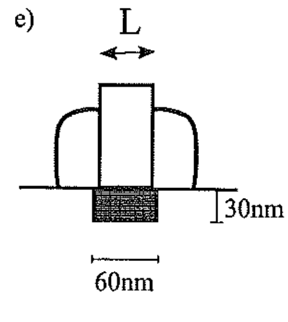


Figure 1. Illustration of concepts at the basis of the evaluation of the effect of LER (a) and of RDD (b)





σVth	Vds =50mV	Vds =1.1V
a (10x1)	36 mV	40 mV
b (10x2)	43 mV	46 mV
c (10x5)	45 mV	47 mV
d (20x10)	47 mV	50 mV
e (40x20)	48 mV	51 mV

Figure 2. (a) 10×1, (b) 10×2, (c) 10×5, (d) 20×10, (e) 40×20 boxes; table with results of σV_{th} for RDD.

Results show that only few simulations (in case 2b 20 for high V_{ds}, or 10 for low Vds) are sufficient to obtain reasonably accurate results. Very accurate results can be obtained in case

2d with a factor 10 more simulations. We have also checked that doping variations in the regions external to the partitions shown have no effect on the threshold voltage.

B. *Effect of line-edge roughness*

We can translate line edge roughness in term of the dispersion of the average position of both gate edges along the y axis ($y = 0 + y_1$ and $y = L + y_2$) in Fig. 1b. This in turn translates into gate length dispersion. We assume that y_1, y_2 are only affected by LER and their fluctuations are governed by independent processes.

To evaluate the variance of y_1 we assume a Gaussian autocorrelation function r of correlation length Λ_L and mean square amplitude Δ_L:

$$r(d) = \Delta_L{}^2 e^{-\frac{d^2}{2\Lambda_L{}^2}}$$

We find that:

$$\sigma_{y_1}^2 = \sigma_{y_2}^2 = \sigma_{LER}^2 = \frac{2\Delta_L^2 \Lambda_L}{W^2}\left[\Lambda\left(e^{-\frac{W^2}{2\Lambda^2}} - 1\right) + \sqrt{\frac{\pi}{2}} W erf\left(\frac{W}{\sqrt{2}\Lambda}\right)\right]$$

The variance of V_{th} due to line-edge roughness therefore is:

$$\sigma_{V_{th}LER}^2 = \left(\frac{\partial V_{th}}{\partial y_1}\right)^2 \sigma_{y_1}^2 + \left(\frac{\partial V_{th}}{\partial y_2}\right)^2 \sigma_{y_2}^2 = 2\left(\frac{\partial V_{th}}{\partial L}\right)^2 \sigma_{LER}^2$$

All required derivatives only require two 2D TCAD simulations, and are strictly dependent on device length, as shown in Fig. 3.

The total variance of the threshold voltage is computed by summing the variances due to all independent physical effects.

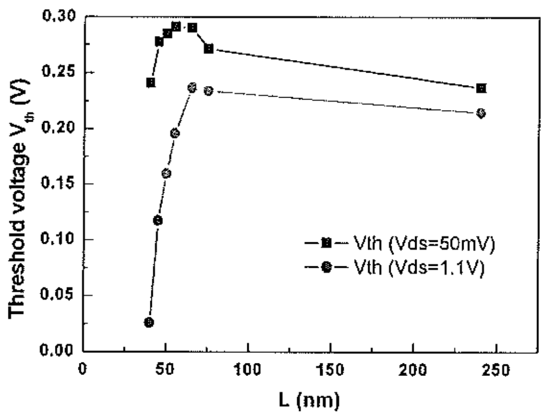


Figure 3. Threshold voltage as a function of gate length of the 45-nm CMOS from 2D TCAD simulations.

III Discussion

Table 1 shows the results for LER and RDD and the value of total variance of threshold voltage for V_{ds} equal to 50 mV and 1.1 V. The results are compared with those of Ref. [4] obtained with statistical simulations

For RDD we consider values of the standard deviation of the threshold voltage obtained for case 2e of Fig. 2.

As can be seen, results for the random dopants agree pretty well, also considering that the standard deviation of the error for the statistical method is 5% (ensembles of 200 devices). For the LER, especially at low V_{ds}, there is a significant discrepancy for which we do not have an explanation. The same method, applied to different devices in the case of LER and compared with statistical simulation results from the same group [8], provided a very good agreement.

We have shown that if the appropriate independent parameters are identified, the evaluation of the dispersion of the threshold voltage only requires the computation of a limited number of derivatives, each obtainable from one or two two-dimensional device simulations. The procedure is much less expensive from a computational point of view with respect to a statistical simulation (typically 100-200 3D simulations with a very fine grid). Obviously, there is a price to pay, in terms of the initial analysis of variability sources and the consequent assumptions.

We firmly believe that the method presented here is a powerful tool to quickly evaluate variability of device parameters in the context of technology developments, using simulations tools already available and routinely used by CMOS technology developers. It also provides a better understanding of the effect of single physical parameters on the overall device behaviour, and can therefore be a useful guide for device design.

TABLE I. RESULTS OF THE PROPOSED METHOD FOR THE THRESHOLD VOLTAGE STANDARD DEVIATION OF A MINIMUM SIZE NMOSFET (L=W=45NM) AND COMPARISON WITH ASENOV RESULTS

L = W = 45nm	Our method V_{DS} = 50mV	Stat. Sim [4] V_{DS} = 50mV	Our method V_{DS} = 1.1V	Stat.Sim[4 V_{DS} = 1.1
$\sigma_{Vth\ LER}$	7 mV	20 mV	22 mV	33 mV
$\sigma_{Vth\ RDD}$	47 mV	50 mV	50 mV	52 mV
$\sigma_{Vth\ TOT}$	48 mV	54 mV	55 mV	61 mV

References

[1] H.-S. Wong, Y. Taur, "Three-dimensional "atomistic" simulation of discrete random dopant distribution effects in sub-0.1 mm MoSFETs", *Tech. Dig. IEDM* 1993, pp.705-708.

[2] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 mm MOSFET's: A 3-D "atomistic simulation study" ", *IEE Trans. Electron Devices*, vol.45, pp. 2505, 1998.

[3] G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, and A. Asenov, "Simulation study of individual and combined sources of intrinsic parameter fluctuations in conventional nano-MOSFETs", IEEE Trans. Electron Devices, vol. 53, no. 12, pp.3063-3070, Dec. 2006.

[4] A. Cathignol, B. Cheng, D. Chanemougame, A. R. Brown, K. Rochereau, G. Ghibaudo, and A. Asenov, "Quantitative Evaluation of Statistical Variability Sources in a 45-nm Technological Node LP N-MOSFET", *IEEE Electron Device Letters*, vol.29, no. 6, June 2008.

[5] X. Tang , V. De, and J. D. Meindl, "Intrinsic MOSFET parameter fluctuations due to random dopant placement" *IEEE Trans. VLSI Syst.*, Vol. 5, pp. 369-376, 1997.

[6] P. A. Stolk, F. P. Widdershoven, and D. B. M. Klaassen, "Modeling Statistical Dopant Fluctuations in MOS Transistors", *IEEE Trans. Electron Devices*, Vol. 45 (9), pp.1960-1971, 1998.

[7] C. H. Diaz, H.-J. Tao, Y.-C. Ku, A. Yen, and K. Young, "An experimentally validated analytical model for gate line edge roughness (LER) effects on technology scaling." *IEEE Electron Device Letters*, Vol. 22, pp. 287–289, 2001.

[8] V. Bonfiglio, G. Iannaccone, "Analytical and TCAD-supported Approach to Evaluate Intrinsic Process Variability in Nanoscale MOSFETs", ESSDERC 2009, pp. 419 - 422.

[9] Manual of TCAD Sentaurus (SYNOPSYS), Version 12.2007.