Analytical Drain Current Model Reproducing Advanced Transport Models in nanoscale Double-Gate (DG) MOSFETs

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1. Abstract

In this paper we extend a Double Gate (DG) MOSFET model to nanometer technology nodes in order to include the hydrodynamic and quantum mechanical effects, and we show that the final model can accurately reproduce simulation results of the advanced transport models. Template devices representative of 22nm and 16nm DG MOSFETs were used to validate the model. The final model includes the main short-channel and nanoscale effects, such as mobility degradation, channel length modulation, drain-induced barrier lowering, overshoot velocity effects and quantum mechanical effects.

2. Introduction

Many modeling approaches for the determination of the drain current in MOSFETs are currently used and developed. One of the main reasons driving these modeling efforts is the industry need to understand performance improvements due to quasi-ballistic transport and other technology boosters such as strain, high-k dielectrics and ultra-thin-body Silicon-On-Insulator (SOI) architectures [1].Ultra-thin-film body MOS transistors and, in particular, double-gate (DG) MOSFETs are considered to be a very attractive option to improve the performance of CMOS devices. Nanoscale DG-MOSFETs introduce challenges to compact modeling associated with the enhanced coupling between the channels, ballistic or quasi-ballistic transport, quantum confinement, etc. In this work we present the extension of a DG MOSFET model to nanoscale technology nodes by incorporating quantum mechanical and hydrodynamic transport effects validating it by comparison with transport models range from drift-diffusion (DD) to direct solutions of the Boltzmann-Transport-Equation with the Monte Carlo method. Our starting point in this paper is a classical analytical model for the undoped DG-MOSFET [2] based on a unified charge control model [3]. The final compact model for the drain-current includes mobility degradation, short-channel effects (SCE), or channel length modulation (CLM). Velocity overshoot is also modeled through the hydrodynamic transport and quantum effects are extended from the classical compact model [4]. The results of the comparison between the compact model and simulations are presented and discussed in this work.

3. Simulated Devices and Approaches

The 22 nm template transistor is shown in Fig. 1.The 22 nm device is an idealized DG MOSFET with a gate length of 22 nm, a gate stack consisting of 2.4 nm of HfO_2 on top of 0.7 nm of SiO_2 (EOT=1.1 nm). The silicon film thickness is 10nm. The channel is lowly doped (10^{15} cm^{-3}).

The 16 nm device is an idealized DG MOSFET with a gate length of 16 nm, a gate stack of 4.7 nm of HfO_2 (EOT=0.8 nm). The silicon film thickness is 8nm. The channel is lowly doped (10^{15} cm^{-3}).

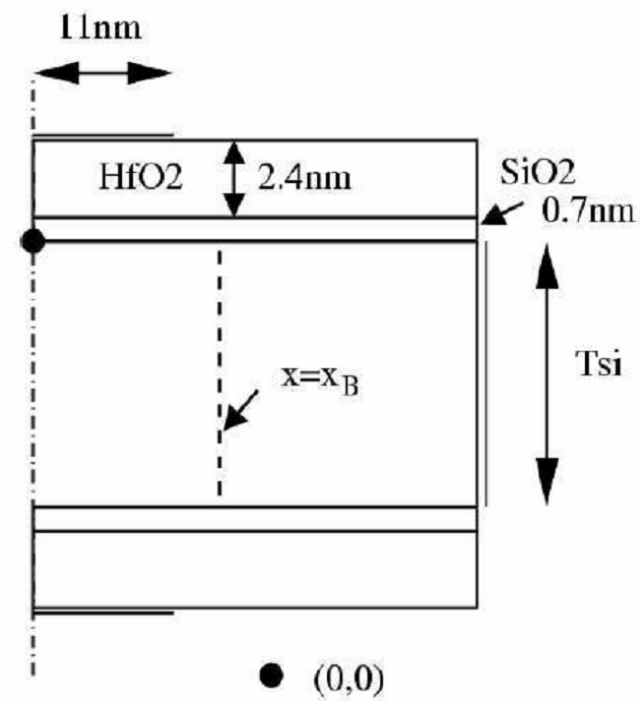

Fig.1: *Structure of the 22 nm template transistor used in the work. One half of the symmetric structure is shown. All dimensions are in nm.*

The key features of each model (identified with the acronym of the main developer) are presented. The models are grouped into two families: the MC family which collects models based on the direct solution of the Boltzmann-Transport-Equation (BTE) using Monte Carlo method, and the DD family, which gathers drift-diffusion like models where only the first momenta of the BTE are calculated. The MC family model incorporates all relevant scattering mechanisms such as ionized impurities (II), surface roughness (SR), phonon scattering, etc. Also, different simulation approaches have been implemented such as full-band, semi-classical, multi sub-band ensemble monte-carlo simulators. The numerical models used by the different groups [5]-[7] differ in terms of band-structure, scattering models, etc. For comparison, all simulators have been first calibrated to reproduce the universal curves in silicon devices.

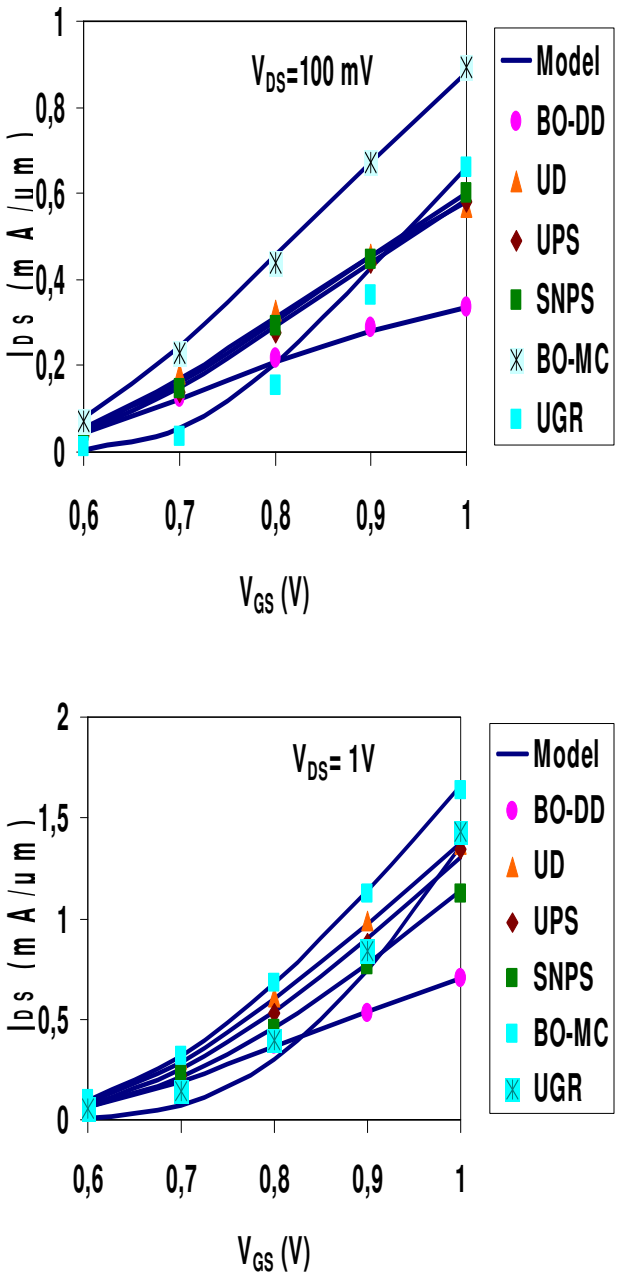

Fig.2: *Trans-characteristics of 22 nm DG MOSFETs for low (top) and high (bottom) V_{DS}.Numerical simulation data by Univ.of Bologna (BO-DD) [6], Univ.of Udine (UD) [6], Univ.of Paris-Sud (UPS) [6], Synopsys (SNPS) [6], Univ.of Bologna (BO-MC) [6], Univ.of Granada (UGR) [7]*

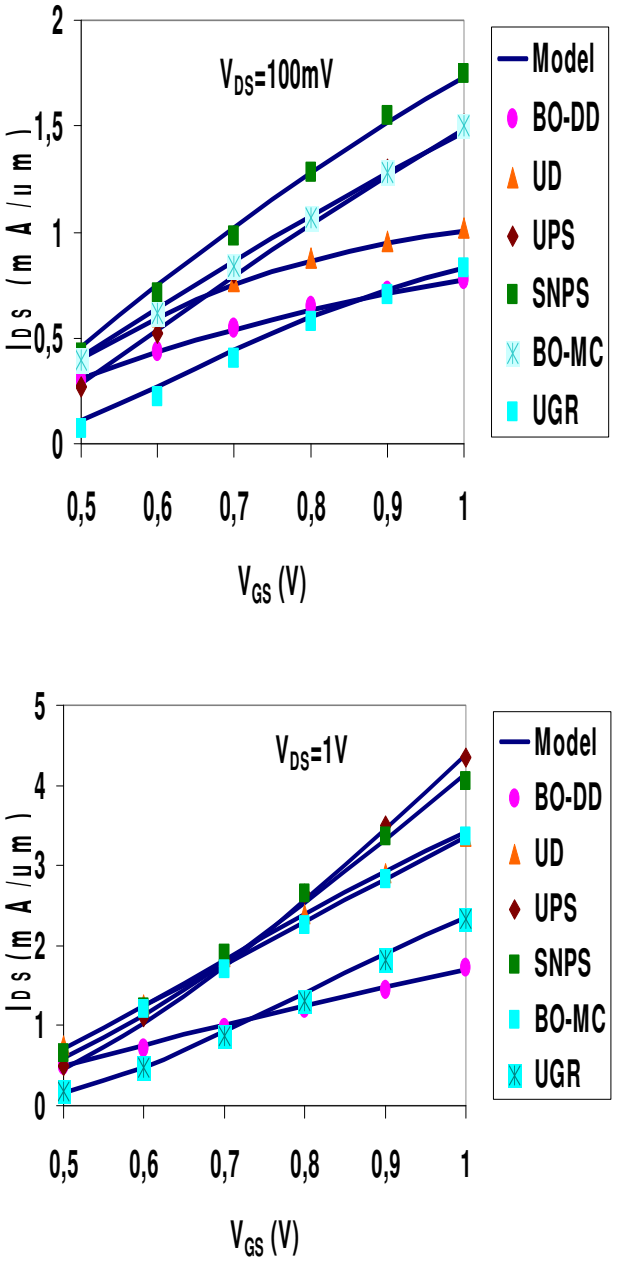

Fig.3: *Trans-characteristics of 16 nm DG MOSFETs for low (top) and high (bottom) V_{DS}. Numerical simulation data by Univ.of Bologna (BO-DD) [6], Univ.of Udine (UD) [6], Univ.of Paris-Sud (UPS) [6], Synopsys (SNPS) [6], Univ.of Bologna (BO-MC) [6], Univ.of Granada (UGR) [7]*

4. DC Model

We have accurately reproduced these advanced transport model simulations using our compact model (with physical parameter values), taking into account the physical mechanisms included in their approaches. The mobile charge densities at the source Q_s and at the drain Q_d end are calculated using,

$$Q = 2C_g\left(-\frac{2C_g\beta^2}{Q_o\exp\left(\frac{V_{scc}}{\beta}\right)}+\sqrt{\left(\frac{2C_g\beta^2}{Q_o\exp\left(\frac{V_{scc}}{\beta}\right)}\right)^2+4\beta^2\log^2\left[1+\exp\left[\frac{V_{gs}-V_{th}+\Delta V_{th}-V}{2\beta}\right]\right]}\right) \quad (1)$$

where $Q_o = 4\beta C_{si}$ and $\beta = \frac{kT}{q}$, $C_{si} = \frac{\varepsilon_{si}}{t_{si}}$ is the silicon-film capacitance, t_{si} being the silicon-film thickness. V_{th} is defined as

$$V_{th} = V_o + 2\beta\log\left(1+\frac{Q'}{2Q_o}\right) \quad (2)$$

where Q' is calculated by solving eqn (1) for Q but using V_o instead of V_{th} in eqn (3) and without considering the ΔV_{th} correction.

$$V_o = \Delta\varphi - \beta\log\left(\frac{qn_i t_{si}}{2Q_o}\right) \quad (3)$$

where

$$\Delta V_{th} = \frac{\left(\frac{C_g\beta^2}{Q_o}\right)Q'}{Q_o+\frac{Q'}{2}} \quad (4)$$

where $\Delta\varphi$ is the work function difference between the gate electrode and the intrinsic silicon, n_i being the intrinsic concentration.

where $C_g = \frac{C_{ox}}{\left(1+\frac{C_{ox}y_1}{\varepsilon_{si}}\right)}$ is the effective oxide capacitance calculated using the inversion-layer centroid [8] to take into account the quantum mechanical effects, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ is the gate oxide capacitance, t_{ox} is the oxide thickness. In eqn (1), the term ΔV_{th} ensures the correct behaviour of Q above threshold.

The velocity overshoot is included in the model using a one dimensional energy-balance model [9]. The velocity overshoot is modeled through the hydrodynamic transport model which is included in the model. The low-field mobility data are obtained from a model that takes into account the mobility degradation [10] due to quantum effects. We have also included the effects of channel length modulation (CLM) and drain-induced barrier lowering (DIBL) [2].

The drain current expression is thus written in terms of the charge densities at the source and drain ends [2] as,

$$I_{DS} = \frac{W\mu_{eff}}{L_e(1+\gamma_n V_{dss})}\left[2\frac{kT}{q}(Q_s-Q_d)+\frac{Q_s^2-Q_d^2}{4C_g}+8\left(\frac{kT}{q}\right)^2 C_{si}\log\left[\frac{Q_d+2Q_o}{Q_s+2Q_o}\right]\right] \quad (5)$$

where

$$\mu_{eff} = \frac{\mu_o}{1+\theta_1\beta\log(1+\exp(1+(V_{gs}-V_o)/V_t)+\theta_2\beta^2\log(1+\exp(1+(V_{gs}-V_o)/V_t)^2}$$

is the mean effective mobility [10], where μ_o is the low-field mobility, and θ_1 and θ_2 are the mobility attenuation coefficients of the first and second orders, respectively, which can be considered as a fitting parameters, $\gamma_n = \frac{\mu_{eff}}{v_{sat}L}\left(\frac{1}{1+2\lambda_w/L}\right)$ is the hydrodynamic model [9] through which the velocity overshoot is also modeled where $\lambda_w \approx 2v_{sat}\tau_w$, v_{sat} is the saturation velocity and τ_w is the energy relaxation time constant, $L_e = L - \Delta L$ and W is the effective channel length and width of the device respectively.

The final compact model for the drain current includes the mobility degradation, short channel effect and velocity overshoot which is modeled through the hydrodynamic transport.

In addition, the quantum confinement correction is included in the threshold voltage of the model. Thus, the correction makes a positive shift in the threshold voltage of the device (n-channel) [11].

5. Results and Discussions

The results of our compact model have been compared with numerical simulation data obtained by several research groups using advanced transport models [5]-[7]. Fig. 2 shows the trans-characteristics of the 22 nm DG MOSFETs at low and high V_{DS}. A good agreement between the compact model and the simulations is obtained by considering the low field mobility and for a fitted saturation velocity. Fig. 3 shows the trans-characteristics of the 16 nm DG MOSFETs at low and high V_{DS}. A good agreement is obtained between the compact model and the simulations. The mobility degradation at low drain voltages is significantly

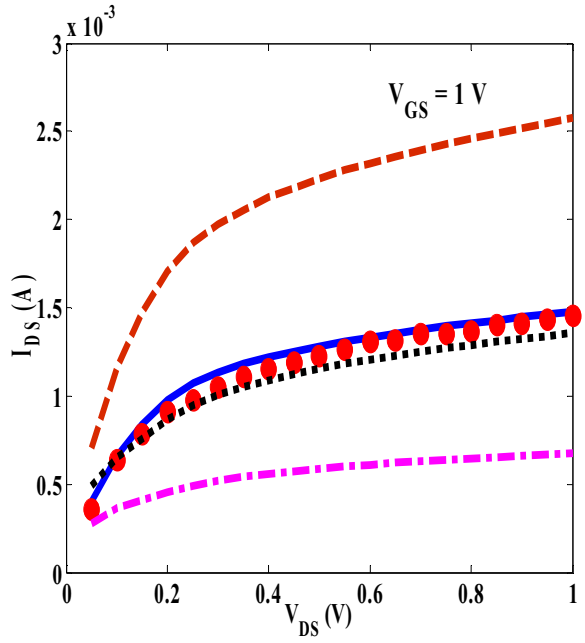

Fig.4: *Output characteristics of 22 nm DG-MOSFET for V_{GS}=1V Dashed line: Without quantum effects, Solid line: Compact model, Dotted line: Without velocity overshoot and quantum effects, Dash-dotted line: Without hydrodynamic transport, Symbol: Simulation (UGR-MSB-EMC) [7].*

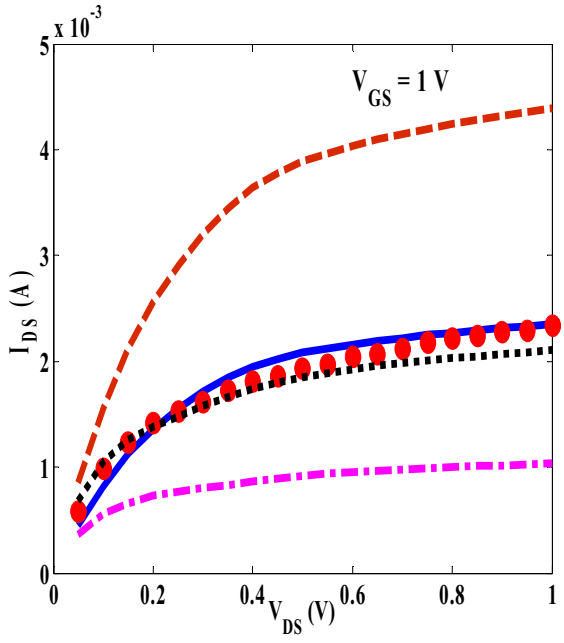

Fig.5: *Output characteristics of 16 nm DG-MOSFET for V_{GS}=1V Dashed line: Without quantum effects, Solid line: Compact model, Dotted line: Without velocity overshoot and quantum effects, Dash-dotted line: Without hydrodynamic transport, Symbol: Simulation (UGR-MSB-EMC) [7].*

reproduced. As expected the drain current values provided by the drift-diffusion model (BO-DD) are lower than the other numerical models for both 22 nm and 16 nm devices.

Figs. 4 and 5 show the output characteristics of the 22 nm and 16 nm DG MOSFETs. A good agreement between the compact model and the simulations (UGR-MSB-EMC) [7] are seen. It can be seen that the model without the effect of velocity overshoot and quantum effects, a good agreement is obtained at low drain bias and becomes lower at higher drain bias. If the quantum effects are not included in the model, the current is significantly higher than the MC simulations. If the hydrodynamic transport is not considered the model gives much lower current values than the simulation. It can be inferred that the hydrodynamic model can be used to compare results from advanced transport models.

6. Conclusions

The comparison between the advanced transport modeling approaches and the compact model for the drain current in nanoscale DG MOSFETs are presented. The model is valid and continuous in linear and saturation regimes. The model used for the mobile charge is valid in weak and strong inversions. Short channel effects are taken into account by modeling the channel length modulation and drain induced barrier lowering, as well as mobility degradation, velocity saturation and quantum mechanical effects are also included. The model shows a very good agreement with the simulation results obtained for the practical range of voltages considered.

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