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Origin of the Substrate Current after Soft-Breakdown in Thin Oxide n-MOSFETs

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Origin of the Substrate Current after Soft-Breakdown in Thin Oxide n-MOSFETs

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Abstract In this paper is presented an experimental investigation on the origin of the substrate current after soft-breakdown in n-MOSFETs with 4.5 nm-thick oxide. At lower voltages this current shows a plateau that can be explained with the generation of hole-electron pairs in the space charge region and at the Si-SiO_2 interface, and to carrier diffusion between the channel and the substrate. At higher voltages the subtrate current steeply increases with voltage, due to trap-assisted tunneling from the substrate valence band to the gate conduction band, which becomes possible for gate voltages higher than the threshold voltage. Measurements on several devices at dark and in the presence of light, and in the case on substrate reverse bias, confirm the proposed interpretation.

1. Introduction

The integrity of thin silicon dioxide films is one of the most important reliability issues for future ULSI's. In recent years much effort has been dedicated to the study of a new degradation mode in thin oxides, called with several different names: soft-breakdown (SBD), quasi-breakdown, B-mode SILC, or partial-breakdown [1-4]. Although several SBD models have been proposed, the conduction mechanism of SBD has not been clarified yet.

The main features of SBD are: i) an abrupt increase of the low field current through the oxide on top of the SILC and ii) an increase of the noise at the gate electrode. Depending of the type of induced noise, SBD has been classified in: analog or stable mode, characterized by 1/f noise, and digital or unstable mode, characterized by random telegraph signal (RTS) noise [5,6].

Although many authors have claimed that SBD is possible only in oxide films thinner than 5 nm, this degradation mode has been reported also in a 9.6 nm thick oxide [5]. For this reason, SBD should be a concern also for the reliability of E^2PROM devices, even if there is still much debate on the relationship between SBD and device failure [7,8].

Lee *et al.* have reported that the SBD event gives rise to a large current jump at the high stress fields also at the substrate electrode [1]. They proposed that the physically damaged region (PDR) of the SBD spot makes the hole barrier lower and reduce the hole tunneling distance, which results in a large increase of hot hole injection from the anode. In a recent work [6] the characteristic of the substrate current as a function of the gate voltage after SBD is reported for the first time, and a strong correlation is shown to exist between current noise at the gate and substrate electrode during the SBD analog mode and a direct correlation during the SBD digital mode.

Our investigation has been focused on the substrate current, in order to acquire new knowledge on the conduction mechanisms through the SBD spot and the characterization of the nMOSFETs after SBD. We report new experimental results on the substrate current in n-MOSFETs after analog SBD in different operating conditions and propose an explanation of its origin consistent with the measurements performed.

2. Experimental Details

The n-MOSFETs used in this work were fabricated on (100) oriented *p*-type substrates. The 4.5 nm-thick oxide was grown in wet ambient at 700 °C. The gate was phosphorus-implanted at 30 keV (dose $2x10^{14}$ cm^{-2}). After gate definition, arsenic was implanted into the source and drain regions at 75 keV. All the electrodes were metalized with

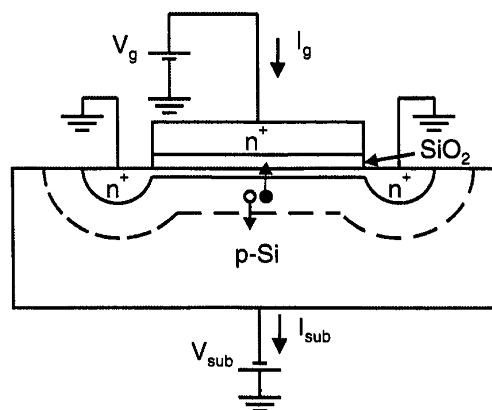

Fig. 1: Experimental arrangement for carrier separation in nMOSFETs.

aluminum in order to lower the contact resistance for the electrical measurements. The threshold voltage V_{th}, measured on several devices, is 1.1 V and no significant change was observed after SBD, in agreement with other results presented in the literature [7].

All the measurements have been realized by means of an HP4156 semiconductor parameter analyzer using the carrier separation method [9], shown in Fig.1. Using this bias configuration, the gate current is almost entirely due to the electron current flowing from the inversion layer, whereas an hole current can be measured as substrate current.

3. Results and Discussion

Fig. 2 shows the gate current I_g and the substrate current I_{sub} as a function of the gate voltage V_g after SBD, with V_{sub}=0, for one of the devices considered. The curves shown may somewhat vary with different devices, being dependent on the particular failure occurred; nevertheless, they exhibit a regular and reproducible behavior, which allow to clearly identify three different regions.

The first region is that where $0<V_g<V_{P1}$~0.3-0.5 V: both I_g and I_{sub} increase with the applied voltage, and have approximately the same value. This is confirmed by the data shown in Fig. 3, where the ratio I_g/I_{sub} in the first region is plotted for five different devices after SBD, and in all cases is very close to one, meaning that I_g and I_{sub} are practically coincident.

The second region is that defined by $V_{P1}<V_g<V_{P2}$, where V_{P2} has value in the range 1.1-2.5 V, depending on the particular sample. In this region I_g rapidly increases with V_g, while I_{sub} exhibits a plateau varying from a few picoamperes to a few tens of pA, again depending on the particular sample. The plateaus are usually rather flat, and in many cases the substrate current exhibits a shallow minimum near the middle of the plateau.

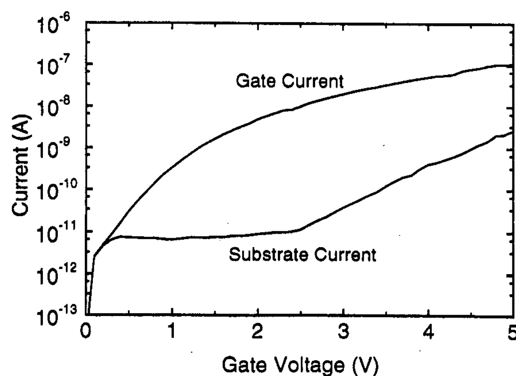

Fig.2: Gate and substrate current as a function of the gate voltage after SBD. Three different regions can be identified in the substrate current.

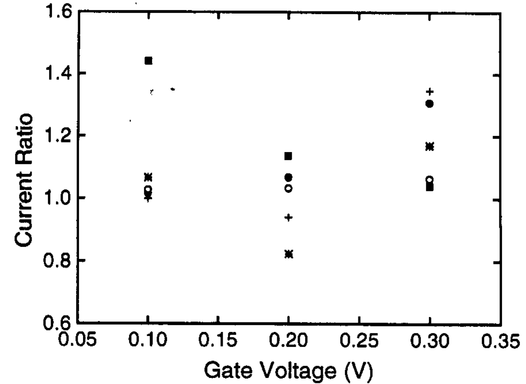

Fig. 3: Values of the ratio between the gate current and the substrate current at low gate voltages for five different samples.

The third region is defined by $V_g>V_{P2}$: the behavior of the gate current practically is unchanged, while the substrate current steeply increases with the gate voltage.

In Fig. 4 are shown the conduction and valence bands, computed with a one-dimensional self-consistent Poisson-Schrödinger solver for different values of the gate voltage.

For V_g lower than V_{P1} [Fig. 4(a)] the current is basically due to the generation of hole-electron pairs in the space charge region and at the Si-SiO_2 interface via the SHR mechanism, and to the diffusion of carriers between the channel and the substrate. In the case of fresh oxide electrons cannot escape the inversion layer, therefore recombination exactly balances generation, diffusion in both direction is balanced, and there is no net current. When SBD occurs, generated electrons are quickly collected at the gate electrode and holes at the substrate electrode, so that there is a net deficit of carriers in the channel region that sustains the current.

Since the gate voltage is still very low, electrons cannot reach the channel from the contacts because of the high potential barrier they encounter, therefore I_g and I_{sub} must be practically identical, as shown in Fig. 3.

In the second region ($V_{P1}<V_g<V_{P2}$) I_g rapidly increases with respect to I_{sub} because a new contribution is added to I_g. With increasing V_g, the transmission probability of the gate oxide rapidly increases, and electrons in the inversion layer are more effectively collected by the gate. In addition, when V_g approaches V_{th} the potential barriers from the drain and source contacts to the Si-SiO_2 interface are progressively lowered, so that electrons from the contacts easily reach the SBD spot and contribute to I_g. Since there is a low impedance path for electrons from the contacts to the gate,

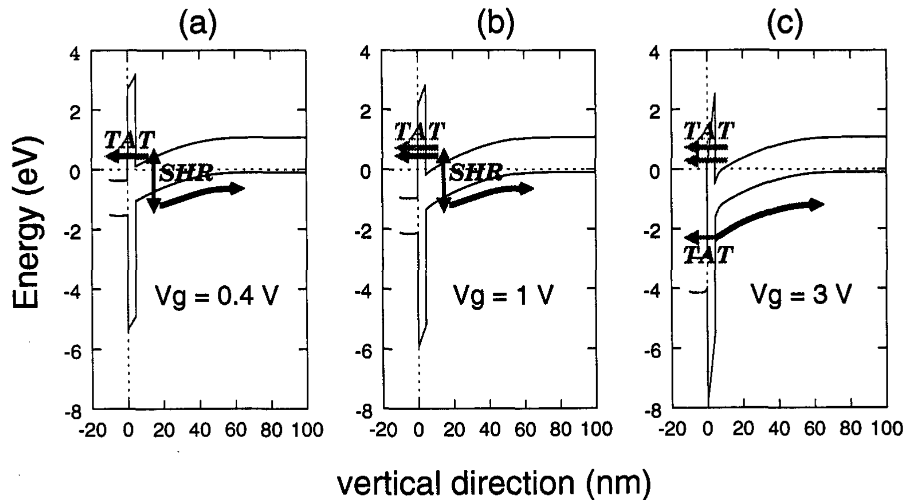

Fig. 4: Conduction and valence band profiles computed with a one-dimensional Schrödinger-Poisson solver for different values of the gate voltage: 0.4 V (a), 1 V (b), 3 V (c).

the quasi-Fermi level for electrons in the channel is virtually unchanged, leaving diffusion and generation currents between the substrate and the channel unchanged. This is the reason for the plateau of I_{sub}.

When V_g is increased above V_{P2}, I_{sub} undergoes a steep increase, because a new mechanism becomes dominant: as can be seen in Fig. 4(c), for V_g greater than V_{th}, interband trap-assisted-tunneling from the valence band in the bulk to the conduction band of the gate can take place. This contribution to the current increases more rapidly than the gate current, since the number of states available for interband tunneling increases super-linearly with the gate voltage, while electrons in the conduction band available for tunneling are proportional to V_g - V_{th}.

The interpretation just discussed of the substrate current behavior is consistent with the data shown in Fig. 5, where substrate and gate currents after SBD at dark and under light irradiation are plotted as a function of V_g. As can be seen, only the substrate current in the first and second region is greatly enhanced by light, confirming the fact that electron-hole generation in the space charge region and/or at the SiO_2 interface is the dominant mechanism. On the other hand, I_{sub} in the third region as well I_g are due to mechanisms completely unaffected by photon absorption.

It is worth noticing that the device considered in Fig. 5 has the highest substrate current among the samples considered, therefore has a highly conductive SBD spot: for this reason, it has the lowest value of V_{P2} , which is practically equal to V_{th} (as highlighted in the insert), consistent with the minimum allowed value of V_g for interband tunneling.

In Fig. 6 gate and substrate currents are plotted as a function of V_g for different values of the substrate voltage V_{sub}. With increasing V_{sub} the generation of carriers in the space charge region is enhanced because the depletion region is widened, and quasi-Fermi levels for electrons and holes are separated; in addition, a net current due to electrons from the substrate diffusing to the channel

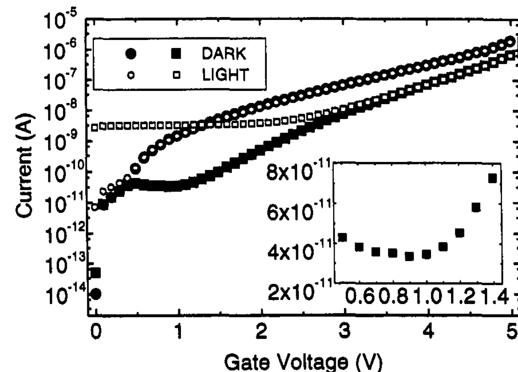

Fig. 5: Gate (circles) and substrate (squares) current after SBD at dark and under light irradiation. Illumination increases only the plateau of the substrate current. The insert highlights a threshold in the substrate current at about 1.1 V.

region and then tunneling to the gate is established. Both these factors increase the substrate current in the first and second region, while do not affect, as expected, other components of I_g and I_{sub}.

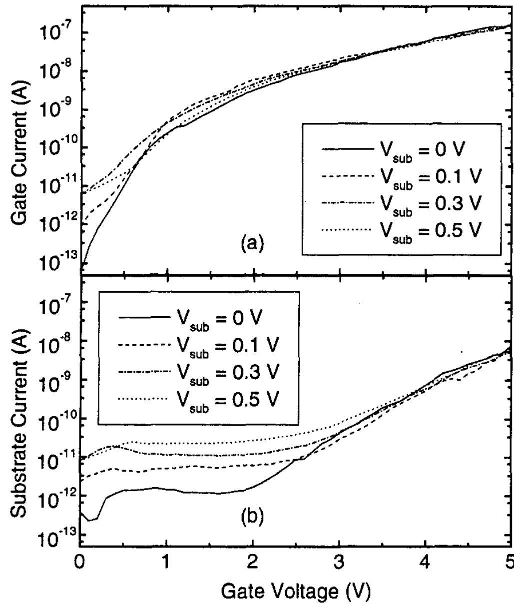

Fig. 6: Gate (a) and substrate (b) current as a function of the gate voltage for different values of the substrate voltage after SBD. Only the plateau of the substrate current sugnificantly increases with the substrate voltage.

4. Conclusion

An extensive experimental investigation of the substrate current in n-MOSFETs after SBD has been performed in different operating conditions. In addition, an interpretation of the experimental results has been presented which is in substantial agreement with the measurements performed. In our opinion, two main aspects need to be clarified yet: the first is whether generation of electron-hole pairs occurs mainly in the space charge region or at the silicon-silicon dioxide interface, due to traps induced by SBD. The second is the detailed tunneling mechanism of electrons and holes through the SBD spot. The main problem in the investigation of both these issues is the extreme variability of the characteristics of SBD spots, which makes difficult to compare and correlate quantitatively results from different samples. For this reason, we think that the simultaneous measurement of current due to electrons and holes could make easier the development and validation of a model for transport through the SBD spot.

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