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Evaluation of performance and perspectives of nanocrystal Flash memories based on 3D quantum modeling

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Abstract

In this paper we evaluate from a quantitative point of view the electric properties of nanocrystal Flash memories, in which the floating gate of conventional Flash-EEPROMs is replaced with a layer of silicon nanocrystals. We have developed a three-dimensional solver of the Poisson-Schrödinger equation based on density functional theory, with the local density approximation. In this paper we focus on the stationary electric behavior of the memory devuces, focusing on the effect of nanocrystal size and density, and providing a first estimate of the effect of randomness in the nanocrystal layer.

1 Introduction

The rapid growth of the market for portable electronic appliances (cellular phones, GPS, palm computers) requires memory devices with very large storage density. In particular, this situation has strongly accelerated the development of solid state memories such as Flash-EEPROMs, which provide superior robustness and reduced access times with respect to magnetic storage devices. The state of the art of Flash-EEPROMs currently follows the evolution of VLSI Technology: 128 Mbit chips are currently being fabricated with 0.18 μm technology.

An interesting evolutionary path for Flash EEPROMs is represented by the recently proposed nanocrystal Flash memories [1, 2], which are extensively studied in industrial and academic laboratories [3, 4, 5, 6, 7]. A layer of silicon nanocrystals embedded in a thin oxide layer can be used as a charge storage medium that promises to efficiently replace the polysilicon floating gates used in current Flash EEPROMs.

In particular, a few electrons trapped in a nanocrystal layer sandwiched between the gate and the channel of a MOSFET, as sketched in Fig. 1, can increase significantly the MOSFET threshold voltage, and therefore store a bit of information.

The operation of a memory based on nanocrystals in sketched in Fig. 2(a-c). The memory is programmed by

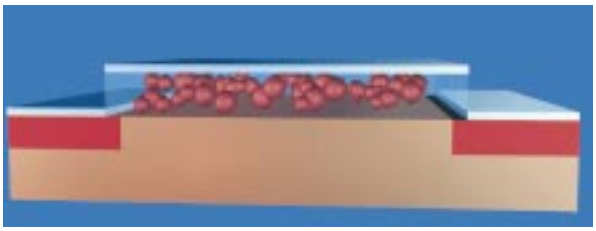

Figure 1: Sketch of the memory obtained with a nanocrystal layer stacked between the gate and the channel of a MOSFET.

applying to the gate a positive voltage of a few Volts, that lowers the dielectric conduction band and enhances tunneling of electrons from the substrate to the nanocrystals (Fig. 2(a)). Electrons get trapped in the nanocrystal, since further tunneling to the gate is inhibited by the thick barrier. However, due to already observed Coulomb Blockade effects at room temperature [3], only a well defined number of electrons (depending on the applied gate voltage) can occupy each nanocrystal, so that charging of the nanocrystals is a self-limited process. When one electron is added to each nanocrystal the MOSFET threshold voltage increases in steps, so that both single and multi-bit storage is possible. The information stored in the memory is then simply read by measuring the saturation current corresponding to a given voltage applied to the gate.

When only reading voltages are applied to the gate, tunneling barriers are sufficiently opaque to prevent electrons from leaking out and therefore information is retained (Fig. 2(b)). Information is erased by applying a negative gate voltage that removes electrons from the traps (Fig. 2(c)). Given the small number of electrons involved in device operation, nanocrystal layers are very promising in terms of reduced power consumption, short program-erase times, and limited degradation after many write-erase cycles.

While a conventional Flash EEPROM (Electrically Erasable Programmable Read-Only Memory) has a tunneling oxide typically thicker than 7 nm and requires programming voltages larger than 10 V, a nanocrystal memory has a very thin tunneling oxide (2-4 nm), exhibits short programming times with direct tunneling

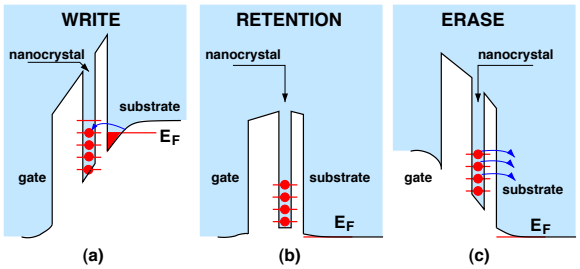

Figure 2: Basic operation of the nanocrystal memory: (a) conduction band profile along z when a positive voltage of a few V is applied to the gate and pictorial view of the write operation; (b) conduction band profile along z during the retention of information; (c) conduction band profile along z when a negative voltage of a few V is applied to the gate and pictorial view of the erase operation.

dot/insulator material	ΔV_T per electron	retention time	Ref.
Si in SiO_2	0.36 V	not shown	[1]
InAs/AlGaAs	0.25 V	1 h @ 100 K	[6]
Si or Ge in SiO_2	0.3 V	$\approx$ 1 h	[5]
SiGe/SiO_2	0.4 V	1 day	[7]
SRO/SiO_2	$\approx$ 1 V	not shown	[4]
Si/Si_3N_4-SiO_2	0.48 V	$\approx$ 3 h	[3]

Table 1: A few prototypes of nanocrystal memories presented in the literature, with measured ΔV_T per electron and retention time

and much smaller write-erase voltages ($\approx$ 3 V). It is therefore extremely promising in terms of endurance to write-erase cycles and power consumption [4], while it usually has a poor retention time, compared to the ten year requirement typical of commercial Flash EEPROMs.

Nanocrystal memories might have interesting applications as quasi-non volatile memories, where cyclability and power consumption are more important than a ten-year data retention time, or as Dynamic Random Access Memories with very long refresh time. In addition, Coulomb blockade effects should enable easy implementation of multi-bit storage schemes.

Several materials have been investigated for the nanocrystals and the dielectric layer, as shown in table I. At present, Silicon Rich Oxide deposited by LPCVD on SiO_2 [4] and implanted Si or Ge in SiO_2 [5] are the most promising from the point of view compatibility with current CMOS technology, retention time and threshold voltage shift per electron.

2 Basic functions of the nanocrystal layer

A simplified quantitative evaluation of the operation of such memories can be done by considering the equivalent capacitive circuit of the nanocrystal layer (Fig. 3): each nanocrystal is coupled to the top gate by a capacitance C_1 and to the bottom channel by a capacitance C_2. A capacitance C_3 per each nanocrystals couples the gate and the channel (C_3 is the total direct capacitance between gate and channel divided by the total number of nanocrystals). The channel node is grounded. If an electron charge $-q$ is put in the nanocrystal, in order to keep the same charge in the channel node the gate voltage must be increased by a quantity

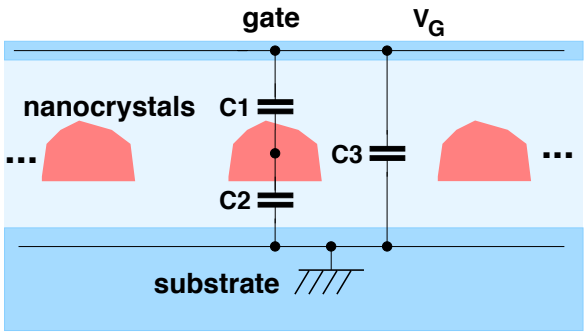

Figure 3: Equivalent capacitance circuit of the nanocrystal layer: C_1 is the capacitance between nanocrystal and gate, C_2 is the capacitance between nanocrystal and channel, C_3 is the capacitance between channel and gate divided by the number of nanocrystals

$$\Delta V_{th} = \frac{q}{C_1 + C_3(C_1 + C_2)/C_2}; \qquad (1)$$

ΔV_{th} represents the threshold voltage shift obtained when one electron is added to each nanocrystal in the layer. As can be seen, in order to increase ΔV_{th}, one must reduce C_1, i.e., reduce the size of the nanocrystal or increase the distance between dots and the top gate, and reduce C_3, i.e., increase the nanocrystal density.

On the other hand, the additional gate voltage required to win Coulomb repulsion and put one more electron into the dot in a state of energy E_0 is

$$\Delta V_G = \frac{q}{C_1} + E_0 \frac{C_1 + C_2}{C_1}; \qquad (2)$$

again, a small value of C_1 and a strong confinement (large E_0) is required for obtaining a large ΔV_G.

3 Three-dimensional model

Since the device structure is inherently three-dimensional and electrons in the dot are strongly confined (the nanocrystal diameter is usually in the range 3-10 nm), an equivalent electrical circuit would not be adequate for obtaining accurate results. For this reason, we have developed a code for the self-consistent solution of Poisson and Schrödinger equations on a 3D grid, based on density functional theory with local density approximation. [8]

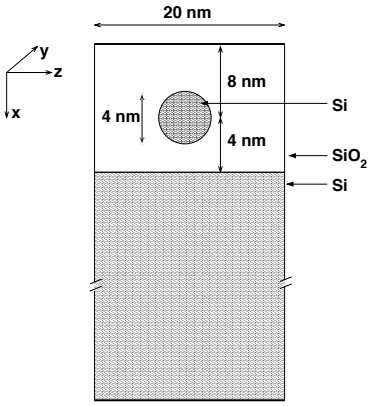

Figure 4: View of one simulation domain: the nanocrystal is a silicon sphere with a diameter of 4 nm embedded in a 12 nm oxide layer.

While nanocrystals are of course randomly distributed in the layer, we have considered a simplified situation where disorder is removed, that is, nanocrystals occupy a perfect two-dimensional lattice in the dielectric layer.

The regular arrangement of dots allows us to simulate only the region that represents the elementary cell of the lattice structure, and then to apply periodic boundary conditions to the potential. The domain in which we actually solve the Schrödinger-Poisson equation is shown in Fig. 4. The surface density of nanocrystals σ_{nc} is the inverse of the area of the considered domain on the horizontal plane: we consider an area varying from 10×10 nm^2, corresponding to $\sigma_{nc} = 10^{12}$ cm^{-2} to 30×30 nm^2, corresponding to $\sigma_{nc} = 1.1 \times 10^{11}$ cm^{-2}. The nanocrystal is a silicon sphere with diameter between 3 and 5 nm embedded in a silicon oxide layer of 12 nm. We assume that the center of the dot is at distance of 4 nm from the Si-SiO_2 interface.

Let us point out that we are making two implicit assumptions: that all nanocrystals are in the same charge condition and that edge effects acting on nanocrystals located close to the contacts are not relevant. While the latter can be readily accepted if we assume a sufficiently large number of nanocrystals under the gate (e. g., at least 5×5), the former is only justified because here we focus on stationary properties of the memories: it would not be acceptable if we were interested in the time-dependent process of nanocrystal charging. The potential profile in our domain is determined by the Poisson equation

$$\nabla[\epsilon \nabla \phi(\mathbf{r})] = -\rho(\mathbf{r}) = -q[p(\mathbf{r}) - n(\mathbf{r}) + N_D^+(\mathbf{r}) - N_A^-(\mathbf{r})], \quad (3)$$

where ϕ is the scalar potential, ϵ is the dielectric constant, p and n the hole and electron densities, respectively, N_D^+ and N_A^- the concentrations of ionized donors and acceptors, respectively, that depend on ϕ as indicated in Ref. [9]. While electrons and hole concentrations in the substrate are computed with the semiclassical approximation [9], electrons in the nanocrystal are strongly confined, and therefore their density is computed by solving the Schrödinger equation with density functional theory:

$$-\frac{\hbar^2}{2} \nabla \left(\frac{1}{m} \nabla \Psi \right) + E_c(\mathbf{r}) \Psi + V_{xc}(\mathbf{r}) \Psi = E \Psi, \quad (4)$$

where E_c is the conduction band in the nanocrystal ($E_c = E_c[\phi = 0] - q\phi$), $\hbar$ is the reduced Planck's constant, and V_{xc} is the exchange-correlation potential in the local density approximation: [8]

$$V_{xc}(\mathbf{r}) = -\frac{q^2}{4\pi^2 \epsilon_0 \epsilon_r} \left[3\pi^3 n(\mathbf{r}) \right]^{1/3}. \quad (5)$$

Nanocrystals are randomly oriented, therefore we prefer not to use the effective mass tensor for silicon, but only a single effective mass for the density of states $m = 0.32 m_0$, where m_0 is the electron mass at rest. Each eigenfunction Ψ_i of energy E_i has a degeneracy of 12, due to spin degeneracy and to the presence of six equivalent minima in the conduction band. If the dot is occupied by N electrons, and l and m are two integer such as $N = 12 \times l + m$ (with $m < 12$) the electron density reads

$$n(\mathbf{r}) = 12 \sum_{i=1}^{l} |\Psi_i(\mathbf{r})|^2 + m |\Psi_{l+1}(\mathbf{r})|^2 \quad (6)$$

under the assumption that the electron density in the dot is not appreciably different from that in the ground state.

The Poisson-Schrödinger equation is selfconsistently solved for several values of N and of the gate voltage V_G. The maximum number of electrons that can occupy a dot $N_{\max}$ is a function of V_G: if $\mu(N, V_G)$ is the chemical potential of the dot with N electrons and applied gate voltage V_G, and E_F is the Fermi energy in the substrate, $N_{\max}$ must satisfy the conditions

$$\mu(N_{\max}, V_G) < E_F; \qquad \mu(N_{\max} + 1, V_G) > E_F. \quad (7)$$

The chemical potential is computed with Slater's transition rule [11] as $\mu(N) = E_{N-1/2}$, where $E_{N-1/2}$ is the highest occupied eigenvalue of the system with $N - 1/2$ electrons, computed with density functional theory.

By keeping fixed the number of electrons and computing the electron density in the channel as a function of V_G, one can directly obtain the value of the threshold voltage for any number of electrons in the nanocrystal.

4 Results and discussion

The conduction band in the simulaton domain on the x-z plane for a 4 nm silicon dot and $\sigma_{nc} = 2.5 \times 10^{11}$ cm^{-2}, an applied gate voltage $V_g = 1$ V and 3 electrons in the dot is shown in Fig. 5 and the corresponding electron density in the dot in shown in Fig. 6. As can be seen, the

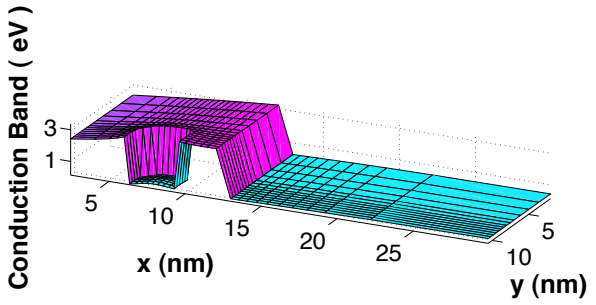

Figure 5: Conduction band in the x-z plane in the simulation domain of Fig. 4 for an applied gate voltage of 1 V and 3 electrons in the dot.

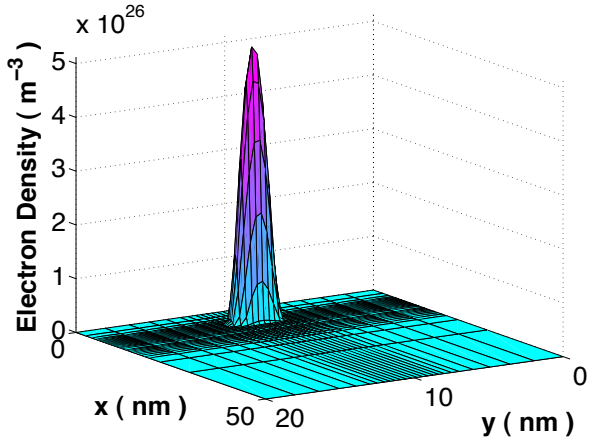

Figure 6: Electron density on the x-z plane in the simulatin domain of Fig .4 for an applied gate voltage of 1 V and 3 electrons in the dot.

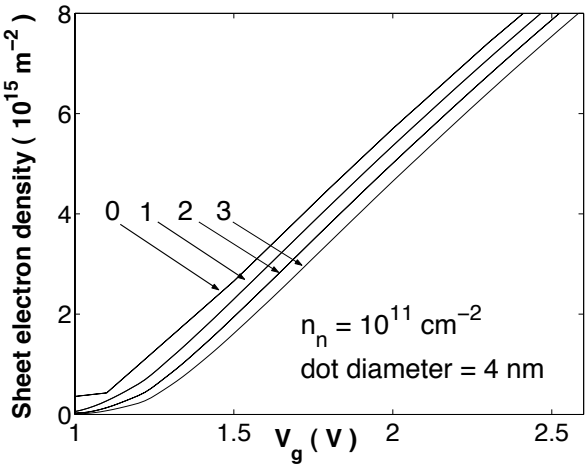

Figure 7: Sheet electron density in the channel as a function of the gate voltage for a number of electrons in the nanocrystal ranging from 0 to 3. Nanocrystals have a diameter of 4 nm and a surface density of 10^{11}cm^{-2}.

electron density has the shape of the first eigenfunction, with only one peak at the center.

In Fig. 7 we plot the sheet electron density in the channel as a function of the gate voltage V_G for a number of additional electrons in the nanocrystal ranging from 0 to 3. Data refer to a nanocrystal diameter of 4 nm and to a density $\sigma_{nc} = 10^{11}$ cm^{-2}. The threshold voltage shift is in this case approximately 60 mV per each stored electron. Since the threshold voltage shift is approximately proportional to the nanocrystal density, larger shifts may be obtained by increasing the nanocrystal density.

In Fig. 8 we plot the electrochemical potential μ of the dot as as a function of V_G for a number of electrons N ranging from 1 to 3, for a larger nanocrystal density of 10^{12} cm^{-2}. The Fermi level in the channel is zero, therefore the intercept of all the curves with the horizontal axis gives the gate voltage at which an additional electron can enter the nanocrystal, which is approximately 0.5 V. Other simulations, not reported, have shown that such value depends very weakly on nanocrystal density and size.

We have also started to take into account the effect of randomness in the nanocrystal layer, first focusing on a finite distribution of dot size. We have performed a conservative estimate of the effects of disorder, because for computational reasons we have to restrict ourselves to a simulation domain containing only one nanocrystal. In such a way, we believe we are underestimating the effects of disorder. By performing a set of simulations, we have obtained the sheet electron density in the channel as a function $f(d, V_g, N(V_w, d))$ of the external gate voltage V_g, of the dot diameter d, and of the number of electrons stored in the nanocrystal N, which is a function of the dot diameter and of the writing voltage V_w. If we suppose a statistical distribution in dot diameters $\rho_\sigma(d)$, we can write the charge density of the channel as:

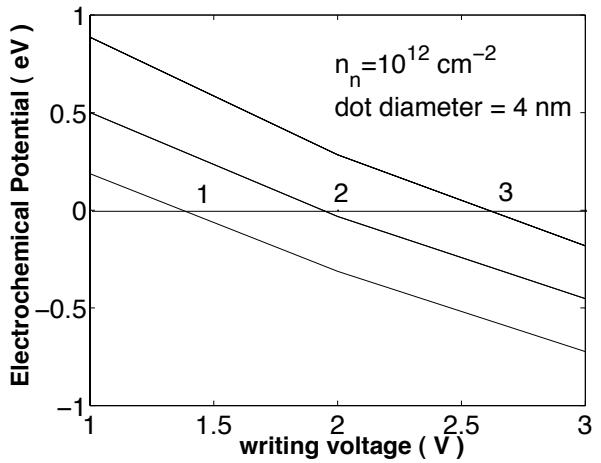

Figure 8: Chemical potential of the nanocrystal as a function of the gate voltage for a number of stored electrons ranging from 1 to 7.

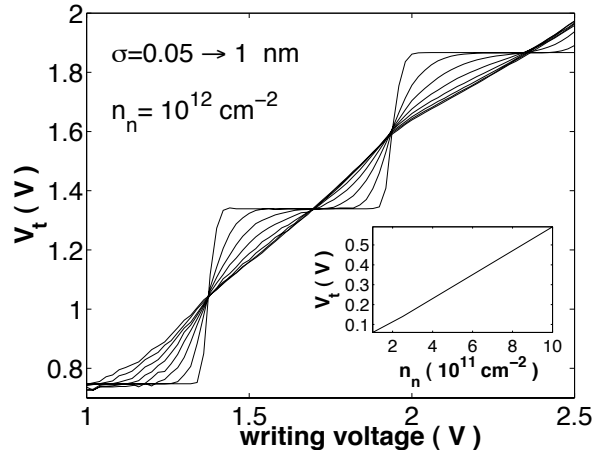

Figure 9: Threshold voltage as a function of writing voltage for a sheet density of 10^{12} cm^{-2} nanocrystals with diameter of 4 nm. The standard deviation of the nanocrystal diameter varies from 0.05 to 1 nm.

$$n(V_g, V_w, \sigma) = \int \rho_\sigma(d) f(d, V_g, N(V_w, d)) dd \quad (8)$$

where ρ_σ is a Gaussian distribution of average 4 nm, and standard deviation σ. From n, we can compute the threshold voltage as a function of V_w and σ. In Figure 9 we have plotted the threshold voltage as a function of the writing voltage for a diameter standard deviation ranging from 0.05 nm to 1 nm. For a standard deviation as small as 0.3 nm we lose the step-like behavior of the curve, consequently reducing the possibility of easy implementation of multi-bit storage schemes.

5 Conclusion

We have developed a numerical model for the three-dimensional quantum-mechanical simulation of nanocrystal Flash memories, and we have shown results for a typical device structure. The developed model is a useful tool for exploring the effects of process parameters and of geometry on the electrical properties of such memory devices.

For simplicity, we have considered a perfectly regular array of nanocrystals. A disordered distribution of nanocrystals would have an effect very similar to that of the random distribution of dopants in conventional MOSFETs, causing a statistical dispersion of V_T and of V_T-shifts. From this analogy, we can say that the relative dispersion of V_T-shifts increases when channel area is reduced, but decreases with increasing nanocrystal density σ_{nc}, and can be therefore kept under control by increasing σ_{nc} [10].

A very important aspect for the industrial application of non-volatile memories based on nanocrystal layers is the evaluation of write, erase, and retention times. Promising results have been obtained in experiments [3, 4, 5, 6, 7] and the issue has been partially addressed from the theoretical point of view in Ref. [12]. An in-depth analysis of this aspect is also needed to evaluate the maximum operating temperature as a function of the required retention time.

6 Acknowledgments

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