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Variations of the Power Dissipation in Adiabatic Logic Gates

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Abstract. The yield of adiabatic circuits strongly depends on the effects of parameter variations on the power dissipation. The dispersion of the threshold voltage has the most important impact on the yield. Different effects on the energy consumption due to interdie and intra-die variations of the threshold voltage are presented. Three logic families, the Efficient Charge Recovery Logic (ECRL), the Positive Feedback Adiabatic Logic (PFAL) and the 2N-2N2P are compared with respect to energy saving and operating frequency range. Finally it is shown that power dissipation variations due to parameter variations are strongly dependent on the logic family.

1 Introduction

A limiting factor for the exponentially increasing integration of microelectronics is represented by the power dissipation. Though CMOS technology provides circuits with very low static power dissipation, during the switching operation currents are generated, due to the discharge of load capacitances, that cause a power dissipation increasing with the clock frequency. The adiabatic technique prevents such losses: the charge does not flow from the supply voltage to the load capacitance and then to ground, but it flows back to a trapezoidal or sinusoidal supply voltage and can be reused. Just losses due to the resistance of the switches needed for the logic operation still occur. In order to keep these losses small, the clock frequency has to be much lower than the technological limit.

In the literature, a multitude of adiabatic logic families are proposed [1]-[11]. Each different implementation shows some particular advantages, but there are also some basic drawbacks for these circuits. For example one logic family [3] has a very large area occupation, other implementations ([2], [3], [6], [7], [9]) require several clock phases, or the functionality is strongly dependent on the transistors dimensions [8]. Up to date just few partial comparisons between different

adiabatic logic families can be found in the literature [12], [13]. However, no methodical investigations has been presented describing the robustness of such circuits. The goal of this paper is to compare different adiabatic logic families and to investigate their robustness against technological parameter variations. For this purpose three adiabatic logic families are evaluated and the impact of parameter variations on the power dissipation is determined. Both *interdie* (or global) and *intra-die* (or local) parameter variations of different components in the same sub-circuit are considered. The most important factor is the threshold voltage variation, especially for sub-micrometer processes with reduced supply voltage. This was also found for low voltage CMOS circuits, cf. [14], where the fundamental yield factor was the gate delay variation (in CMOS the power dissipation is not significantly dependent on the threshold voltage). For adiabatic circuits the timing conditions are not critical, because the clock frequency is particularly low, and therefore the outputs can always follow the clocked supply voltage. Here the yield critical requirement is the power dissipation that has a very low nominal value. Hence it exhibits large relative deviations due to parameter variations that can lead to the violation of the specifications.

Our investigations show that robustness of adiabatic circuits against parameter variations is significantly different for various circuit families. Global variations of the p-channel threshold voltage V_{th} affect the energy consumption in the adiabatic frequency range. Dissipation can increase up to more than 20% for global threshold voltage variations as low as 50mV.

2   Adiabatic Logic Families

Out of the many adiabatic logic families proposed in the literature three are chosen: the Efficient Charge Recovery Logic (ECRL) [7], that often is used as reference for evaluating the power dissipation of a new logic family, the Positive Feedback Adiabatic Logic (PFAL) [10], [11] and the 2N-2N2P [2].
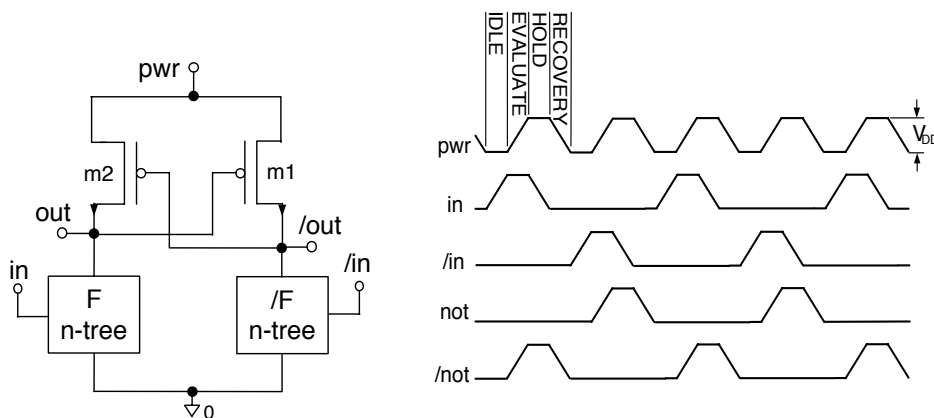

Fig. 1. General schematic (left) and timing of the NOT gate (right) for ECRL

2.1   Efficient Charge Recovery Logic

The first logic family we simulated is ECRL [7]. Figure 1 shows the general schematic for ECRL and the waveforms of the supply clock as well as I/O signals for a NOT gate. In order to recover and to reuse the supplied energy, an *ac* power supply is used for ECRL gates. As usual in adiabatic circuits, the supply voltage also acts as clock. Both *out* and $\overline{out}$ are generated so that the power
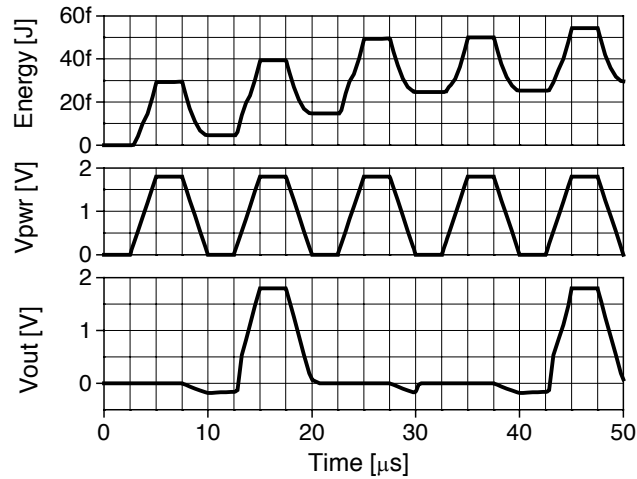

Fig. 2. From top to bottom: Supplied energy behavior, supply voltage and output voltage for ECRL family

clock generator can always drive a constant load capacitance, independent of the input signal. A more detailed description of ECRL can be found in [7].

If the circuit operates correctly, energy has an oscillatory behavior, because a large part of the energy supplied to the circuit is given back to the power supply, as shown in figure 2. As usual for adiabatic logic the energy behavior follows the supply voltage. In the same figure we may observe that, due to a coupling effect, the low level output goes to a negative voltage value during the recovery phase (that is, when the supply voltage ramps down). We define *"Dissipated Energy"* as the difference between the energy that the circuit needs to load the output capacitance, and the energy that the circuit gives back to the power supply during the recovery phase. The dissipated energy value depends on the input sequence and on the switching activity factor α, therefore the dissipated energy per cycle can be obtained from the mean value of the whole sequence. It can also be seen that a larger energy is dissipated if the input state changes and therefore the output capacitances have to switch.

2.2   Positive Feedback Adiabatic Logic

The structure of PFAL logic [10], [11] is shown in figure 3. Two n-trees realize the logic functions. This logic family also generates both positive and negative

outputs. The two major differences with respect to ECRL are that the latch is made by two pMOSFETs and two nMOSFETs, rather than by only two pMOSFETs as in ECRL, and that the functional blocks are in parallel with the transmission pMOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged. The ratio between the energy needed in a cycle and the dissipated one can be seen in figure 4. During the recovery phase, the loaded capacitance gives back energy to the power supply and the supplied energy decreases.
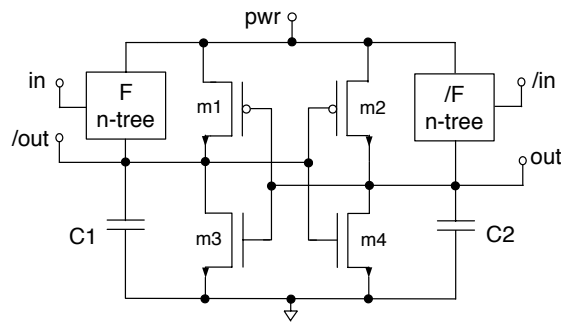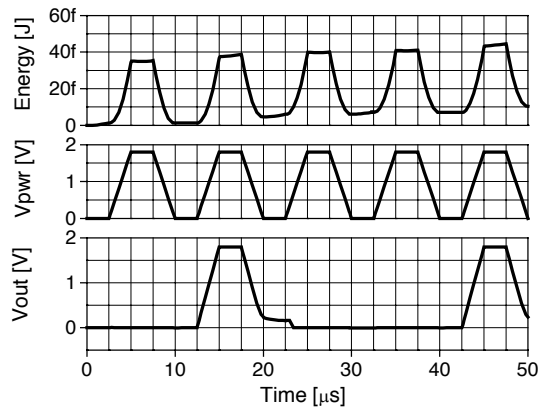
Fig. 3. General schematic for PFAL family

Fig. 4. From top to bottom: Supplied energy behavior, supply voltage and output voltage for PFAL family

2.3 2N-2N2P

This adiabatic logic family was derived from ECRL in order to reduce the coupling effect. Figure 5 shows the general schematic. The primary advantage of

2N-2N2P [2] over ECRL is that the cross-coupled nMOSFETs switches result in non-floating outputs for large part of the recovery phase.
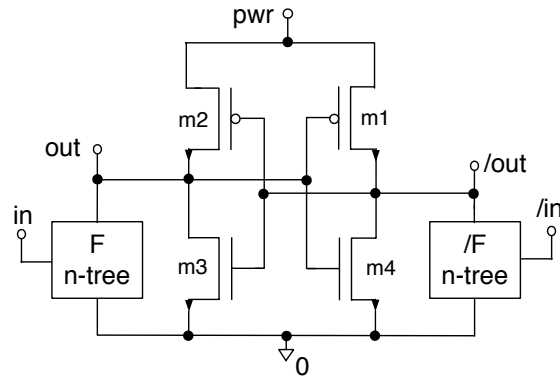

Fig. 5. General schematic for 2N-2N2P logic family

3   Influence of Parameter Variations on the Energy Consumption

The influence of threshold voltage variations on the power dissipation for the three introduced logic families is investigated by means of PSPICE simulations. In the considered 0.25μm CMOS technology the nominal threshold voltages of the n- and p-channel transistors are $V_{th,n} = 0.44V$ and $V_{th,p} = -0.43V$. Both in-terdie and intra-die parameter variations, in particular between the pMOSFETs
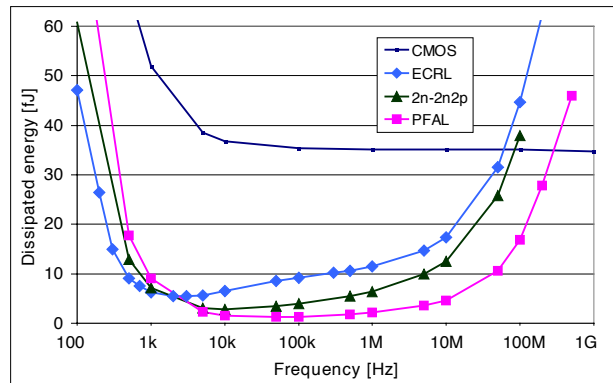

Fig. 6. Energy consumption per switching operation versus frequency for a CMOS inverter, an ECRL inverter, a PFAL inverter and a 2N-2N2P inverter in case of nominal threshold voltage. V_{DD} is 1.8V and C_{load} is 20fF.

of the inverter, are taken into account.

In order to determine the energy dependence on the threshold voltage and on the frequency the three adiabatic inverters are simulated for the whole useful frequency range.

Figure 6 shows the energy consumption per switching operation for the three logic families in case of *nominal* threshold voltage. As a reference the energy consumption of a conventional CMOS inverter is also plotted. The supply voltage V_{DD} is 1.8V and the load capacitance C_{load} is 20fF. For high frequencies the behavior is no more adiabatic and therefore the energy consumption increases. At low frequencies the dissipated energy increases for both CMOS and adiabatic gates due to the leakage currents of the transistors. Thus for each employed logic family an optimal interval for the operating frequency is obtained, that we call *"adiabatic frequency range"*. For f = 1MHz the ECRL, PFAL and 2N-2N2P inverters dissipate 30.9%, 6.2% and 18.3% of the energy dissipated by the CMOS inverter. For gates with a larger number of transistors, e.g. an adder [7], the adiabatic logic shows an even better improvement with respect to CMOS, because the number of transistors needed for an adiabatic implementation becomes comparable with those of the conventional CMOS implementation.
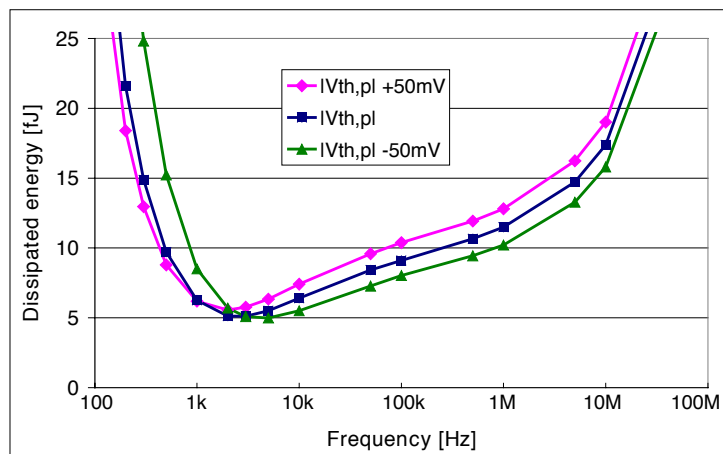

Fig. 7. ECRL inverter: Effect of global $V_{th,p}$ variations on the energy consumption.

For each simulated frequency the effects of both interdie (or global) and intra-die (or local) threshold voltage variations were determined. Figure 7 shows the energy consumption per switching operation for the ECRL inverter, in case of two *global* threshold voltage variations of pMOSFETs ($\Delta|V_{th,glob}| = +50$mV and $\Delta|V_{th,glob}| = -50$mV) and of nominal $|V_{th}|$. A dependence of the dissipated energy on the threshold voltage variations can be observed. At medium and high frequencies an increase of the dissipated energy corresponds to a larger absolute value of the threshold voltage $|V_{th}|$. The increase of the leakage

currents for smaller $|V_{th}|$ causes the energy dissipation rise at low frequencies. For PFAL and 2N-2N2P inverters the effect of global threshold voltage variations has the same qualitative trend of the ECRL inverter. At f = 1MHz and for $\Delta|V_{th,glob}| = +50mV$ the increase of the dissipated energy amounts to +11.5% for ECRL, +21.4% for PFAL and +15.2% for the 2N-2N2P inverter respectively. We also simulated the effect of an nMOSFET global V_{th} variation. In this case we could observe significant variations of the dissipated energy only in the low frequency range, where parasitic currents are significant. Since nMOSFETs do not switch during the phases where power changes, their V_{th} variations do not modify the circuit dissipation at medium and high frequencies.
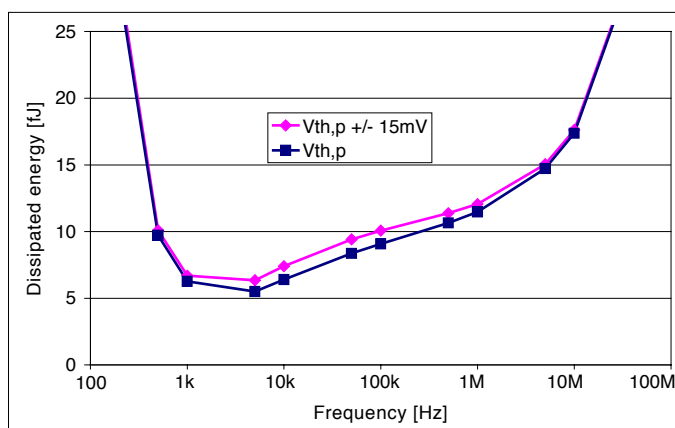

Fig. 8. ECRL inverter: Effect of local $V_{th,p}$ variations on the energy consumption.

Local variations are smaller than the global process tolerances. For the 0.25μm process and minimal dimension transistors, the standard deviation of the threshold voltage difference between neighboring transistors is approximately $\Delta V_{th,loc} = 30$mV and scales down in accordance with

$$\Delta V_{th,loc} \propto \frac{1}{\sqrt{W \cdot L}} \tag{1}$$

for larger area transistors [15]. However this presumes that a symmetric layout of transistor pairs optimized for the matching behavior is implemented, as it is typical for analog design. In usual digital layout style, these variations increase due to the effects of different parasitic elements and to proximity effects.

Figure 8 shows the effect of *local* threshold voltage variations. The local variation of a pMOSFET is simulated as a differential variation of two symmetrical pMOSFETs, that is one pMOSFET V_{th} is increased and the other V_{th} is decreased by the same value (in this case $\Delta V_{th,loc} = \pm 15$mV). Due to the asymmetry between the pMOSFETs, a larger short circuit current results, leading to an increase of the energy consumption.

NOT					
	Logic family		ECRL	PFAL	2N-2N2P
	Number of MOSFETs		4	6	6
	Energy minimum [fJ]		4.88	1.24	2.83
	E_{CMOS}/E_{adiab}		7.2	28.4	12.4
	Optimal frequency [kHz]		3	50	10
	Highest frequency [MHz]		100	200	100
1MHz	Dissipated Energy [fJ]		10.85	2.16	6.44
	E_{CMOS}/E_{adiab}		3.2	16.2	5.5
	Global $|V_{th,p}|$ variation (-50mV)		-11.2%	-18.6%	-14.2%
	Global $|V_{th,p}|$ variation (+50mV)		11.5%	21.4%	15.2%
	Local $V_{th,p}$ variation ($\pm15mV$)		5.1%	0.14%	2.1%
10MHz	Dissipated Energy [fJ]		17.37	4.61	12.57
	E_{CMOS}/E_{adiab}		2.1	7.6	2.8
	Global $|V_{th,p}|$ variation (-50mV)		-9.1%	-11.8%	-9.2%
	Global $|V_{th,p}|$ variation (+50mV)		9.4%	13.4%	10%
	Local $V_{th,p}$ variation ($\pm15mV$)		1.5%	0.07%	1.13%

Table 1. Summary of the results for adiabatic NOT gates

At medium and high frequencies the dissipated energy increases with a V_{th} variation, because a local V_{th} variation destroys the circuit symmetry, making one pMOSFET faster than the other in the latch circuit. At $f = 1$MHz, the ECRL NOT energy dissipation increase is equal to 5.1%. For PFAL and 2N-2N2P gates the effect of local threshold voltage variations is smaller than for the ECRL inverter. A local variation may occur also in a nMOSFET, but it does not introduce any relevant variation of the energy dissipation. Table 1 summarizes the results for all analyzed adiabatic NOT gates at $f = 1$MHz and $f = 10$MHz. The optimal frequency for the three adiabatic logic families is between $f = 3$kHz (ECRL) and $f = 50$kHz (PFAL). Adiabatic logic has a gain factor against the static CMOS implementation for frequencies up to 100MHz for ECRL and 2N-2N2P, and up to 200MHz for PFAL. At $f = 1$MHz, the gain factor is equal to 16.2 for PFAL, 5.5 for 2N-2N2P and 3.2 for ECRL. At $f = 10$MHz, a smaller gain factor is obtained.

We also simulated a NAND gate for the three adiabatic implementations. Table 2 shows the results for adiabatic NAND gates at $f = 1$MHz and $f = 10$MHz. The gain factor compared to static CMOS is equal to 2.9 for ECRL, 7.1 for PFAL and 4.2 for 2N-2N2P at $f = 1$MHz. Also in NAND gates the effect of local V_{th} variations for ECRL is stronger than for PFAL and 2N-2N2P (4.2% vs. 0.2% and 1.3%).

Due to an intrinsic smaller activity factor α of NAND gate both CMOS and adiabatic implementations dissipate less energy. For the adiabatic logic families the load capacitances have to be charged and discharged every cycle, similar to dynamic CMOS logic. As consequence adiabatic NAND gates show a lower

NAND					
	Logic family		ECRL	PFAL	2N-2N2P
	Number of MOSFETs		6	8	8
	Energy minimum [fJ]		3.36	1.65	2.30
	E_{CMOS}/E_{adiab}		5.1	10.4	7.5
	Optimal frequency [kHz]		10	50	10
	Highest frequency [MHz]		50	100	50
1MHz	Dissipated Energy [fJ]		6.01	2.43	4.14
	E_{CMOS}/E_{adiab}		2.9	7.1	4.2
	Global $|V_{th,p}|$ variation (-50mV)		-11.2%	-16.0%	-12.4%
	Global $|V_{th,p}|$ variation (+50mV)		9.9%	18.4%	13.1%
	Local $V_{th,p}$ variation ($\pm 15mV$)		4.2%	0.2%	1.3%
10MHz	Dissipated Energy [fJ]		10.23	4.83	8.20
	E_{CMOS}/E_{adiab}		1.7	3.6	2.1
	Global $|V_{th,p}|$ variation (-50mV)		-11.5%	-10.8%	-7.8%
	Global $|V_{th,p}|$ variation (+50mV)		3.9%	12.0%	8.20%
	Local $V_{th,p}$ variation ($\pm 15mV$)		1.3%	0.1%	0.8%

Table 2. Summary of the results for adiabatic NAND gates

gain factor compared to static CMOS. For more complex adiabatic gates, we expect a gain factor between that of NOT gates and that of NAND gates. First simulations for a 1-bit adder confirm our assumption.

4   Conclusions

For three adiabatic logic families the dependence of the power dissipation on interdie (or global) and intra-die (or local) threshold voltage variations has been characterized. Global variations determine an energy consumption increase with the p-channel threshold voltage $|V_{th}|$ in the adiabatic frequency range. At very low frequencies however, a decreasing $|V_{th}|$ produces an increase of the energy consumption due to the increased leakage currents of the transistors. In future technologies with reduced dimensions, these effects become more and more important.

The effects due to local threshold voltage variations are strongly dependent on the simulated logic family. For ECRL the effects on the energy consumption due to local ($\Delta V_{th,loc} = \pm$ 15mV) and global ($\Delta|V_{th,glob}| = +50mV$) threshold voltage variations are comparable (at f = 1MHz 5.1% vs. 11.5% for NOT, and 4.2% vs. 9.9% for NAND). The effect of local V_{th} variations on PFAL and 2N-2N2P is much smaller.

The decrease of the energy consumption for a lower global threshold voltage can also be considered as an option for future technology optimization. The power dissipation could be reduced at a given frequency or the maximum of the adiabatic frequency range could be enhanced.

The investigations show that robustness of adiabatic circuits against parameter variations is significantly different for various circuit families. Power variations can amount up to more than 20% for global threshold voltage variations as low as 50mV. Therefore, robustness has to be considered as a criterion for the choice of an adiabatic logic family and it is an important objective in the design of adiabatic circuits.

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