

Detailed modeling of nanocrystal flash memories

Giuseppe Iannaccone

Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni,
Università di Pisa

P. Coli

Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni,
Università di Pisa

G. Iannaccone*, P. Coli
Dipartimento di Ingegneria dell'Informazione
Università degli studi di Pisa, Via Diotisalvi 2
I-56126 Pisa, Italy, * e-mail: ianna@iet.unipi.it

We have developed a code for the simulation of the electronic properties of an array of semiconductor nanocrystals embedded in a thin dielectric layer. Such nanocrystal layers — stacked between the gate and the channel of a field effect transistor — can be effectively used as a storage medium for non-volatile memory applications, with perspectives of improved performance in terms of power consumption, ease of programming and shorter write-erase times with respect to conventional non-volatile memories. We show results from a detailed simulation based on the self-consistent solution of the Poisson-Schrödinger equation on a three-dimensional grid, focusing on the charging process and on the effect of charge stored in the nanocrystals on transistor threshold voltage.

I. INTRODUCTION

Functional nanocrystal layers for application in non-volatile and quasi-non-volatile memories have been recently proposed [1,2] and extensively studied in industrial and academic laboratories [3–7]. They can be used as a charge storage medium that promises to efficiently replace the polysilicon floating gates used in current EEPROMs (Electrically Erasable Programmable Read Only Memories) and Flash memories.

In particular, a few electrons trapped in a nanocrystal layer sandwiched between the gate and the channel of a Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), as in the example shown in Fig. 1a, can increase significantly the MOSFET threshold voltage, and therefore store a bit of information.

The operation of a memory based on nanocrystals is sketched in Figs. 1b-d. The memory is programmed by applying to the gate a positive voltage of a few V, that lowers the dielectric conduction band and enhances tunneling of electrons from the substrate to the nanocrystals (Fig. 1b). Electrons get trapped in the nanocrystal, since further tunneling to the gate is inhibited by the thick barrier. However, due to already observed Coulomb Blockade effects at room temperature [3], only a well defined number of electrons (depending on the applied gate voltage) can occupy each nanocrystal, so that charging of the nanocrystals is a self-limited process. When one electron is added to each nanocrystal the MOSFET threshold voltage increases in steps, so that both single and multi-bit storage is possible. The information stored in the memory is then simply read by measuring the saturation current corresponding to a given voltage applied to the gate.

When only reading voltages are applied to the gate, tunneling barriers are sufficiently opaque to prevent electrons from leaking out and therefore information is retained (Fig. 1c). Information is erased by applying a negative gate voltage that removes electrons from the traps (Fig. 1d). Given the small number of electrons involved in device operation, nanocrystal layers are very promising in terms of reduced power consumption, short program-erase times, and limited degradation after many write-erase cycles. Coulomb blockade provides interesting possibilities for multi-bit storage.

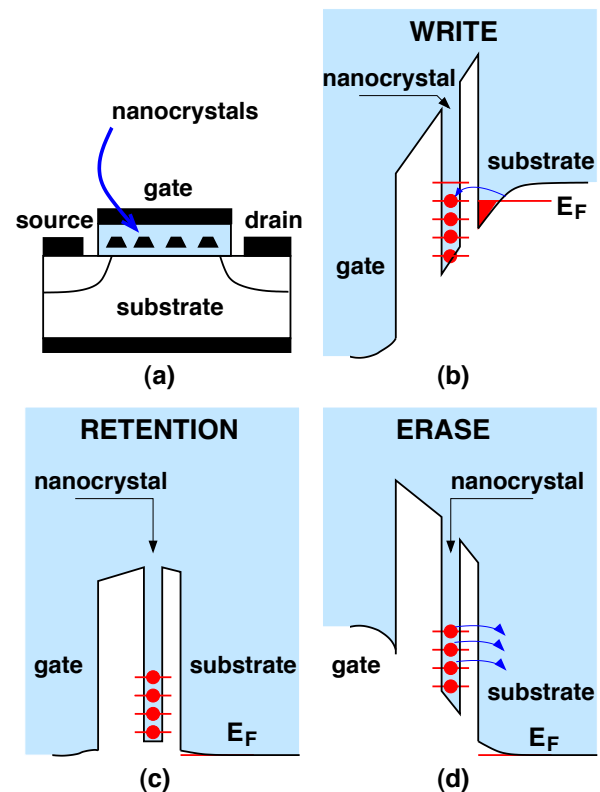


FIG. 1. (a) Sketch of the memory obtained with a nanocrystal layer stacked between the gate and the channel of a MOSFET; (b) conduction band profile along z when a positive voltage of a few V is applied to the gate and pictorial view of the write operation; (c) conduction band profile along z during the retention of information; (d) conduction band profile along z when a negative voltage of a few V is applied to the gate and pictorial view of the erase operation.

Several materials have been investigated for the nanocrystals and the dielectric layer, as shown in table

I. At present, Silicon Rich Oxide deposited by LPCVD on SiO_2 [4] and implanted Si or Ge in SiO_2 [5] are the most promising from the point of view compatibility with current CMOS technology, retention time and threshold voltage shift per electron.

II. BASIC FUNCTIONS OF THE NANOCRYSTAL LAYER

A simplified quantitative evaluation of the operation of such memories can be done by considering the equivalent capacitance circuit of the nanocrystal layer (Fig. 2): each nanocrystal is coupled to the top gate by a capacitance C_1 and to the bottom channel by a capacitance C_2 . A capacitance C_3 per each nanocrystals couples the gate and the channel (C_3 is the total direct capacitance between gate and channel divided by the total number of nanocrystals). The channel node is grounded. If an electron charge $-q$ is put in the nanocrystal, in order to keep the same charge in the channel node the gate voltage must be increased by a quantity

$$\Delta V_{th} = \frac{q}{C_1 + C_3(C_1 + C_2)/C_2}; \quad (1)$$

ΔV_{th} represents the threshold voltage shift obtained when one electron is added to each nanocrystal in the layer. As can be seen, in order to increase ΔV_{th} , one must reduce C_1 , i.e., reduce the size of the nanocrystal or increase the distance between dots and the top gate, and reduce C_3 , i.e., increase the nanocrystal density.

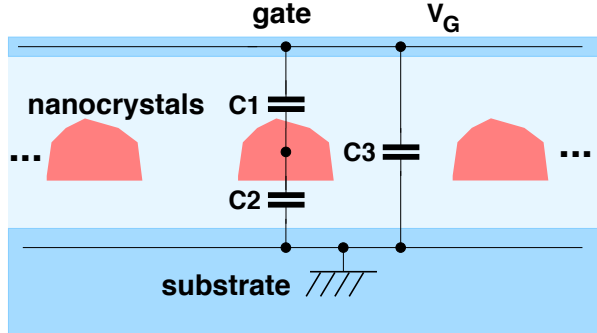


FIG. 2. Equivalent capacitance circuit of the nanocrystal layer: C_1 is the capacitance between nanocrystal and gate, C_2 is the capacitance between nanocrystal and channel, C_3 is the capacitance between channel and gate divided by the number of nanocrystals

On the other hand, the additional gate voltage required to win Coulomb repulsion and put one more electron into the dot in a state of energy E_0 is

$$\Delta V_G = \frac{q}{C_1} + E_0 \frac{C_1 + C_2}{C_1}; \quad (2)$$

again, a small value of C_1 and a strong confinement (large E_0) is required for obtaining a large ΔV_G .

III. THREE-DIMENSIONAL MODEL

Since the device structure is inherently three-dimensional and electrons in the dot are strongly confined (the nanocrystal diameter is usually in the range 3-10 nm), the circuit representation described above is not sufficient for obtaining accurate results. For this reason, we have developed a code for the self-consistent solution of Poisson and Schrödinger equations on a 3D grid, based on density functional theory with local density approximation. [9]

While nanocrystals are of course randomly distributed in the layer, we have considered a simplified situation where disorder is removed, that is, nanocrystals occupy a perfect two-dimensional lattice in the dielectric layer. Under this assumption, we can simulate only the region that represents the elementary cell of the lattice structure, and then apply periodic boundary conditions on the potential.

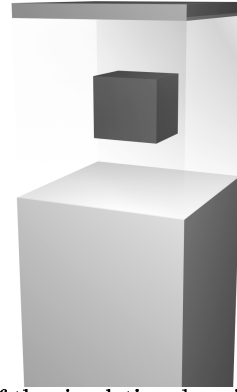


FIG. 3. View of the simulation domain: the nanocrystal is a silicon cube with 5 nm-edge, the thickness of the top and bottom oxide is 6 nm and 3 nm, respectively, the gate area considered is $10 \times 10 \text{ nm}^2$, corresponding to a nanocrystal density of 10^{12} cm^{-2} .

The device structure considered in our numerical simulations is a MOSFET with layer of silicon nanocrystals embedded in SiO_2 stacked between the gate and the channel. The simulation domain is shown in Fig. 3: without losing generality, we assume cubic dots with 5 nm-edge and average donor doping of 10^{19} cm^{-3} (here we will not consider the effect of discrete dopants). The thickness of the top and bottom oxide layer is 6 nm and 3 nm, respectively. The substrate has an acceptor doping of 10^{18} cm^{-3} and the gate is metallic. The surface density of nanocrystals is inversely proportional to the area of the considered domain on the horizontal plane: we consider an area of $10 \times 10 \text{ nm}^2$, which corresponds to a nanocrystal density of 10^{12} cm^{-2} .

The potential profile in our domain is determined by the Poisson equation

$$\nabla[\epsilon \nabla \phi(\mathbf{r})] = -\rho(\mathbf{r}) = -q[p(\mathbf{r}) - n(\mathbf{r}) + N_D^+(\mathbf{r}) - N_A^-(\mathbf{r})], \quad (3)$$

where ϕ is the scalar potential, p and n the hole and electron densities, respectively, N_D^+ and N_A^- the concentrations of ionized donors and acceptors, respectively, that depend on ϕ as indicated in Ref. [8]. While electrons and hole concentrations in the substrate are computed with the semiclassical approximation [8], electrons in the nanocrystal are strongly confined, and therefore their density is computed by solving Schrödinger equation with density functional theory:

$$-\frac{\hbar^2}{2} \nabla \cdot \left(\frac{1}{m} \nabla \Psi \right) + E_c(\mathbf{r}) \Psi - V_{xc}(\mathbf{r}) \Psi = E \Psi, \quad (4)$$

where E_c is the conduction band in the nanocrystal ($E_c = E_c[\phi = 0] - q\phi$) and V_{xc} is the exchange-correlation potential in the local density approximation [9]

$$V_{xc}(\mathbf{r}) = -\frac{q^2}{4\pi^2 \epsilon_0 \epsilon_r} [3\pi^3 n(\mathbf{r})]^{1/3}. \quad (5)$$

Nanocrystals are randomly oriented, therefore we do not use the effective mass tensor for silicon, but only a single effective mass m . Once the eigenfunctions Ψ_i and the corresponding eigenvalues E_i are obtained, the electron density corresponding to N electrons in the dot can be readily obtained as

$$n(\mathbf{r}) = \begin{cases} \sum_{i=1}^{N/2} 2|\Psi_i \mathbf{r}|^2 & \text{if } N \text{ is even} \\ \sum_{i=1}^{(N-1)/2} 2|\Psi_i \mathbf{r}|^2 + |\Psi_{(N+1/2)}(\mathbf{r})|^2 & \text{if } N \text{ is odd,} \end{cases} \quad (6)$$

since we assume that the electron density in the dot is not appreciably different from that in the ground state.

The Poisson-Schrödinger equation is solved for different N and gate voltages V_G . The maximum number of electrons that can occupy a dot N_{\max} is a function of V_G : if $\mu(N, V_G)$ is the chemical potential of the dot with N electrons and applied gate voltage V_G , and E_F is the Fermi energy in the substrate, N_{\max} must satisfy the condition

$$\mu(N_{\max}, V_G) < E_F; \quad \mu(N_{\max} + 1, V_G) > E_F. \quad (7)$$

The chemical potential is computed with Slater's transition rule as $\mu(N) = E_{N-1/2}$, where $E_{N-1/2}$ is the highest occupied eigenvalue of the system with $N-1/2$ electrons, computed with density functional theory.

By keeping fixed the number of electrons and computing the electron density in the channel as a function of V_G , one can directly obtain the value of the threshold voltage for any number of electrons in the nanocrystal.

IV. RESULTS AND DISCUSSION

The electron density in the nanocrystal in the x - z plane for an applied voltage of 1.2 V and occupancy of one

electron is plotted in Fig. 4. As can be seen, the electrons density has the shape of the first eigenfunction, with only one peak at the center.

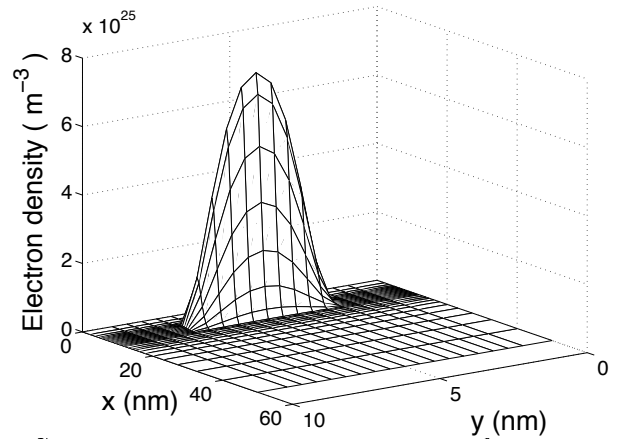


FIG. 4. Electron density on the x - z plane for an applied gate voltage of 1.2 V and one electron in the dot

In Fig. 5 we plot the sheet electron density in the channel as a function of the gate voltage V_G for a number of additional electrons in the nanocrystal ranging from 0 to 5 (thin solid lines). From those curves the threshold voltage can be obtained as the intercept on the horizontal axis of the line approximating each curve in the quasi-linear region. As can be seen, the threshold voltage with no electrons in the nanocrystal is $V_{T0} = 0.5$ V and increases of approximately 0.4 V per each stored electron.

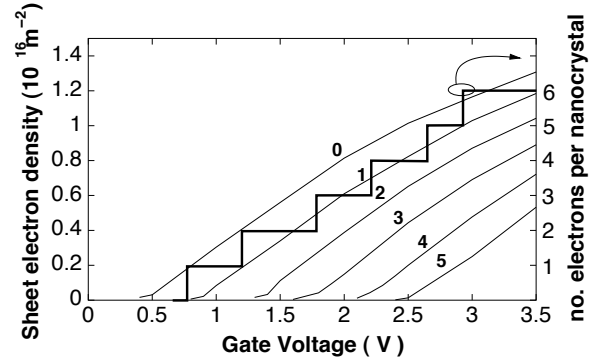


FIG. 5. Sheet electron density in the channel as a function of the gate voltage for a number of electrons in the nanocrystal ranging from 0 to 5 (left axis). Maximum number of electrons allowed in the nanocrystal as a function of the gate voltage (right axis).

In the same figure, on the right axis, we plot the maximum allowed number of electrons in the nanocrystal N_{\max} as a function of V_G . Steps are not uniform, and exhibit some shell filling effects, as expected. As can be seen, the gate voltage steps required to add the third and the seventh electron are larger than those corresponding to other electron numbers.

We can see from Fig. 5 that several options for write and read voltages are available. For example, one could program the memory to logical “1” by applying a voltage pulse of 2 V, thereby introducing 3 electrons in the nanocrystal and obtaining a threshold voltage $V_{T1} = 1.7$ V. Then a voltage $V_{GR} = 0.6$ V could be chosen to read the status of the memory, since it satisfies $V_{TO} < V_{GR} < V_{T1}$ and, in addition, it is small enough not to introduce any electron in a memory not programmed.

One very important aspect for the industrial application of non-volatile memories based on nanocrystal layers is the evaluation of write, erase, and retention times. While very promising results have been obtained in experiments [3–7] this issue is beyond the scope of the present paper and will be addressed in the near future.

V. ACKNOWLEDGMENTS

This work has been supported by the project NANOT-CAD [no. 10828] of the IST programme of the European Union.

-
- [1] S. TIWARI, F. RANA, H. HANAFI, A. HARTSTEIN, E. F. CRABBLE, and K. CHAN: *Appl. Phys. Lett.*, 1996, **68**, 1377-1379.
 - [2] S. TIWARI, F. RANA, K. CHAN, L. SHI, and H. HANAFI: *Appl. Phys. Lett.*, 1996, **69**, 1232-1234.
 - [3] I. KIM, S. HAN, H. HAN, J. LEE, H. SHIN: *IEEE Electron Device Lett.*, 1999, **20**, 630-631.
 - [4] Y.-C. KING, T.-J. KING, C. HU: *IEEE Electron Device Lett.*, 1999, **20**, 409-411.
 - [5] H. I. HANAFI, S. TIWARI, I. KHAN: *IEEE Trans. Electron Devices*, 1996, **43**, 1553-1558.
 - [6] T. MIZUTANI, T. INAYOSHI, Y. EGUCHI, S. KISHIMOTO, K. MAEZAWA: Tech. Digest IEEE Electron Device Meeting, 1999, 234-237.
 - [7] Y.-C. KING, T.-J. KING, C. HU: Tech. Digest IEEE Electron Device Meeting, 1998, 115-118.
 - [8] S. SZE, ‘Physics of Semiconductor Devices’, 2nd Edition, Wiley, New York, 1981.
 - [9] INKSON, Many body theory of solids — an introduction’, Plenum, New York, 1984.

dot/insulator material	ΔV_T per electron	retention time	Ref.
Si in SiO ₂	0.36 V	not shown	[1]
InAs/AlGaAs	0.25 V	1 h @ 100 K	[6]
Si or Ge in SiO ₂	0.3 V	≈ 1 h	[5]
SiGe/SiO ₂	0.4 V	1 day	[7]
SRO/SiO ₂	≈ 1 V	not shown	[4]
Si/Si ₃ N ₄ -SiO ₂	0.48 V	≈ 3 h	[3]

TABLE I. List of nanocrystal layers presented in the literature, with measured ΔV_T per electron and retention time