Adiabatic 4-bit Adders: Comparison of Performance and Robustness against Technology Parameters Variations

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ADIABATIC 4-BIT ADDERS: COMPARISON OF PERFORMANCE AND ROBUSTNESS AGAINST TECHNOLOGY PARAMETER VARIATIONS

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Abstract - **A large number of adiabatic families has been proposed, but there exist only few partial comparisons and no methodical investigations of the robustness of such circuits. Using a 4-bit adder as a reference circuit we compare different adiabatic logic families with respect to energy consumption, area occupation and frequency range. Significant differences among various adiabatic implementations are found and a reduction of energy dissipation compared to standard CMOS up to 200MHz. Energy saving by a typical factor of 10 can be achieved. The effect of supply voltage scaling is investigated as well as the sensitivity to technological parameters. It is shown that different effects due to inter-die and intra-die variations of the threshold voltage can strongly affect the performance of adiabatic circuits, increasing the energy dissipation by 7.7%.**

1. INTRODUCTION

Power consumption is an increasing concern in VLSI circuits. To meet the energy requirements new logic circuits have been developed alternatively to standard CMOS. The so-called adiabatic families reduce energy consumption due to the use of a pulsed power supply [1] - [7]. A slowly varying voltage source requires less energy to charge a capacitance if its period is longer than the time constant of the charging path [1] and furthermore, when the supply voltage decreases, the output capacitance is discharged and its stored energy can be recovered by the supply source. Up to date just few partial comparisons between different adiabatic logic families can be found in the literature [8, 9]. However, no methodical investigations have been presented describing the robustness of such circuits.

In a previous paper [10], we compared different adiabatic logic families by means of simple logic gates. The goal of this paper is to compare the architecture performances of adiabatic families with static CMOS and to investigate their robustness against technological parameter variations. The behavior of a reference circuit realized with different architectures and different adiabatic logic families but with the same process technology is examined and compared with the corresponding static CMOS circuit. Three dynamic adiabatic families operating with differential stages are considered. The used reference circuit is a 4-bit adder, which is a fundamental building block of digital ICs and, at the same time, it is sufficiently complex to address synchronization and cascading issues.

Our investigations show that adiabatic logic up to an operating frequency higher than 200MHz presents an alternative to conventional static CMOS for the realization of low-energy electronics. However, power consumption can be significantly affected by technology parameter variations, in particular by the fluctuation of the threshold voltage, and hence robustness of adiabatic circuits has to be taken into account.

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2. ADIABATIC LOGIC FAMILIES

The adiabatic logic families proposed in the literature are compared with respect to energy consumption, area occupation, and frequency range. Since the implementation and the distribution of many power clock phases requires additional area and power consumption, logic families with more than four phases are not taken into account. Moreover, due to the increase of energy dissipation caused by the use of diodes, logic families employing just MOSFETs are preferred. For these reasons, the following three families are chosen: the Efficient Charge Recovery Logic (ECRL) [2], the 2N-2N2P [3] and the Positive Feedback Adiabatic Logic (PFAL) [6, 7].

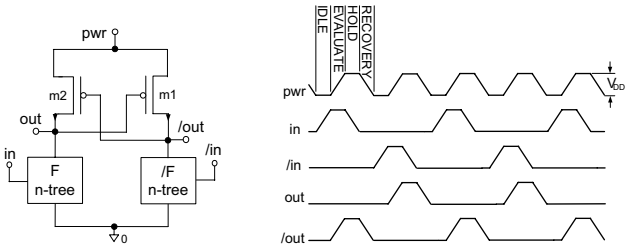

Figure 1: **General schematic (left) and timing of the inverter (right) for ECRL.**

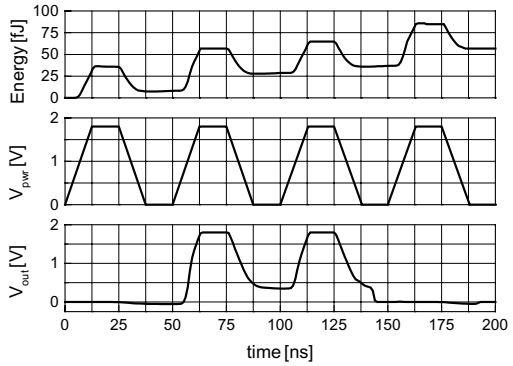

Figure 2: **From top to bottom: Supplied energy behavior, supply voltage and output voltage for ECRL family.**

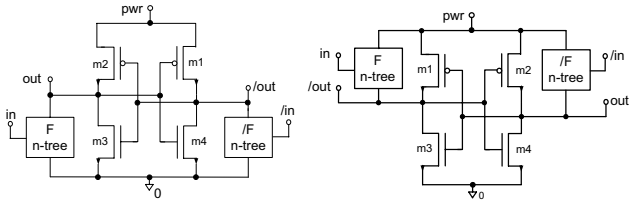

Figure 3: **General schematic for 2N-2N2P logic (left) and PFAL family (right).**

Fig. 1 shows the general schematic for ECRL and the waveforms of the supply clock as well as I/O signals for an inverter. In order to recover and to reuse the supplied energy, an AC power supply is used for ECRL gates. As usual in adiabatic circuits, the supply voltage also acts as clock. Both *out* and $\overline{out}$ are generated so that the power clock generator always drives a constant load capacitance, independent of the input signal.

If the circuit operates correctly, energy has an oscillating behavior, because a large part of the energy supplied to the circuit is given back to the power supply, as shown in Fig. 2. The energy versus time curve nearly follows the supply voltage. During the recovery phase (that is, when the supply voltage ramps down) the low level of V_{out} goes to a negative voltage value due to a coupling effect ($V_{out} \cong$ -50mV, not observable in the figure). We define *"dissipated energy"* as the difference between the energy needed to load the output capacitance and the energy that the circuit gives back to the power supply during the recovery phase.

The 2N-2N2P logic family (see Fig. 3, left) was derived from ECRL in order to reduce the coupling effect. The major difference with respect to ECRL is that the latch is made by two pMOSFETs and two nMOSFETs, rather than by only two pMOSFETs as in ECRL. The additional cross-coupled nMOSFET switches lead to non-floating outputs for a large part of the recovery phase.

The primary advantage of PFAL over ECRL and 2N-2N2P is that the functional blocks are in parallel with the transmission pMOSFETs (see Fig. 3, right). Thus the equivalent resistance is decreased when the capacitance needs to be charged, leading to a reduction of the energy dissipation at high frequency.

3. COMPARING DIFFERENT ARCHITECTURES

The 4-bit adder has been chosen as reference circuit because its complexity allows to investigate signal propagation and circuit robustness. A first figure of merit for the comparison between

	pipelined RCA			**RCA**			**RCA**
	ECRL	PFAL	2N-2N2P	ECRL	PFAL	2N-2N2P	CMOS
pMOSFETs	52	52	52	16	16	16	60
nMOSFETs	156	208	208	120	136	136	60
Area $[\mu m^2]$	13	16.25	32.5	8.5	9.5	14.5	11.25
	pipelined CLA			**CLA**			
	ECRL	PFAL	2N-2N2P	ECRL	PFAL	2N-2N2P	
pMOSFETs	64	64	64	44	44	44	
nMOSFETs	128	192	192	108	152	152	
Area $[\mu m^2]$	12	16	36	9.5	12.25	26	

Table 1: **Adiabatic 4-bit adders: Number of transistors and area occupation for different topologies and different adiabatic logic families compared with the best conventional static CMOS implementation**

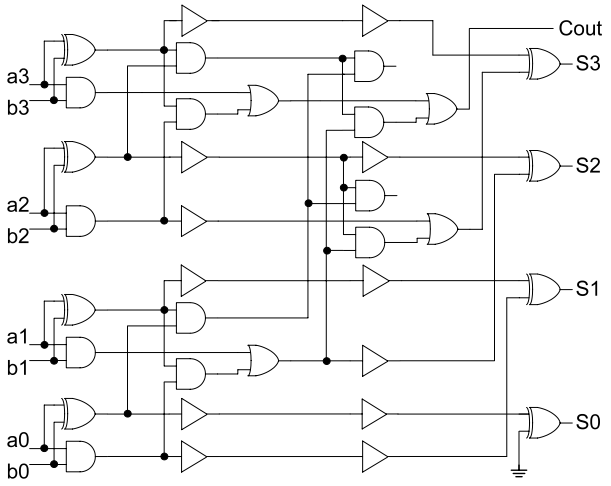

Figure 4: **Schematic design of the simulated pipelined 4-bit Carry Lookahead Adder.**

standard CMOS and adiabatic circuits is the area occupation. In Table 1, the number of transistors and an area estimation for different topologies of adiabatic 4-bit adders with and without pipeline are compared with a static CMOS Ripple Carry Adder (RCA), which represents the best solution for implementing a 4-bit adder in static CMOS. The area occupation value is obtained defining the nMOSFET dimensions to the minimum size allowed by the technology (nMOSFETs in these architectures only drive small currents). The choice of the optimal pMOSFET dimensions was made through a compromise to minimize the energy dissipation: a W/L increase reduces the pMOSFET channel resistance, but it also enlarges the capacitance C_{gs}, inducing a larger dissipation through the negative coupling voltage. The ECRL and the PFAL families have the lowest power consumption with minimum size pMOSFETs, while in the 2N-2N2P logic $W/L = 6$ is the optimum value for the pMOSFET dimensions.

For the adiabatic implementations also a Carry Lookahead Adder (CLA) realization was considered. Although the pipelined CLA is one of the most expensive with regard to the occupied area, it is preferred to a RCA because it has maximal throughput. It is worth noticing that some adiabatic implementations without pipeline require less area than the static CMOS one. The large area occupation required by 2N-2N2P is due to the higher W/L ratio chosen. The schematic of the simulated pipelined CLA is shown in Fig. 4. The needed logic blocks, i.e. AND, OR and XOR gates, can easily be implemented using each of the considered adiabatic logic families. We simulated the different implementations of the adiabatic 4-bit adder with PSpice according to a 0.25μm CMOS technology. The nominal threshold voltage of the n- and p-channel transistors is equal to $V_{th,n} = 0.44V$ and $V_{th,p} = -0.43V$, respectively.

4. PERFORMANCE COMPARISON

To calculate the average dissipated energy considering the dependency on the input configuration we introduced a numerical model based on the hypothesis that the transitions of input state producing an equal output activity factor induce the same energy dissipation. Thus, depending on the number of output transitions induced, the transitions of input state were divided in six *sets*. For every adiabatic family several input state transitions for each set were simulated, and the energy difference for all possible consecutive pairs of transitions was computed. Simulation results show

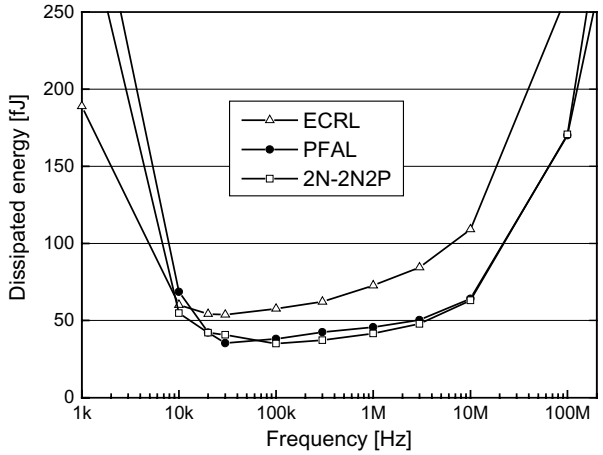

Figure 5: **Dissipated energy versus frequency for three adiabatic 4-bit adders. The conventional static CMOS Ripple Carry Adder under the same conditions dissipates 370fJ.**

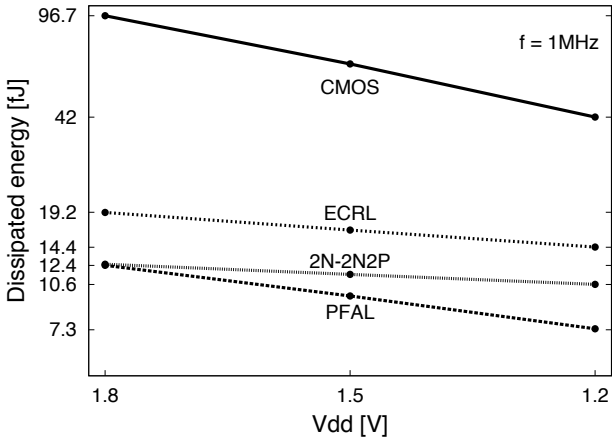

Figure 6: **Effect of $\mathbf{V_{dd}}$ scaling on the energy dissipation for 1-bit adiabatic adders and for the static CMOS RCA at f = 1MHz.**

that the dissipated energy difference caused by the input state transitions belonging to the same set is smaller than the energy difference caused by the transitions belonging to different sets. Hence, the average dissipated energy could be computed as the weighted average of the dissipated energy in each set considering the number of elements n for each set as weight.

Fig. 5 shows the results using the same technological parameters for each implementation. The average dissipation for the standard CMOS RCA is 370fJ, so in the medium frequency range (f = 1MHz) the adiabatic adders require between *10%* and *19.5%* of the energy dissipated by the standard CMOS adder. All curves are characterized by the same qualitative behavior: in the low frequency range, the energy mostly depends on the parasitic subthreshold current, and hence it decreases with frequency. In the medium frequency range there is the minimum dissipation, while in the high frequency range the load capacitance voltage does not closely follow the power supply clock, causing a larger voltage difference in the charging path and therefore increasing the energy dissipation. Thus for each logic family an optimal interval for the operating frequency is obtained, that we call *"adiabatic frequency range"*. In comparison with the standard CMOS RCA, the three

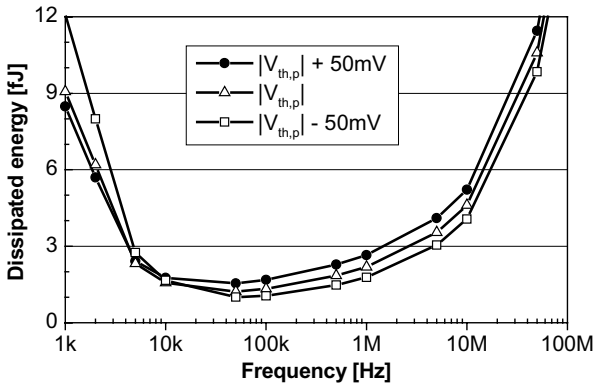

Figure 7: **PFAL inverter: Effect of global $\mathbf{V_{th,p}}$ variations on the energy consumption.**

simulated logic families allow to save energy up to a frequency higher than 200MHz.

Fig. 6 shows the effects of supply voltage scaling on the energy dissipation at f = 1MHz for three adiabatic 1-bit adders compared with static CMOS. As expected, the dissipation of the static RCA scales by a factor 2.25, according to V_{dd}^2. For the adiabatic adders, a scaling of the dissipated energy can also be observed. However, the scaling factor is lower and it depends on the logic family (1.18 for 2N-2N2P, 1.33 for ECRL and 1.7 for PFAL). For V_{dd} = 1.2V the adiabatic adders still dissipate between 2.9 and 5.7 times less energy than the static CMOS RCA.

5. ROBUSTNESS AGAINST TECHNOLOGICAL PARAMETER VARIATIONS

Both *inter-die* (global) and *intra-die* (local) parameter variations of different components in the same sub-circuit are considered. A global variation is for example due to the changes in process temperature or doping concentration. A local variation may be determined by a random deviation of the dopant concentration. The threshold voltage variation is the most important factor, especially for sub-micrometer processes with reduced supply voltage. For adiabatic circuits, the timing conditions are not critical, because the clock frequency is particularly low, and therefore the outputs can always follow the clocked supply voltage. Here the yield critical requirement is the power dissipation that has a very low nominal value. Hence, it may exhibit large relative deviations due to parameter variations that can lead to violation of the specifications. A global variation is simulated varying the threshold voltage of all pMOSFETs according to the typical standard deviation for the considered 0.25μm CMOS technology of 50mV. For simple adiabatic logic gates [10], power variations can reach up to 20% for global threshold voltage variations as low as 50mV (see Fig. 7).

If the absolute value of the pMOSFET threshold voltage $|V_{th,p}|$

Energy sensitivity $\Delta E/E$ to *global* $\|V_{th,p}\|$ variations				
Freq.	Variation	ECRL	PFAL	2N-2N2P
1MHz	$\Delta\|V_{th,p}\|$ = -50mV	-2.29%	-7.05%	-5.80%
	$\Delta\|V_{th,p}\|$ = +50mV	5.58%	7.66%	6.42%
10MHz	$\Delta\|V_{th,p}\|$ = -50mV	-4.40%	-7.64%	-4.42%
	$\Delta\|V_{th,p}\|$ = +50mV	3.37%	6.81%	4.79%

Table 2: **Adiabatic 4-bit adders: Effects of *global* threshold voltage variations on the energy dissipation**

is lowered, at medium and high frequencies the circuit dissipates less energy, because the residual charge on the load capacitance is lowered, and because the latch switches more rapidly. At low frequency instead, energy dissipation increases due to the rise of subthreshold current.
For the adiabatic 4-bit adders the dependency of energy dissipation on global variations, reported in Table 2 for two significant frequency values, shows the same qualitative trend but a lower sensitivity than for simple logic gates. It is worth noticing that the decrease of energy consumption in correspondence to a lower global threshold voltage could be considered as an option for future technology optimization. Using low V_{th} pMOSFETs, the power dissipation could be reduced at a given frequency and the maximum of the adiabatic frequency range could be enhanced.
Since nMOSFETs do only switch during the *hold* and the *idle* phases (see Fig. 1), their V_{th} variations do not modify the energy dissipation at medium and high frequencies. Hence, the effect of a nMOSFET global V_{th} variation affects the dissipated energy only in the low frequency range, where parasitic currents are significant.
The local V_{th} variation of a pMOSFET is simulated as a differential variation of two symmetrical pMOSFETs, that is one pMOSFET V_{th} is increased and the other V_{th} is decreased by the same value. In this case $\Delta V_{th,loc} = \pm$ 15mV is chosen because the standard deviation of the threshold voltage difference between neighboring transistors is approximately $\Delta V_{th,loc} = 30$mV for the considered process and minimal dimension transistors [11]. Of course, in a circuit there is a large number of possible local variations. The worst case occurs when the threshold voltages of the cross-coupled pMOSFETs (see Fig. 1 and 3) vary, since this results in a larger short circuit current, leading to an increase of the energy consumption (see Table 3). For static CMOS circuits, a compensation effect occurs due to the statistical distribution of the threshold voltage variations, so that the delay time of a gate chain has a smaller spreading than the single gates [12]. In adiabatic circuits instead, local $V_{th,p}$ variations always deteriorate the circuit performance and therefore a compensation effect for the variations of power dissipation cannot be observed.

Energy sensitivity $\Delta E/E$ to *local* variations			
$\Delta\|V_{th,p}\| = \pm$ 15mV			
Freq.	ECRL	PFAL	2N-2N2P
1MHz	3.17%	0.99%	1.27%
10MHz	0.54%	0.92%	0.85%

Table 3: **Adiabatic 4-bit adders: Effects of *local* threshold voltage variations on the energy dissipation**

6. CONCLUSIONS

Up to f = 200MHz adiabatic logic presents an alternative to conventional static CMOS for the realization of low-energy electronics. By means of 4-bit adders, different adiabatic logic families have been compared with respect to energy consumption, area occupation and frequency range. At f = 1MHz PFAL and 2N-2N2P implementations reduce energy dissipation by a factor of *10*, ECRL by a factor of *5.1* compared to a standard static Ripple Carry Adder. The influence of the supply voltage scaling on the energy dissipation was also investigated. For adiabatic adders a reduction of the dissipated energy could also be observed. At V_{dd} = 1.2V adiabatic adders still dissipate between 2.9 and 5.7 times less than the standard CMOS implementation. The sensitivity to technological parameter fluctuations and the dependency of energy dissipation on inter-die (global) and intra-die (local) threshold voltage variations have been characterized. For local threshold voltage variations, there is no compensation effect in case of statistical variations, as it occurs in static CMOS circuits. In presence of global variations the energy consumption increases with the p-channel threshold voltage $|V_{th,p}|$ in the adiabatic frequency range. In future technologies with reduced dimensions, these effects will become more and more important.
The investigations show that adiabatic 4-bit adders are more robust against parameter variations than simple adiabatic logic gates. However, the variations of the energy dissipation are still significant (7.7% for global threshold voltage variations as low as 50mV). Hence robustness should be regarded as a criterion for the choice of an adiabatic logic family. Finally, by the use of design centering tools it should be investigated if the effects of parameter variations can be reduced, so that an optimization of the parametric yield in the design of adiabatic systems can be obtained.

7. ACKNOWLEDGMENT

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8. REFERENCES

[1] W.C. Athas, L. Svensson, J.G. Koller *et al.*: Low-power digital systems based on adiabatic-switching principles. IEEE Transactions on VLSI System. Vol. 2, Dec. 1994, pp. 398-407
[2] Y. Moon and D.-K. Jeong: An efficient charge recovery logic circuit. IEEE Journal of Solid-State Circuits, Vol. 31, 1996, pp. 514-522
[3] A. Kramer, J.S. Denker *et al.*: 2nd order adiabatic computation with 2N-2P and 2N-2N2P logic circuits. Proc. Intern. Symp. Low Power Design, 1995, pp. 191-196
[4] V.G. Oklobdzija, D. Maksimovic *et al.*: Pass-transistor adiabatic logic using single power-clock supply. IEEE Trans. Circ. Syst. II, Vol. 44, Oct. 1997, pp. 842-846
[5] Y. Ye, and K. Roy: Energy recovery circuits using reversible and partially reversible logic. IEEE Trans. Circuits Syst. I, Vol. 43, Sep. 1996, pp. 769-778
[6] A. Vetuli, S. Di Pascoli and L.M. Reyneri: Positive feedback in adiabatic logic. Electronics Letters, Vol. 32, No. 20, Sep. 1996, pp. 1867ff
[7] A. Blotti, S. Di Pascoli and R. Saletti: Simple model for positive-feedback adiabatic logic power consumption estimation. Electronics Letters, Vol. 36, No. 2, Jan. 2000, pp. 116-118
[8] D.J. Frank: Comparison of high speed voltage-scaled conventional and adiabatic circuits. Proc. Intern. Symposium on Low Power Electronics and Design, ISLPED, Monterey, CA, Aug. 1996, pp. 377-380
[9] D. Mateo and A. Rubio: Design and Implementation of a 5x5 trits Multiplier in a Quasi-Adiabatic Ternary CMOS Logic. IEEE J. Solid-State Circuits, Vol. 33, July 1998, pp. 1111-1116
[10] E. Amirante, A. Bargagli-Stoffi, J. Fischer, G. Iannaccone and D. Schmitt-Landsiedel: Variations of the Power Dissipation in Adiabatic Logic Gates. Proc. 11th Int. Work. on Power And Timing Modeling, Optimization and Simulation, PATMOS'01, Yverdon-les-Bains, Switzerland, Sep. 2001, pp. 9.1.1-9.1.10
[11] R. Thewes: Matching of active and passive devices in analog CMOS applications. Tutorial International Conference for Microelectronic Test Structures, Monterey, California, 2000
[12] M. Eisele, J. Berthold, D. Schmitt-Landsiedel *et al.*: The Impact of Intra-Die Device Parameter Variations on Path Delays and on the Design for Yield of Low Voltage Digital Circuits. IEEE Trans. on VLSI Systems, Vol. 5, No. 4, Dec. 1997, pp. 360-368