# *On the occurence of few electron phenomena in ultra-scaled Silicon nano-crystal memories*

**G. Molas**
CEA-LETI, Grenoble
**Barbara De Salvo**
CEA-LETI, Grenoble
**G. Ghibaudo**
IMEP-CNRS/INPG Grenoble
**Giuseppe Iannaccone**
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
**D. Mariolle**
CEA-LETI, Grenoble
**A. Toffoli**
CEA-LETI, Grenoble
**N. Buffet**
CEA-LETI, Grenoble
**S. Lombardo**
IMM-CNR, Catania
**S. Deleonibus**
CEA-LETI, Grenoble

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# On the occurrence of few-electrons phenomena in ultra-scaled Silicon nano-crystals memories

G. Molas, B. De Salvo, G. Ghibaudo*, G. Iannaccone+
D. Mariolle, A. Toffoli, N. Buffet, S. Lombardo** and S. Deleonibus

CEA-LETI, 17 rue des Martyrs 38054 Grenoble Cedex 9, France molasga@chartreuse.cea.fr
(*) IMEP-CNRS/INPG Grenoble France, (+) University of Pisa, Italy, (**) IMM-CNR, Catania, Italy

## Abstract:

*In this work, we present the single electron charging and discharging phenomena occurring at room temperature in an ultra-scaled Silicon nano-crystals memory. A deepen investigation of the impact of critical dimensions of the memory cell (i.e. active area and channel width and length) on the memory programming window and on the size of the current discontinuities (induced by the variation of one electron in the floating gate) is reported here. Poisson-Schroedinger simulations allowing for a good understanding of experimental results are also shown.*

## 1. Introduction

As the dimensions of Flash memories are scaled down, new physical phenomena, as single electron effects [1], could seriously affect the whole memory operation and reliability. In fact, when the channel of the memory cell will be sufficiently small to be sensitive to a variation of one charge in the floating gate, the main characteristics of the memory operation will be no more governed by the statistical behaviour of a large number of electrons but, on the contrary, discrete events will become dominant. Thus, in order to predict the ultimate scaling limit allowing for reliable devices, the experimental and theoretical investigation of ultra-small memory devices is today of great importance [2, 3, 4].

## 2. Device

Our devices, named "Nano-Flash" devices (Fig1.a), were fabricated on 8" Silicon On Insulator wafers (Fig2.a). Several oxidations (LOCOS) were performed to create a ~15nm-thick active region and a 80nm-thick contact region (Fig2.b, c). A nanowire of variable width W (30nm to 400nm) and length (200nm), was defined by an hybrid lithography. In particular: the electrodes were defined in the thick Silicon regions by deep UV lithography, while the channel was defined in the thin Silicon region by e-beam (Fig.2d, e). The channel was n doped ($10^{18}cm^{-3}$) or intrinsic (p-Si, $10^{15}cm^{-3}$). The etching process of the channel was optimised in order to obtain a trapezoidal shape section, allowing for a uniform thermal oxidation. Afterwards, a tunnel dielectric of 2.5nm was made by Rapid Thermal Oxidation. The Silicon nano-crystals, which act as floating gates, are successively formed by depositing a 3nm-thick sub-oxide layer ($SiO_{0.5}$) followed by an annealing (1050°C, 3mn) (Fig.2f). The average diameter of the Si-dots was estimated by Transmission Electron Microscopy as ~3nm (see Fig.1b). A 20nm-thick control oxide (High Thermal Oxide) was deposited to cover the Si-dots array (Fig.2g). Finally, a 100nm-thick poly-Si gate of variable length L (30-200nm) was also deposited and defined by e-beam lithography (Fig.2h). Source and drain were n+ doped (As). Point contact devices, with the same gate stack dielectric, but with the channel presenting a constriction of 20nmx20nm and a control gate with a length L of 100nm have also been processed [5].

Finally, reference devices without Si-dot have also been fabricated in order to verify the role of Si-dots in the memory characteristics.

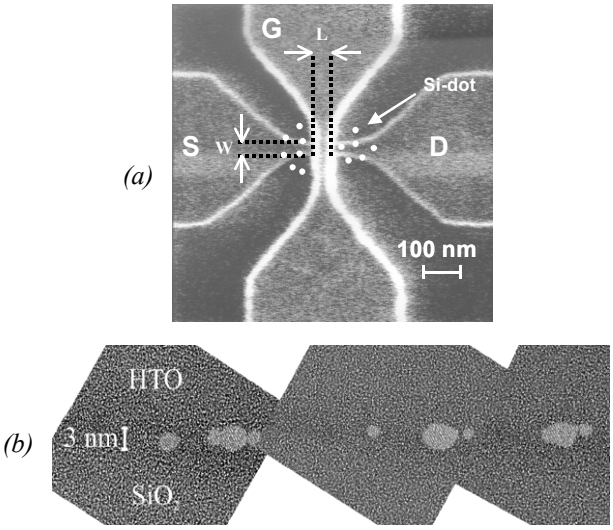


**Fig.1** - (a) Plan view of the nano-flash memory made by Scanning Electron Microscopy. (b) Transmission Electron Microscopy image of the Si-dots layer.

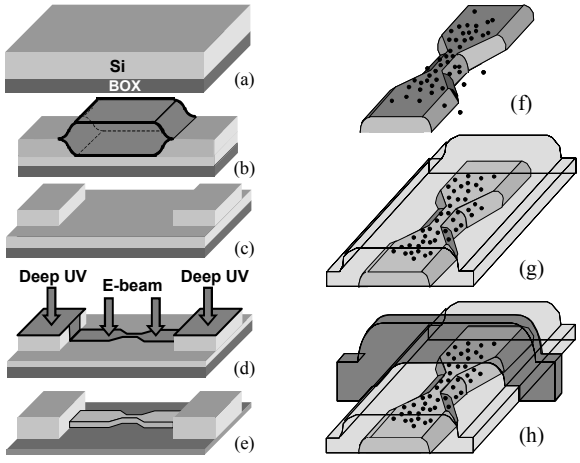


**Fig.2** - Schematic diagram of the nanoflash memory process.

## 3. Experiment and discussion

### *3.1 Influence of the cell active area on the memory charging/discharging behaviour*

We have studied the time evolution of the drain current after programming and after erasing (see Fig.3) on the nano-flash memory structures. The used gate voltage is chosen so that devices operate in the sub-threshold region. It should be mentioned that in large area Si-dots memories [6] a continuous charging/discharging behaviour was detected. In the nano-flash devices, on the contrary, staircases are clearly observed, each current discontinuity corresponding to the variation of one electron in a nano-crystal. In Fig.3, we can observe that the stepwise behaviour tends to disappear for the long and large area device.

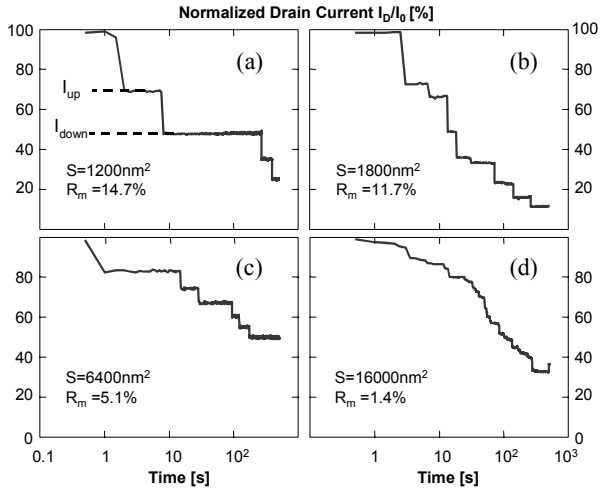


**Fig.3 -** Time evolution of the normalized drain current in the sub-threshold region for nano-flash devices with different surfaces (after a stress at $V_G$=-7V, $T_E$=20s). The characteristics have been normalised at their initial drain current values. The exact dimensions of the tested devices are : (a) W=30nm L=40nm; (b) W=30nm L=60nm; (c) W=80nm L=80nm; (d) W=80nm L=200nm.

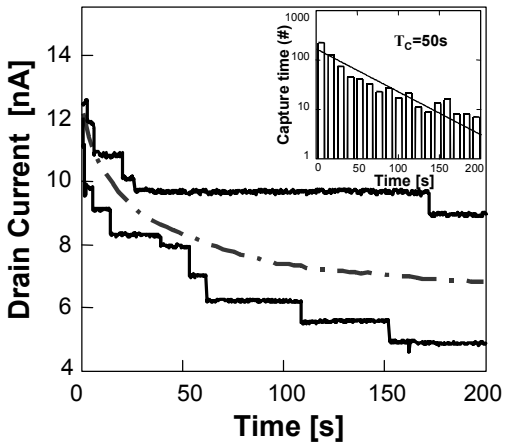


**Fig.4 -** Time evolution of the drain current after erasing on a point contact structure($V_G$=-0.6V, $V_D$=100mV). Solid lines correspond to two sequential measurements. The mixed line represents the mean value of the drain currents (nearly 100 runs, with average capture time as reported in the inset).

The Random Telegraphic Signal theory allows to evaluate the average drain current variation (below threshold) induced by the charge of an electron in a Si-dot, i.e.:

$$\log\left(\frac{I_{Up}}{I_{Down}}\right) = \frac{1}{s}\frac{q}{C_2} \propto \frac{1}{S} \qquad (1)$$

where $I_{up}$ is the current value before a current hump, $I_{down}$ the current value after a current hump, 1/s is the slope of the log[$I_D(V_G)$] curves, $C_2$ the dot to gate capacitance and S the active area (WxL). Note that we make the assumption that the effect of a charged Silicon dot is spread all over the area.

This formula indicates that the threshold voltage shift induced by one electron in a nano-crystal can be at the first order linked to the surface of the active region WxL, so the staircases phenomena is expected to disappear as the channel width and the gate length are increased. From Fig.3 we can calculate the mean value of the relative current discontinuity defined as $R_m$=mean(log($I_{up}/I_{down}$)). As we can see in this figure, the smaller the surface of the active region, the larger the current discontinuities and the value of $R_m$.

Note that the trapping and emission times are not reproducible from one measurement to another [3, 7], but a statistical analysis (see Fig.4) clearly shows that the charging and the emission times follow an exponential distribution law. Moreover, the average value of the measured currents (made over 100 experiments) converges to an exponential time evolution. These statistical results can be also qualitatively explained by the Random Telegraphic Signal (RTS) theory [8] which predicts an exponential behaviour for the charging/discharging times of a trap occupied by one electron.

### 3.2 *Influence of the cell linear dimensions on $\Delta V_{th}$*

We have investigated the influence of the width and of the length of the active area of the nano-flash structures on their programming window $\Delta V_{th}$. To this aim, we have measured the $\Delta V_{th}$ at 1nA (in the sub-threshold region) on about ten devices (each one corresponding to a different chip on the wafer) for each different couple of linear dimensions. The results are given in Fig.5. The wide dispersion of the threshold voltage shift, especially in ultra-small devices clearly appears. Several factors can explain this dispersion. Firstly, the number of Si-dots can fluctuate from one device to another, and this is more critical as the cell active area, so the number of active dots, scale down. Secondly, the random position of the Si-dots can induce the presence of percolation paths different from one device to the other. Thirdly, the tunnel oxide thickness (nominal tunnel oxide is about 2.5nm, so in the direct-tunnelling regime) can slightly fluctuate from one chip to the other, with a great influence on the written characteristics. On the other hand, we can see that the mean value of $\Delta V_{th}$ increases as the width of the device decreases (see Fig5.a). The Id(Vg) of samples with same L and different W (with $\Delta V_{th}$ close to the mean values) are given in Fig6.a. As recently reported by other authors [4], two phenomena can be invoked to justify this result, as illustrated in Fig.6b.

Firstly, in a narrow channel device, the charged Si-dots cut more easily the conduction paths than in a large device, due to the absence of percolation paths. Secondly, the role of the Si-dots located on the lateral sides of the channel, becomes more and more critical as the channel width is reduced. Thus a larger threshold voltage shift is expected in a narrow channel memory device. On Fig.6c, we have plotted the evolution of the $\Delta V_{th}$ with W measured in weak and in strong regimes. The measurements have been made at three different current levels, corresponding to the sub-threshold regime and the strong inversion regime. We can observe that the sensitivity of $\Delta V_{th}$ with the channel width W is more important in the sub-threshold region, but still exists in strong inversion. Indeed, this result implies that the effect of the Si-dots on the lateral sides of the channel plays the major role in the dependence of $\Delta V_{th}$ with W. In fact, the percolation is expected to play a role in the sub-threshold region, and not in strong inversion where the carriers are much less sensitive to the potential fluctuations in the channel. On the contrary, the effect of the Si-dots on the lateral sides of the channel should be seen in weak and in strong inversion (as in our case).

On the other hand, as shown in Fig.5b, we have also observed that $\Delta V_{th}$ increases with the channel length. Once again, the two previous enounced phenomena can be invoked. In fact, the probability to have a cluster of charged Si-dots giving rise to a bottleneck effect [4] in the channel or on the sides of the channel is higher in a long channel device than in a short one.

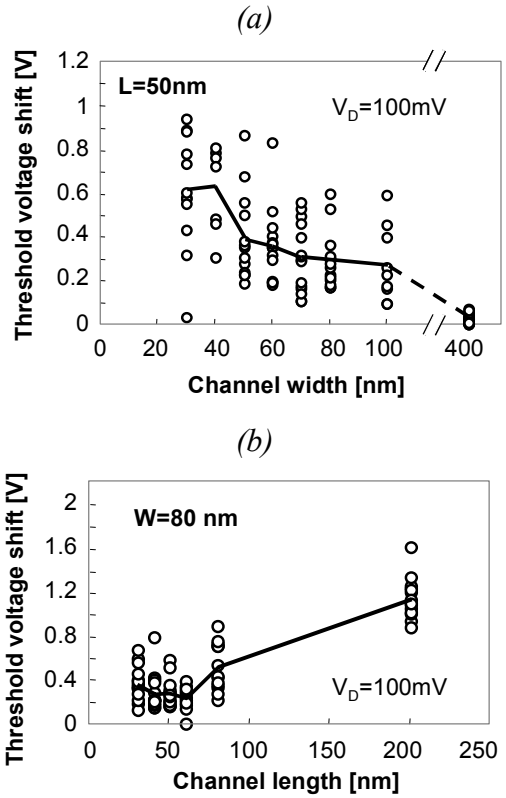


**Fig.5 -** Evolution of $\Delta V_{th}$ measured at 1nA (sub-threshold region) with the channel width (a) and length (b). Each circle corresponds to the $\Delta V_{th}$ value measured on one chip. The mean value of $\Delta V_{th}$ is also represented by a solid line.

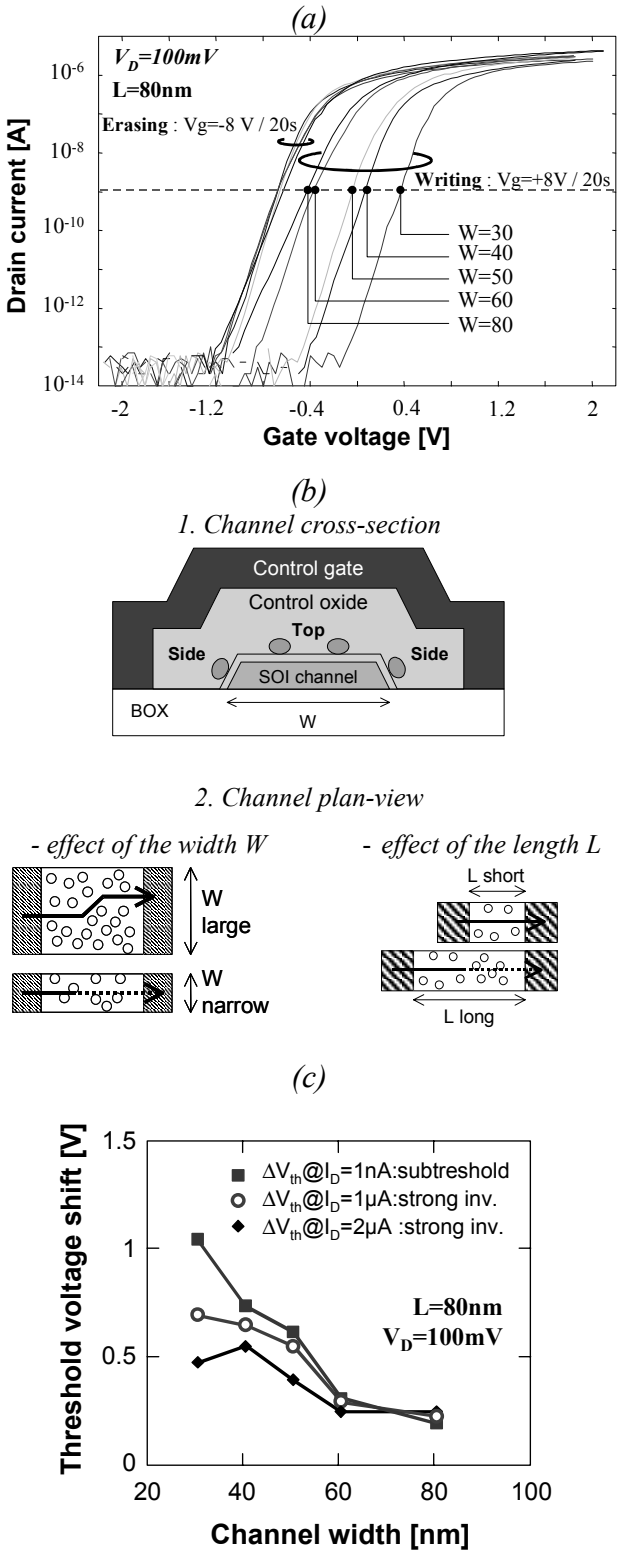


**Fig.6 -** (a) Drain current versus gate voltage of written and erased nano-flash devices (with $\Delta V_{th}$ close to the mean value, Fig.5a) with different channel width W. The characteristics have been shifted to superpose the erased curves. (b) Schematic views of the memory channel showing : 1. the impact of the dots over the lateral sides of the channel; 2. the impact of the reduction of W and L on the conduction path in the memory channel. (c) Evolution of $\Delta V_{th}$ with the channel width W measured at different current levels (in the sub-threshold region and in strong inversion).

## 4. Numerical Simulations

In order to investigate the effect of the presence of lateral Silicon dots on the observed dependence of $\Delta V_{th}$ on W we have performed a numerical simulation of the two-dimensional device cross section with a self-consistent Poisson-Schroedinger solver. The considered structure is illustrated in the inset of Fig.7. For simplicity, we have assumed a rectangular cross section for the wire, and we have replaced the layer of quantum dots with a uniform dielectric layer 4-nm thick with a charge density per unit volume corresponding to one electron per dot ($2.5 \times 10^{18}$ $cm^{-3}$). The Schroedinger equation is solved with density functional theory in the Silicon wire, taking into account effective mass anisotropy [9].

In Fig. 7 we plot the theoretical threshold voltage shift, in the case of one electron per Si-dot, as a function of wire width W. As can be seen, results are in qualitative agreement with those of Figs. 5 and 6. Roughly, the computed $V_{th}$ shift is between three and four times the experimental value, leading us to provide an estimate of the actual average electron number per dot of 0.25-0.3, that is consistent with results obtained in similar structures [4].

However, let us point out that a two-dimensional simulation does not allow us to take into account three-dimensional effects that may have a significant influence on $\Delta V_{th,}$ such as charge sharing with the source and drain contact, and the effect of the discrete distribution of Silicon dots, in the order of few tens per device. The former aspect should have some relevance, since the sub-threshold swing of the simulated device (infinitely large L) is close to 60mV/decade, while from Fig. 6 the experimental device has s=100mV/decade. The latter aspect should be relevant well below threshold, when hopping conduction and percolation may dominate transport, and should mainly represent an additional source of dispersion of $\Delta V_{th.}$

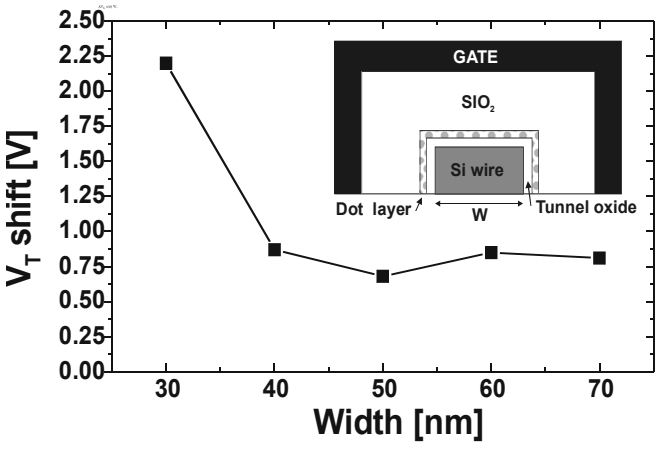


**Fig.7 -** Theoretical $V_{th}$ shift as a function of wire width for one electron per dot, obtained from a two-dimensional solution of the Poisson-Schroedinger equation. Short channel effects and the effects of random dot positioning is not considered.

## 5. Conclusion

We have demonstrated the occurrence of single electron storing processes at room temperature in a Silicon nanocrystal memory. The impact of the device dimensions on the electrical characteristics of the memory devices have been investigated. Numerical simulations allow to see the dominant role of Si-dots located on the lateral sides of the narrow channel on the programming window of the memory device.

## 6. Acknowledgements

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## 7. References

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