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Abstract— We have derived a set of consistent design criteria for the RF section of long range passive RFID transponders, operating in the 916 MHz and 2.45 GHz ISM frequency ranges. In particular, we describe the design criteria for the voltage multiplier, for the power matching network between the antenna and the non linear circuit represented by the voltage multiplier, and for the modulator of the backscattered radiation. We discuss the various design tradeoffs and determine the regions of the design space that allow us to maximize the operating range of the RFID system.

I. INTRODUCTION

Dense networks of low-power, low-cost, and low-data-rate wireless sensors (or "smart tags") are envisaged in recent scenarios of Ambient Intelligence [1]. For such networks to be practically deployed, present available choices are not completely satisfactory.

Indeed, on the one hand we have wireless networks based on the Bluetooth standard characterized by link datarates up to 780 kbps, nodes with reasonable computational capabilities, but also by a transceiver power consumption not lower than 50 mW, requiring the use of (to-be-frequently-recharged) batteries [2].

On the other hand, we have microwave RFID systems based on *passive* transponders, that extract power for operation (few μWs) by rectifying the RF signal transmitted by the *reader*, but have only a very simple logic state machine on board, sufficient for performing basic memory read and write operations. The reader also is the master of the minimum-size RFID network, has an on-board microprocessor, and is charged by batteries, since a power dissipation of the order of few hundreds mW is required for supplying power to the transponders in the range of few meters.

An interesting trade-off between the options described above would be represented by an RFID network of *passive* transponders carrying a very simple microprocessor on-board. Such choice would allow the introduction of more complex functionalities in the nodes and consequently in the network.

In this paper, we propose a very specific architecture for the RF section of passive transponders of a wireless identification and sensor network and discuss the related design options and tradeoffs. Here, we do not discuss the implementation of the microprocessor, that has to be realized with subthreshold logic schemes to reduce power dissipation below 1 μW.

In order to achieve an operating range of several meters, desired for several applications, it is necessary to reduce the power consumption of both the analog and digital sections of the tag to the sub-μW regime and to increase the power efficiency of the voltage multiplier at least over 15%.

To achieve such a performance, the circuit architecture of the voltage multiplier has to be optimized and the non-linear input impedance of the voltage multiplier has to be quasi-matched to the antenna.

Most of the passive and semi-passive RFID systems that operate in the UHF or microwave range exploit the backscatter modulation to transmit data from transponder to reader. The backscatter modulation consists in modulating the impedance seen by the transponder's antenna with the data signal, in order to modulate the reflected wave [3]. It is clear that the larger the variation of the impedance seen by the antenna, when modulating, the larger the modulation depth and the signal-to-noise ratio at the reader. However, the larger the variation of the impedance seen by the antenna, the larger the mismatch, and therefore the smaller the DC power converted by the voltage multiplier.

In order to maximize the operating range, it is important to achieve a difficult trade-off between minimum error probability at the reader, and maximum DC conversion efficiency.

The digital section of the transponder consists of a simple general purpose processor, 6502 compatible, with a clock frequency of 1 MHz and an addressable space of 64 Kbytes. Such processor will implemented with subthreshold logic schemes, CMOS and Pseudo-NMOS, with a supply voltage of 0.6 V, that allows us to maintain the power consumption below 1 μW. All results discussed in the paper are referred to the AMS 0.35 μm BiCMOS process. We show that by an appropriate choice of the modulation depth, a passive RFID system in the ISM 2.45 GHz band (916 MHz) with a digital section dissipating about 1 μW, can reach an operating range of more than 4 m (10 m), for a data-rate of few kbps, and that once a maximum operating range of 4 m (10 m) is fixed, a data-rate larger than 30 kbps (180 kbps) can be achieved.

II. N-STAGE VOLTAGE MULTIPLIER

An N-stage voltage multiplier consists of a cascade of N peak to peak detectors (a 2-stage voltage multiplier is used in the RF section shown in Fig.1). Let us suppose that a sinusoidal voltage, V_{in}, with a frequency f_0 and an amplitude V_0 is applied at the input of the voltage multiplier. In order to have a small ripple in the output voltage, capacitances have to be dimensioned so that their time constant is much

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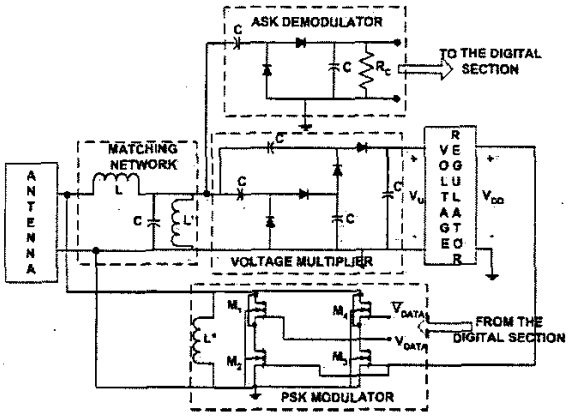

Figure 1: RF Section of a Passive Transponder.

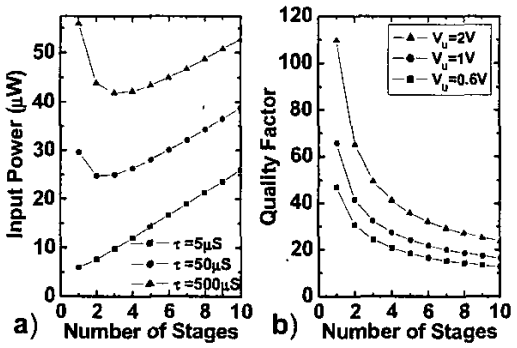

Figure 2: a) Average input power vs. number of stages for an output voltage of 0.6 V and an output power of 1μW ($\tau = R_{SUB}(\omega C_{SUB})^2$), b) Q-factor of the matching network vs. the number of stages for an output power of 1μW.

smaller than the period of the input signal, that is, $1/(2\pi R_L C) << f_0$, where C is the blocking capacitor and R_L is the equivalent load resistance (V_U divided by the output current of the voltage multiplier). In this way, the voltage applied to all C capacitors and the output voltage can be considered a DC voltage. In such condition the input-output characteristic is implicitly given by,

$$\left(1+\frac{V_U}{R_L I_S}\right)\exp\left(\frac{V_U}{2NV_T}\right)=B_0\left(\frac{V_0}{V_T}\right), \qquad (1)$$

where V_T is the thermal voltage and B_0 is the modified Bessel function of zero order. Solving (1) by numerical iteration, for a fixed output voltage and power consumption, it is possible to note that the higher the number of stages, the smaller the amplitude of the input voltage required to obtain a given DC output voltage and power consumption, even if for large N the amplitude of the input voltage almost saturates, since voltage multiplication is limited by the voltage drop of the diodes. The average input power, P_{IN} required to obtain a given output voltage and power, can be calculated by summing up the average power, P_D, dissipated in each diode and the power, P_L, transferred to the load. Taking into account substrate losses, the average input power is given by,

$$P_{IN}=2NI_S V_0 B_1\left(\frac{V_0}{V_T}\right)\exp\left(-\frac{V_U}{2NV_T}\right)+\frac{N}{2}V_0^2 R_{SUB}(\omega_0 C_{SUB})^2 \qquad (2)$$

where R_{SUB} and C_{SUB} are the substrate resistance and capacitance, respectively [4]. In Fig. 2a P_{IN} obtained from (2) is plotted as function of N: it is possible to note that for small substrate loss, the optimum power efficiency is obtained using a single stage; then, the optimum number of stages increases with increasing substrate loss. If we use an LC matching network, the Q-factor of the LC matching network is bound to the resistance transformation ratio [5] and its expression is given by $Q=\sqrt{R_{eq}/R_A-1}$, where R_A is the antenna resistance and *Req* is the equivalent input resistance of the voltage multiplier, considering the power consumption, that is, $R_{eq}=V_0^2/2P_{IN}$. Assuming a λ/2 dipole antenna (antenna resistance 72 Ω), the diagram of $Q(N)$ is plotted as function of N in Fig. 2-b. Although the highest power efficiency is reached with a number of stages corresponding to the minima in Fig. 2a, the choice of the number of stages has to be done taking into account that achievable values of Q are only up to some tens. Once the number of stages N is fixed, solving the equation $P_{IN}(I_S)$ for a given value of the output voltage and power, it is possible to find that the higher is the diode area and then the saturation current of the diodes and the better is the power efficiency of the voltage multiplier [6]. However, it is not possible to excessively increase the diode area otherwise the diode capacitance would become comparable with the capacitances of the voltage multiplier. Such situation would lead to a reduction of the efficiency because only a fraction of the input voltage would drop across the diodes due to the capacitive divider between voltage multiplier capacitances and diode capacitances. While Schottky diodes are typically preferred because of their larger I_S, the choice of p-n junctions allows us to use a cheaper CMOS process.

III. POWER MATCHING

The equivalent input impedance of the voltage multiplier might be represented, as a zero-order approximation, by the parallel of a resistance and a capacitance. In the high frequency analysis of the voltage multiplier, all the capacitances of the voltage multiplier can be considered as short-circuited and so all diodes can be considered in parallel or anti-parallel with the input. As a consequence, at the input of the voltage multiplier, the capacitances of all diodes are in parallel. The equivalent input resistance, R_{eq}, of the voltage multiplier is the resistance calculated from power consumption. Using an LC power matching network, the values of L and C are chosen as: $L=QR_A/\omega_0$ and $C=Q/R_{eq}\omega_0$ [5], where, R_A is the resistance of the antenna and Q is the quality factor of the LC network $Q=\sqrt{R_{eq}/R_A-1}$. An inductance L', in parallel with the input of the voltage multiplier, can be used to compensate the equivalent input capacitance of the voltage multiplier. Since the input capacitance due to the capacitances of the diodes is variable with the voltage across diodes, the inductance L' is dimensioned in order to resonate with the average value of the input capacitance at the operating frequency. It is clear that the power matching, achieved as described above, is reasonable provided that the variations

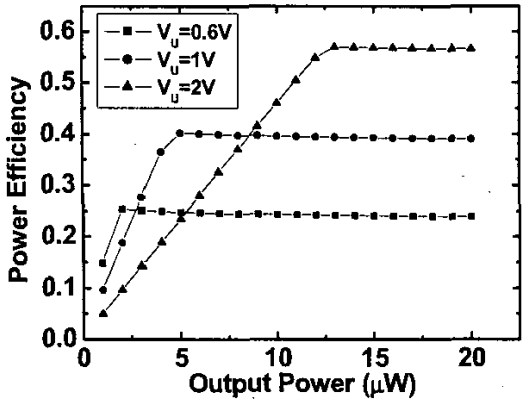

Figure 3: Power Efficiency of a single stage voltage multiplier as function of the output power for three values of the output voltage

of the input impedance, due to the variations of the input capacitance around the mean value are small with respect to the equivalent input resistance [6]. This leads to the condition,

$$\Delta C << \frac{Q}{2\pi f_0 R_{eq}} \tag{3}$$

where ΔC is the maximum variation of the input capacitance of the voltage multiplier with respect to its mean value. Once fixed the minimum diode area, allowed by the IC technology used, and the output voltage, from (3) we can derive the maximum equivalent input resistance of the voltage multiplier and then the minimum output power we can obtain, so that the power matching can be done correctly. Now we can suppose that for the application we are interested to, it is sufficient to have an output power smaller than the minimum value obtained from (3). It is possible to demonstrate that in this case we can optimize the power efficiency by putting a resistance R in parallel with the input of the voltage multiplier, to decrease the input resistance of the voltage multiplier down to the value calculated from (3), even if the power efficiency is reduced with respect to an N-stage voltage multiplier, due to the power dissipated in the resistance R [6]. Referring to the AMS 0.35μm IC technology, using diodes with an area of 1 μm^2, one obtains the diagram shown in Fig. 3, where, for small output power, the effect of the resistance added in parallel is apparent.

Since the voltage multiplier is a non-linear circuit, it is important to consider the non-linear effects on power matching. Because of the non-linear effects of the voltage multiplier, the current in the antenna also contains components at frequencies that are integer multiples of the operating frequency. Such effect is important when the quality factor of the power matching network is low and therefore higher harmonics are not strongly suppressed. In this condition, we can place a parallel LC network at the input of the voltage multiplier, resonating at the operating frequency. Such network has no effect on the first harmonic but strongly suppresses higher harmonics of the current in the antenna [6].

IV. BACKSCATTER MODULATION

By properly modulating the impedance seen by the transponder's antenna with the data signal, it is possible to obtain a ASK or PSK backscatter modulation. The impedance seen by the transponder's antenna is given by the parallel of a resistance, R, and an imaginary impedance, jX. In order to obtain an ASK modulation, we can suppose that the impedance seen by the antenna is real ($X>>R$) and it is modulated by the data signal between two values R_1 and R_2; the backscatter power can thus be modulated [3]. In order to obtain a PSK modulation, the imaginary part of the impedance seen by the antenna is modulated with the data signal between $\pm jX$; the phase of the wave reflected from the transponder can thus be modulated [3]. It is possible to show that for a fixed modulation depth, PSK backscatter modulation ensures a larger power available for power supply but the ASK backscatter modulation guarantees a smaller bit-error rate at the receiver [4, 6]. Since, as we shall see later, the transponder power supply typically limits the operating range, the PSK backscatter modulation is to be preferred, even if it requires a coherent receiver at the reader (while ASK does not). The PSK backscatter modulator is shown in the scheme of Fig. 1. Depending on the data signal level, either M1 or M4 conducts leading to a different output capacitance, since the two transistors have different sizes. The inductor L* makes the variation of the imaginary part of the impedance seen by the antenna symmetric with respect to zero. Transistors M2 and M3 allow us to obtain an output resistance of the modulator much larger than the antenna resistance so that only a negligible fraction of the power at the antenna goes to the modulator. Since also the demodulator has a power consumption much smaller than that one of the voltage multiplier, almost all the power, P_{IN}, at the antenna goes to the input of the voltage multiplier. In order to ensure the correct operation of the transponder, the input power, P_{IN}, must be larger than the minimum power necessary for transponder operation. The DC power required by the transponder is constituted by the power, P_{MOD}, dissipated by the modulator and the power, P_{DIG}, dissipated by digital section. Since such power has to be supplied by the voltage rectifier, the power required by the transponder has to be multiplied by the power efficiency η of the voltage rectifier, in order to obtain the minimum input power required for the correct operation of the transponder. As consequence, the following relation has to be fulfilled [6].

$$\frac{P_{EIRP}}{4\pi r^2} A_e \frac{4X^2}{R_A^2 + 4X^2} > \frac{1}{\eta}\left(P_{MOD} + P_{DIG}\right) \tag{5}$$

Another important condition to ensure correct operation of the tag-reader system is related to the probability of error at the receiver [6]. The signal, received by the reader's antenna, consists of two components: the PSK backscattered signal coming from the transponder's antenna and an un-modulated carrier reflected by scattering objects close to the antenna (clutter). The receiver must be able to remove the un-modulated signal, which would introduce an error in the demodulation due to its random phase. To this aim, the baseband receiver filter must have a zero-average impulse response, to block the un-modulated carrier. Since the impulse response of the filter has to be equal to the elementary impulse of one of the two symbols, the previous condition imposes an appropriate choice of the data coding,

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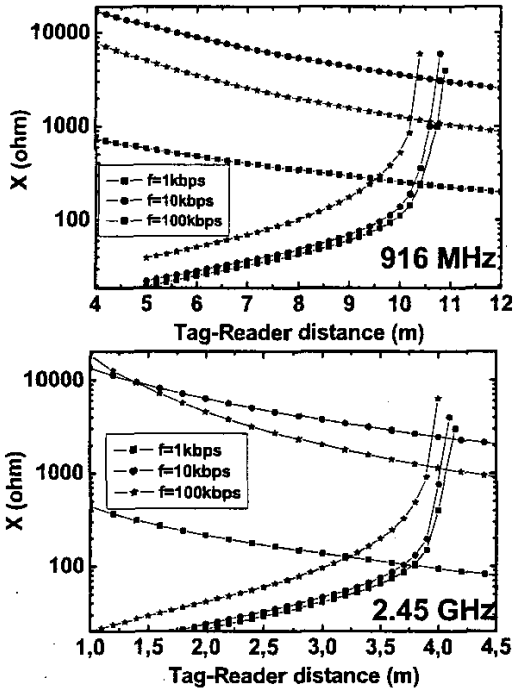

Figure 4: X values that satisfy (5), (6) as function of the distance between reader and transponder for three values of the data-rate and for an operating frequency of 916 MHz (top) and 2.45 GHz (bottom).

since only the data codes where at least a symbol is coded with a zero mean value waveform are acceptable [6]. The most common data codes, such as Manchester, unipolar RZ coding, DBP, Miller coding, verify such condition. The noise at the input of the receiver consists of a thermal noise component, due to the antenna, and a phase noise component, introduced by the frequency synthesizer. Indeed, since the reader works in full duplex mode, the un-modulated carrier, affected by the phase noise, goes to the input of the receiver because of both the power leakage between transmitter and receiver and the reflection of the transmitted carrier with objects close to the antenna. Since the two noise sources are uncorrelated, the variance of the input noise is obtained by summing up the variance of the two noise sources. Then the noise at the output of the receiving filter is obtained by filtering the input noise. The phase noise also affects the down conversion, leading to a shift of the constellation of symbols. Referring to a unipolar RZ coding and assuming that the transmission of '0' and '1' have the same likelihood, the detector's threshold can be chosen in accordance with the MAP criterion [5] and the total probability of error, P_e, is given by [6],

$$P_e = \frac{1}{2}\left\{Q\left\{\frac{A[\sin(\theta)-\sin(\theta+\varphi)-\sin(\theta-\varphi)]}{2\sigma}\right\}+ \right.$$
$$\left. +Q\left\{\frac{A\sin(\theta)}{2\sigma}\right\}\right\} \qquad (6)$$

where $Q(x)$ is the error function, A is the amplitude of the received backscattered signal, $1/T$ is the data-rate, σ is the standard deviation of the filter output noise, φ is the standard deviation of the jitter associated to the local oscillation and θ is the modulation depth. In order to guarantee reasonable receiver performances, the total probability of error has to be smaller than a given probability of error, P_e*. Considering two values for f_0 (2.45 GHz and 916 MHz), P_e*=10^{-3}, P_{DIG} = 1 μW, V_U=0.6 V, and supposing to use a dipole antenna for both transponder and reader, we can plot the values of X that satisfy (5) and (6) as a function of the distance between reader and transponder. From Fig. 4, it is possible to note that by a proper choice of the modulation depth, the operating range, for a passive RFID system can be larger than 4 meters at 2.45 GHz, and 10 meters at 916 MHz. It is also possible to note that for a data-rate larger than some kbps, the thermal noise is prevalent with respect to the phase noise and then increasing the data-rate, the range for a given X becomes smaller because the bandwidth of the receiver filter and the output noise power increase; for a data-rate smaller than some kbps, the phase noise is prevalent with respect to the thermal noise and then increasing the data-rate, the range for a given X becomes larger because the phase noise decreases. We can also determine the maximum data-rate, once the maximum operating range is fixed. It is possible to demonstrate that, for a maximum range of 4 meters and for a frequency of 2.45 GHz, the maximum data-rate is about 30 kbps; for a range of 10 meters and for a frequency of 916 MHz, the maximum data-rate is about 180kbps, both larger than typical datarates of RFID systems.

V. CONCLUSIONS

This paper presents the design criteria for the RF section of passive transponders in the 916 MHz and 2.45 GHz ISM bands, with the main aim of maximizing the operating range of the system. In particular we have derived and discussed the design tradeoffs for the voltage multiplier and for the backscatter modulator. Though our considerations are applicable to generic passive transponders, we have focused in particular on the options that would allow us to extract a DC power of 1 μW with a 0.6 V supply DC voltage that would allow us to put on-board a very simple microprocessor operating with subthreshold logic.

We have shown that with such criteria very interesting performances are achievable, in terms of operating range and data-rates, opening promising perspectives for the deployment of passive RFID systems in Ambient Intelligence or Ubiquitous Computing applications.

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