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Abstract:

In this paper we present a series voltage regulator for long distance passive RFID transponders, operating in the 868/916 MHz and 2.45 GHz ISM frequency ranges. The circuit has been implemented in a 0.35μm BiCMOS technology. Measurements show that the voltage regulator can provide a regulated voltage of 0.6 V, for an output current from 0 to 5 μA, with a quiescent current of only 34 nA, a minimum voltage drop of 30 mV and an output resistance of 100 Ω. Measurements also show a very good PSRR, particularly in DC and at the operating frequency of the tag-reader system, where it is smaller than -58 dB and -54 dB, respectively.

1. Introduction

FOR passive UHF and Microwave RFID (Radio Frequency Identification) transponders an extreme attention to low power issues is key to their widespread adoption in the field of identification systems and to their possible migration to ambient intelligence scenarios [1]. In particular, the actual and practical use of passive transponders is determined by their operating range, which is in turn limited by the minimum required radiation intensity at the antenna sufficient for transponder operation. This is particularly true in the European Union, where very strict regulations limit the power transmitted by the reader to 500 mW EIRP [2]. In such conditions, transponder operation must require only few μW of regulated DC power supply, in order to achieve an operating range of a few meters. In order to achieve such a goal, it is necessary 1) to reduce the power consumption of both the analog and digital sections of the tag to the μW or sub-μW regime, 2) to optimize the power efficiency of the voltage multiplier and the modulation depth [3].

Therefore, the voltage regulator must be able to supply a DC power of only few μW, must have a very small quiescent current, in the order of few tens of nA, and must be able to provide the regulated voltage with a voltage drop as small as possible, in order to minimize the amplitude of the unregulated voltage required for the correct operation of the transponder.

To our knowledge, there are no examples in the literature of series regulators with similar specifications, probably because the application we envisage is extremely low power. Indeed, the lowest power voltage regulators presented in literature provide output currents of some tens of mA and have quiescent currents of a few tens of μA [4, 5]. As can be seen, they would absorb the whole power budget of a passive long distance RFID transponder.

Here, we present a regulator with a quiescent current of only 34 nA and with a low voltage drop in order to maximize the power efficiency and therefore minimize the required radiation intensity at the antenna.

The architecture of the complete passive RFID transponder is shown in Fig.1. The input voltage V_{DDlow}, which has to provide almost all the power required for transponder operation, will be generated by a single stage voltage multiplier, that is shown to provide the maximum power efficiency in the conversion from the RF energy at the transponder's antenna to the DC power supply at the output of the voltage regulator [3]. For the digital section, that we shall not discuss here, we choose an implementation based on subthreshold CMOS logic, with a standard 0.35μm CMOS process, a regulated supply voltage V_{REG} = 0.6 V, and a clock frequency ≤ 1 MHz, which enables sub-μW power consumption. In order to ensure the correct operation of the voltage regulator, a supply voltage V_{DDlow} few tens of mV larger than V_{REG} is sufficient. However, such voltage would not be sufficient to ensure the correct operation of the error amplifier and to generate the reference voltage V_{REF}. As a consequence, a second stage is added to generate the higher voltage V_{DDhigh} that has only to provide the very small power required for the error amplifier and the voltage reference generator. In such a way, power efficiency can be maximized.

In this paper we focus on the design and on the measured performances of the series voltage regulator realized with AMS 0.35 μm BiCMOS technology. In Section II and III we will present the design of the voltage regulator and in Section IV we will show the experimental results.

2. Reference Voltage Generator

The circuit used to generate the reference voltage is shown in Fig. 2. It consists of a circuit that generates a current, I_0, almost independent of the supply voltage, which is injected into a diode, to generate the reference voltage [6]. In the current generator, in order to ensure that the currents in the two branches are as close as possible when varying the supply

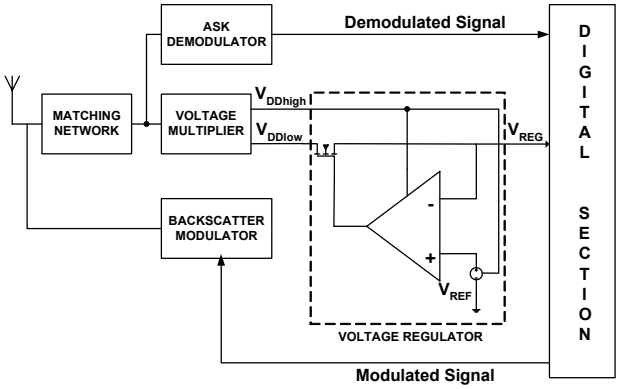

Figure 1: Passive Transponder Architecture.

voltage V_{DDhigh}, a cascode current mirror is used. We choose to use a bipolar rather than a CMOS cascode current mirror because in our IC technology PMOS transistors have a too large threshold voltage (0.75 V) leading to a strong reduction of the dynamic range of the voltage regulator. Assuming identical currents in the two branches, the current I_0, in Fig. 2, has the expression shown below,

$$I_0 = \frac{2}{R^2}\left(\frac{1}{\sqrt{k_1}} - \frac{1}{\sqrt{k_2}}\right)^2, \tag{1}$$

where $k = \mu_n C_{ox} W / L$ for each transistor. In order to show the importance to use a Cascode current mirror in the circuit that generates the current I_0, let us for a moment assume to use instead a simple current mirror: considering the Early effect of bipolar transistors, the ratio m between the output and input current of the current mirror would be given by

$$m = \left(1 + \frac{V_{DD} - V_{GS1}}{V_A}\right) \Big/ \left(1 + \frac{V_\gamma}{V_A}\right), \tag{2}$$

where V_A is the Early voltage of bipolar transistors and V_{GS1} is the gate-source voltage of M_1. In such a condition the current would have the expression shown below,

$$I_0 = \frac{2}{R^2}\left(\sqrt{\frac{m}{k_1}} - \frac{1}{\sqrt{k_2}}\right)^2. \tag{3}$$

When the supply voltage varies between its minimum and maximum values, the ratio m would vary between m_{MAX} and m_{MIN}, causing a variation of the current I_0. As a consequence, the relative variation of the current due to the Early effect would be given by

$$\frac{\Delta I_0}{I_0} = \frac{\left(\sqrt{m_{MAX}} - \sqrt{k_1/k_2}\right)^2 - \left(\sqrt{m_{MIN}} - \sqrt{k_1/k_2}\right)^2}{\left(1 - \sqrt{k_1/k_2}\right)^2}. \tag{4}$$

As the supply voltage has large variations, we would have a large relative variation of the reference current leading to an unacceptable PSRR of the series voltage regulator. As a consequence we have to use a cascode current mirror even if it leads to a reduction of the dynamic range. Since the voltage reference generator has to consume only a negligible fraction of the total power dissipated by the transponder, the current I_0 has to be set in the order of few nA. From (1) it would seem that by choosing similar values for k_1 and k_2 one could obtain a very small current also with a small resistance R. However, as we will show, because of the channel length modulation, in order to ensure a small dependence of the current on V_{DDhigh}, the ratio k_1/k_2 can not be too close to unity. In order to take into account the channel length modulation we can use for the drain current of a MOS transistor in saturation region the expression shown below,

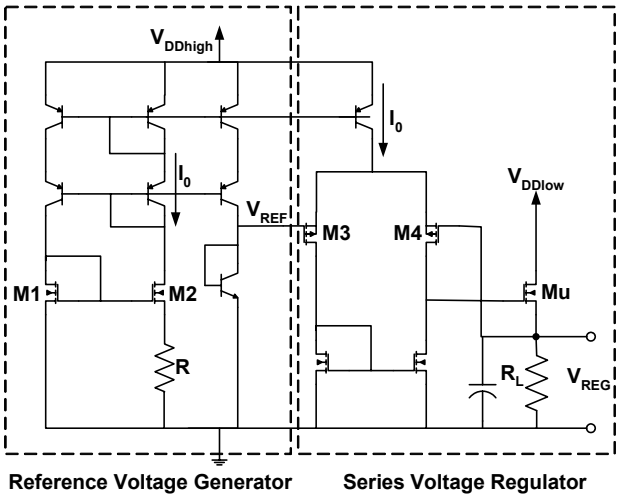

Figure 2: Circuit of the voltage regulator.

$$I_D = \frac{k}{2}\left(V_{GS} - V_{th}\right)^2\left(1 + \lambda V_{DS}\right), \tag{5}$$

where λ is the channel length modulation coefficient approximately inversely proportional to the channel length. Using such expression for the drain current of M_1 and M_2 and assuming small values of λ so that $\lambda V_{DS} << 1$, the relative variation of the current I_0, when V_{DDhigh} varies between its minimum and maximum value can be well approximated by,

$$\frac{\Delta I_0}{I_0} = \lambda \frac{V_{DDhighMAX} - V_{DDhighMIN}}{\sqrt{k_2/k_1} - 1}. \tag{6}$$

From (6) it is possible to note that, in order to have a small dependence of the current I_0 on the supply voltage, the ratio k_1/k_2 can not be too close to one and the channel length has to be chosen sufficiently large so that λ is small enough. Then, on the one hand a small k_1/k_2 would be required to obtain a small relative variation of the generated current when the supply voltage varies; on the other hand, the ratio k_1/k_2 can not be too small otherwise a too large resistance R should be used. A good tradeoff was found by setting k_1/k_2=0.5 and R= 2 MΩ. Such a resistance was implemented in high resistive poly so that its area occupation is not too large compared to the area occupation of the entire transponder. Such a choice ensures, at

the same time, a very good DC PSRR for the voltage regulator and an acceptable area occupation.

Since the reference voltage generator has two stable states, corresponding to the current given by (1) and to zero current, a start-up circuit is used to ensure that the former is reached. Such a circuit compares the current I_0 with a much smaller known current. If I_0 is zero, it provides a start-up current to switch state.

3. Series Voltage Regulator

The series voltage regulator consists of a differential amplifier that compares the output voltage with the reference voltage and produces an error signal that drives the gate of an NMOS transistor, in order to keep the output voltage constant and equal to the reference voltage [4, 5]. A PMOS differential amplifier is used with an active NMOS load. In order to ensure that the differential amplifier operation is as independent as possible of supply voltage variations, it is biased with the current I_0, previously generated, since the differential amplifier is not able to attenuate the variation of the bias current caused by the variations of the supply voltage V_{DDhigh}. Indeed, the effect of the variation of the bias current on the output regulated voltage is, at DC,

$$\left.\frac{\Delta V_{REG}}{\Delta I_0}\right|_{DC} \cong \frac{\dfrac{r_{dn}\|r_{dp}}{2}\dfrac{g_{mU}R_L}{1+g_{mU}R_L}}{1+\dfrac{r_{dn}\|r_{dp}}{2}g_m\dfrac{g_{mU}R_L}{1+g_{mU}R_L}} \cong \frac{1}{g_m}, \qquad (7)$$

where r_{dn} e r_{dp} are the drain-source resistances of the NMOS and PMOS transistors of the differential amplifier, g_m and g_{mU} are the transconductances of the source-coupled transistors, M_3 and M_4, and of the pass transistor, M_U, respectively, and R_L is the load resistance. Since the bias current is very small, in order to ensure very small power consumption, the transconductance of the source-coupled transistors is small causing a strong dependence of the regulated voltage on the bias current. As a consequence, in order to obtain a good PSRR, it is necessary to bias the differential amplifier with a current almost independent of the supply voltage. As already said such a current is obtained by mirroring the reference current previously generated. Furthermore, the differential amplifier is dimensioned so that most of the supply voltage, V_{DDhigh}, and then most of its variation drops on the NMOS active load; then, when varying the supply voltage, the variations of the collector-emitter voltage of the pnp transistor are very small leading to a very small effect of the Early voltage of the pnp transistor on the current mirror ratio. Such a choice ensures that the bias current of the differential amplifier is almost independent of the supply voltage even if a simple current mirror is used to have a larger dynamic range. Furthermore, the channel lengths of the two source-coupled transistors, M_3 and M_4, are set to be large enough (10 μm) to reduce the channel length modulation effect and then make the differential amplifier almost independent of the supply voltage. In such a way a DC PSRR with respect to the supply voltage V_{DDhigh} of about -58 dB is obtained. The DC PSRR with respect to the supply voltage V_{DDlow}, instead, is given by

$$\left.\frac{\Delta V_{REG}}{\Delta V_{DDlow}}\right|_{DC} \cong \frac{\dfrac{R_L / r_{dU}}{1+g_{mU}R_L+R_L/r_{dU}}}{1+\dfrac{r_{dn}\|r_{dp}}{2}g_m} \cong \frac{2}{g_m r_{dn}\|r_{dp}}\frac{1}{g_{mU}r_{dU}} \qquad (8)$$

To maximize the expression in (8) the output transistor M_U has to have a quite large channel width (50 μm) in order to obtain a high value of its gain $g_{mU}r_{dU}$ and the differential amplifier has to have a high gain, which implies that the channel lengths of the NMOS transistors of the active load have to be quite large (80 μm). In such a way we can avoid the use of a second amplification stage that would lead to an increase in the power consumption. It is also important to ensure a high PSRR at the operation frequency of the reader-transponder system (2.45 GHz or 868/916 MHz), in order to drastically attenuate the effect of the ripple superimposed to V_{DDlow} and V_{DDhigh}. In order to reach such objective, a capacitance is put at the output of the series voltage regulator.

The minimum and maximum V_{DDlow} required for the correct operation of the series voltage regulator are imposed by the output NMOS transistor, M_U, and are

$$V_{DDlowMIN} = V_{OUT} + V_{DSsat} \cong 0.63V,$$
$$V_{DDlowMAX} = V_{OUT} + V_{DSMax} \cong 5.6V.$$

The minimum and maximum V_{DDhigh} required for the correct operation of the series voltage regulator are imposed by the reference voltage generator and are

$$V_{DDhighMIN} = 2V_{\gamma} + V_{DSsat} \cong 1.4V,$$
$$V_{DDhighMAX} = V_{\gamma} + V_{GS} + V_{CEMax} \cong 6.3V.$$

As a consequence, the 2-stage voltage multiplier has to be able to provide a V_{DDhigh} larger than 1.4 V when the output voltage of the single stage voltage multiplier is 0.63 V.

Since the digital section is implemented in subthreshold CMOS logic, the static and dynamic current in the logic gates is exponentially increasing with temperature, and so would be the power consumption if the supply voltage was regulated with respect to temperature variations. For this reason we decided not to regulate in temperature the voltage regulator, accepting the negative temperature coefficient of -2mV/°C given by the p-n junction that generates the reference voltage.
In such a way we have a significant advantage: the temperature coefficient of the supply voltage almost exactly compensates the temperature dependence of the subthreshold current, ensuring that the current in the logic gates, and therefore the performance and the power consumption of the subthreshold logic, are practically independent of temperature.

4. Experimental Results

The proposed voltage regulator was successfully implemented in AMS 0.35 μm BiCMOS. The die photograph is shown

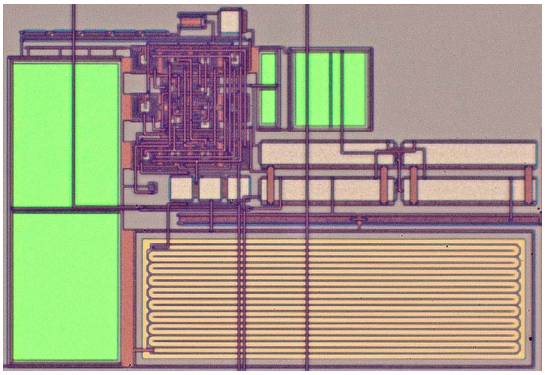

Figure 3: Die Photograph (core).

Fig. 3. The measurements show that the mean output regulated voltage is 605 mV with a line sensitivity of ±0.8 mV/V with respect to V_{DDhigh} and of ±0.18 mV/V with respect to V_{DDlow}. The output regulated voltage as function of V_{DDlow} and V_{DDhigh} is shown in Fig. 4a. Furthermore, the output voltage varies from 605.5 mV to 605 mV when the output current varies from 0 to 5 µA, leading to an equivalent DC output resistance of about 100 Ω (a few thousand times smaller than the equivalent load resistance). The output regulated voltage as a function of the output current is shown in Fig. 4b. The measurements also show a very good PSRR for both the V_{DDlow} and V_{DDhigh}: Fig. 5 (right) shows, with respect to V_{DDhigh}, a DC PSRR of -58.5 dB and a PSRR at the RF operating frequency of -54 dB. Fig. 5 (left), instead, shows, with respect to V_{DDlow}, a PSRR in DC of -78 dB and a PSRR at the RF operating frequency of -57 dB. The quiescent current is about 34 nA. Such a current is provided by V_{DDhigh} for the operation of the error amplifier and to generate the reference voltage. As a consequence, the quiescent power consumption, for the minimum supply voltage V_{DDhigh} that allows the correct operation of the series voltage regulator is about 48 nW. Furthermore, when applying a load current pulse from 0 to 5 µA, a settling time of 480 µs and a maximum variation of the output regulated voltage of 45 mV are obtained. The occupation of area on the chip is of 0.025 mm^2.

5. Conclusion

We have presented a series voltage regulator designed with specific features to be used as a power supply of UHF and Microwave passive RFID transponders. Experiment confirms that it provides a very low regulated voltage, extremely low quiescent power consumption, and a very good PSRR at DC and RF. The regulator is designed for the power supply of circuits operating in subthreshold or weak inversion regions, and for this reason is not temperature compensated, therefore providing a temperature coefficient of −2 mV/°C, that allows suppression of the temperature dependence of the operation of subthreshold and weak inversion circuits.

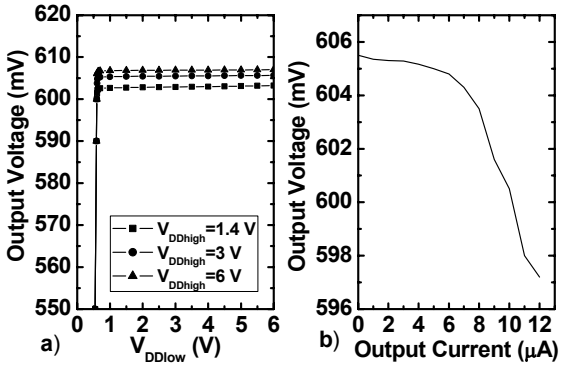

Figure 4: a) Output voltage vs. V_{ddlow} for 3 values of V_{ddigh} for an output current of 2 µA, b) Output voltage vs. Output current for V_{ddlow}=1 V and V_{ddhigh}=3 V.

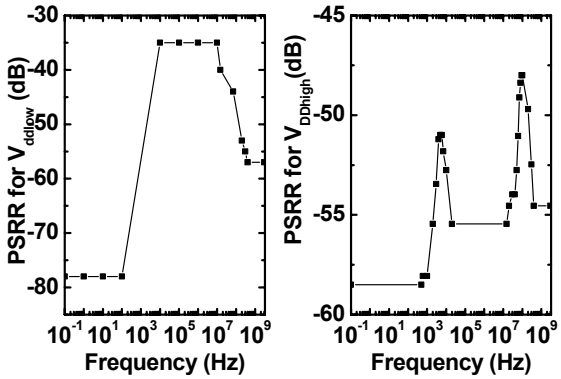

Figure 5: PSRR of the series voltage regulator.

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