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***Abstract*—We present the design of the RF section of a long range passive RFID transponder, consisting of a voltage multiplier and a voltage regulator, that convert the RF signal into a regulated DC supply voltage, a PWM demodulator and a PSK backscatter modulator. The entire circuit has been designed with AMS 0.35 μm BiCMOS technology. Post-layout simulations show the correct operation of the whole section. The supply voltage generator, which provides a supply voltage of 0.6 V – appropriately regulated for the subthreshold CMOS logic to be used for the digital section - exhibits a power efficiency of 20% in the RF/DC conversion. Proper modulation and demodulation is obtained.**

I. INTRODUCTION

Dense networks of low-power, low-cost, and low-data-rate wireless sensors (or "smart tags") are envisaged in recent scenarios of Ambient Intelligence [1]. For such networks to be practically deployed, present available choices are not completely satisfactory. Indeed, on the one hand we have wireless networks based on the Bluetooth standard characterized by link datarates up to 780 kbps, nodes with reasonable computational capabilities, but also by a transceiver power consumption not lower than 50 mW, requiring the use of (to-be-frequently-recharged) batteries [2]. On the other hand, we have microwave RFID systems based on passive transponders, that extract power for operation (few Ws) by rectifying the RF signal transmitted by the reader, but have only a very simple finite state machine on board, adequate only to perform basic memory read and write operations. The reader is also the master of the minimum-size RFID network, has an on-board microprocessor, and is charged by batteries, since a power dissipation of the order of few hundreds mW is required for supplying power to the transponders situated in a range of few meters. In order to achieve an operating range of several meters, desired for many applications, it is necessary to reduce the power consumption of both the analog and digital sections of the tag to the sub-μW regime and to increase the power efficiency of the voltage multiplier at least over 20% [3]. The digital section of the transponder consists of a simple general purpose processor with a clock frequency of 1 MHz, implemented in subthreshold CMOS logic with a supply voltage of 0.6 V, which allows us to maintain the power consumption below 1 μW, required for achieving an operating range of several meters. In this paper we describe the implementation of the entire RF section of a passive transponder that works in both the 2.45 GHz and 916 MHz ISM bands realized with AMS 0.35 μm BiCMOS IC technology.

II. ARCHITECTURE OF THE RF SECTION

The architecture of the RF section is schematically illustrated in Fig. 1. It consists of:

- a voltage multiplier, which converts the antenna RF voltage at the operating frequency into two DC voltages of at least 0.63 V and 1.35 V (in the case of minimum available power at the antenna);
- a series voltage regulator that generates a constant DC voltage independent of the power at the antenna and of the power consumption of the transponder. Such regulator must have a power consumption of few tens of nW and its temperature coefficient is on purpose that of a normal pn junction (-2mV/°C), in order to ensure that the performance and the dissipation of the subthreshold digital section is practically *independent* of temperature;
- an ASK demodulation unit, which extracts from the received RF voltage the baseband signal for the digital section;
- a modulation unit that allows transponder transmission through PSK modulation of the backscattered radiation with the baseband signal provided by the digital section.

A. Voltage Multiplier

The voltage multiplier used in our implementation is shown in Fig. 1. It consists of a single stage voltage multiplier, which provides the power to the digital section of

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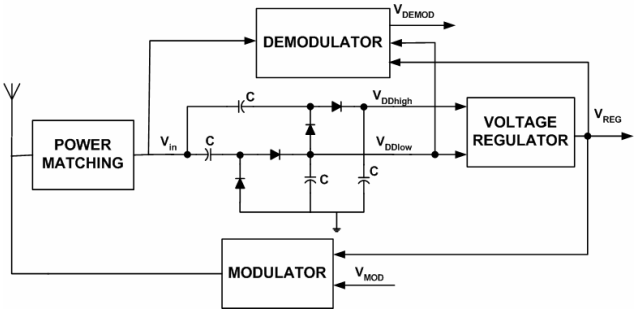

Figure 1. Architecture of the RF Section.

the transponder and for the modulator, and a two-stage voltage multiplier that provides the power to the voltage regulator. Such a choice was made to optimize the power efficiency of the AC-DC conversion, as we will explain later on. The capacitances of the voltage multiplier are chosen so that their time constant is much larger than the interval during which the PWM signal goes low (2 μs), ensuring low ripple also when the transponder is receiving. Let us assume that a sinusoidal voltage, V_{in}, with a frequency f_0 and an amplitude V_0, is applied to the input of an N-stage voltage multiplier. In such condition and for negligible substrate losses, the power efficiency of the voltage multiplier is given by [3],

$$\eta = \frac{V_U I_L}{2NI_S V_0 B_1\left(\frac{V_0}{V_T}\right)\exp\left(-\frac{V_U}{2NV_T}\right)} \tag{1}$$

where V_U is the output voltage, I_S is the diode saturation current, I_L is the output current, and $B_1(x)$ is the first order modified Bessel function. From (1), power efficiency is maximum for $N=1$, therefore we use a one stage voltage multiplier to generate the DC voltage, V_{DDlow}, that goes to the input of the series voltage regulator and that has to provide almost all the 1 μW required for transponder operation. The regulator requires V_{DDlow} to be at least 30 mV larger than the 0.6 V required to supply of the digital section. But such voltage would be too small to generate the reference voltage and to ensure the correct operation of the error amplifier in the series voltage regulator. For those purposes, that require a very small power, we use the voltage V_{DDhigh} provided by the 2-stage voltage multiplier. In such way a power efficiency of 25% in the RF/DC conversion is reached. The input impedance of the voltage multiplier consists of the equivalent resistance of the voltage multiplier (in terms of dissipated power), in parallel to the sum of all diode capacitances. The voltage multiplier will be matched to the antenna using an inductance, in order to compensate the input capacitance, and a LC matching network. The power matching will be tuned to the condition of minimum power at the antenna that still enables proper operation of the voltage regulator. When the power at the antenna increases, the RF section is mismatched, but the voltage regulator continues to work correctly as verified in [3]. Moreover, since the average capacitance of the diodes varies with the amplitude of the voltage at the input of the voltage multiplier, in order to ensure a good power matching the variations of the input capacitance with respect to its mean value have to be much smaller than the input resistance; such condition imposes an upper limit to the area of the diodes [3]. Since we use only one stage to obtain a so small output power, the quality factor of the power matching network is quite high, about 45. Such a high Q requires us to consider the breakdown voltage of the diodes, which is larger than 9 V for the diodes we used. By simulation, we find that, for an input voltage amplitude V_0 of 6.5 V, which ensures the safe operation of the diodes, the input power, P_{IN}, of the voltage multiplier should be 32.3 mW. The power, P_{ANT}, at the antenna, required to obtain such voltage and power at the input of the voltage multiplier, is given by,

$$P_{ANT} \cong \left(\frac{P_{IN} Q\sqrt{R_A}}{V_0} + \frac{V_0}{2Q\sqrt{R_A}}\right)^2 \tag{2}$$

where R_A is the antenna resistance. Assuming to use a dipole antenna (R_A=72 ohm) P_{ANT} is about 3.63 W, which is much larger than the 500 mW maximum EIRP enforced by European regulations[4]. In such conditions, breakdown of the diodes is not an issue.

III. VOLTAGE REGULATOR

The voltage regulator consists of a series voltage regulator and a reference voltage generator. Such voltage regulator has to consume a negligible fraction of the whole power dissipated by the transponder and must have a PSRR larger than -50 dB on a large input dynamics. The regulator was implemented in BiCMOS IC technology, in order to extend the input dynamics of the voltage regulator by the use of pnp transistors instead of PMOS transistors, which have a too high threshold voltage in our technology.

A. Reference Voltage Generator

The circuit used to generate the reference voltage is shown in Fig. 2. It consists of a circuit that generates a current, I_0, almost independent of the supply voltage; then such current is injected into a diode, to generate the reference voltage [5]. In the current generator, in order to ensure that the currents in the two branches are as close as possible in order to reduce the Early effect, a Cascode mirror is used. Assuming identical currents in the two branches, the current I_0 in Fig. 2 has the expression shown below,

$$I_0 = \frac{2}{R^2}\left(\frac{1}{\sqrt{k_1}} - \frac{1}{\sqrt{k_2}}\right)^2, \tag{3}$$

where $k_i = \mu_n C_{ox} W_i / L_i \quad (i = 1,2)$. Since the voltage reference generator has to consume only a negligible fraction of the total power dissipated by the transponder, such current has to be set of the order of 10 nA. It would seem that by choosing similar values for k_1 and k_2 one could obtain a very

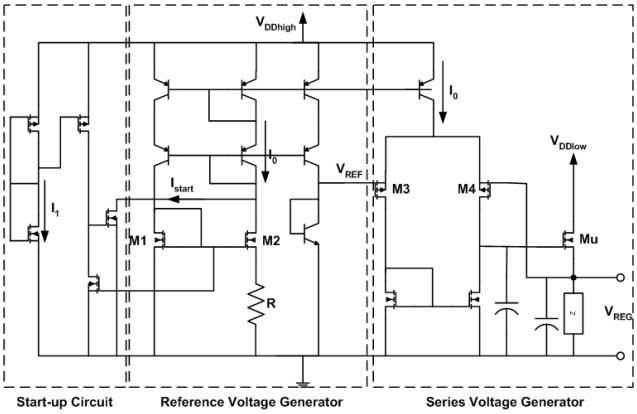

Figure 2. Circuit of the Voltage Regulator

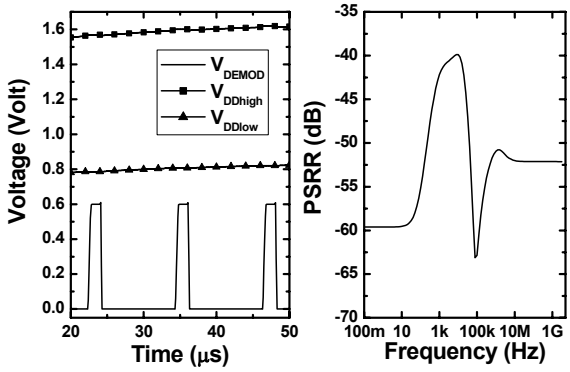

Figure 3. Left: Output signal of the demodulator and the voltage multiplier with a PWM signal at the antenna. Right: PSRR of the voltage regulator.

small current also with a small resistance. As we will demonstrate, because of the channel length modulation, in order to ensure a small dependence of the current on V_{DDhigh}, the ratio k_1/k_2 can not be too close to 1. In order to take into account the channel length modulation we can use for the drain current of a MOS in saturation region the expression shown below,

$$I_D = \frac{k}{2}\left(V_{GS} - V_{th}\right)^2\left(1+\lambda V_{DS}\right), \quad (4)$$

where the parameter λ is inversely proportional to the channel length. Using such expression, the relative variation of the current, I_0, when the V_{DDhigh} varies between the minimum and maximum value is given by,

$$\frac{\Delta I_0}{I_0} = \frac{k_1/k_2}{(1-\sqrt{k_1/k_2})^2}\left(\frac{1}{\sqrt{1+\lambda V_{DS2MIN}}} - \frac{1}{\sqrt{1+\lambda V_{DS2MAX}}}\right)^2 k_1 \quad (5)$$

Since $V_{DS2} \approx V_{DDhigh} - 2V_\gamma$, in order to have a small dependence of the current on the supply voltage, the ratio k_1/k_2 can not be too close to 1 and the channel length has to be chosen sufficiently large so that λ is small enough. On the other hand, the ratio k_1/k_2 can not be too small, otherwise, in order to obtain a current of few nA, a too large resistance should be used. A good compromise was found setting k_1/k_2=0.5, with a resistance $R = 2$ MΩ. It was implemented in high resistive poly so that its area occupation is not too large with respect to the rest of the circuit. Such a choice ensures, at the same time, a very good DC PSRR for the voltage regulator and an acceptable area occupation. Since the reference voltage generator has two stable states, corresponding to the current given by (3) and to zero current, a start-up circuit is used to ensure that the former stable state is achieved. Such a circuit compares the current I_0 with a much smaller known current. If I_0 is zero, it provides a start-up current to change the stable state.

B. Series Voltage Regulator

The series voltage regulator consists of a differential amplifier that compares the output voltage with the reference voltage and produces an error signal that drives the gate of an NMOS transistor, in order to keep the output voltage constant and equal to the reference voltage. A PMOS differential amplifier is used with an active NMOS load. In order to ensure that the differential amplifier operation is as independent as possible of supply voltage variations, it is biased with the current I_0, previously generated, and the channel length of the two source-coupled transistors, M3 and M4, is chosen large enough (10 μm) to reduce the channel length modulation effect. In such a way the operation of the differential amplifier is almost independent of the supply voltage ensuring a DC PSRR of about -60 dB. It is also important to ensure a high PSRR at the operation frequency of the reader-transponder system (2.45 GHz or 916 MHz), in order to drastically attenuate the effect of the ripple superimposed to V_{DDlow} and V_{DDhigh}, and at a frequency of about 1 MHz, in order to attenuate the variation of V_{DDlow} and V_{DDhigh} due to the PWM signal when the transponder is receiving. In order to reach the first objective, a capacitance is put at the output of the series voltage regulator while to reach the second objective a capacitance is put at the output of the differential amplifier. The PSRR, obtained by post-layout simulation, is shown in Fig. 3 (right). The minimum and maximum V_{DDhigh} required for the correct operation of the series voltage regulator are imposed by the reference voltage generator and are $V_{DDhighMIN} = 2V_\gamma + V_{DSsat} \cong 1.4V$ and $V_{DDhighMAX} = V_\gamma + V_{GS} + V_{CEMax} \cong 6.3V$. As consequence, the 2-stage voltage multiplier has to be able to provide a V_{DDhigh} larger than 1.4 V when the output voltage of the single stage voltage multiplier is 0.6 V. Furthermore, in order to ensure that V_{DDhigh} is always smaller than 6.3 V, a series of five diodes is connected in parallel with the output of the 2-stage voltage multiplier. A resistance is added in series with the output, in order to limit the current in the diodes and to ensure that the time constant of the capacitances remains sufficiently high also when diodes conduct. The minimum and maximum V_{DDlow} required for the correct operation of the

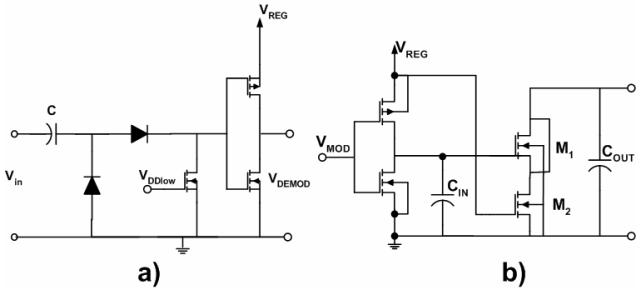

Figure 4. a) Demodulator; b) Modulator.

series voltage regulator are imposed by the output NMOS transistor, M_u, and are $V_{DDlowMIN} = V_{OUT} + V_{DSsat} \cong 0.65V$, $V_{DDlowMAX} = V_{OUT} + V_{DSMax} \cong 5.6V$. Also in this case, in order to ensure that the output voltage of the single-stage voltage multiplier always is smaller than 5.6 V, a series of four diodes and a resistor is connected in parallel with the output of the single-stage voltage multiplier. The total power consumption of the entire voltage regulator is about 60 nW in the case of minimum power at the input of the voltage multiplier. The regulated voltage generated by such a circuit has a temperature coefficient of -2 mV/°C. Indeed, since the digital section is implemented in subthreshold CMOS logic, the current, provided by MOS transistors, is exponentially dependent on temperature. The temperature coefficient of the supply voltage almost exactly compensates the current dependence, ensuring a constant performance and power consumption with varying temperature.

IV. Demodulator

The demodulator is a voltage multiplier that has to follow the variations of the PWM signal (typically 40 Kbps). The output signal of the demodulator goes to an inverter to restore the logic levels. The capacitance and resistance in parallel with the output of the demodulator are obtained exploiting the input capacitance of the inverter and the drain-source resistance of an NMOS transistor, respectively. The gate of the NMOS transistor is driven by the output voltage of the single stage voltage multiplier in order to obtain a variable resistance. Indeed, when the power at the input of the RF section increases the voltage at the output of the demodulator would increase and the time constant would be to slow to follow the signal variation. But at the same time, also the gate voltage of the NMOS transistor increase and then the time constant becomes smaller ensuring the correct operation of the demodulator. Figure 3 (left) shows, for a PWM input signal, the output of the demodulator and the negligible effect of the variations of the PWM signal on the output of the voltage multiplier. The power consumption of the demodulator, in the condition of minimum power at the input of the RF section, is about 250 nW. The demodulator is shown in Fig. 4a.

V. Modulator

Since the transponder exploits a PSK backscatter modulation to transmit data to the reader, the imaginary part of the impedance seen by the antenna has to vary symmetrically with respect to zero, so that only the phase of the backscattered signal is varied. Most of the PSK backscatter modulators vary the output capacitance according to the data signal. Our modulator is shown in Fig. 4b. In such modulator we exploit the variation of the capacitance of the transistor M1 in the saturation and cut-off regions. Once the modulation depth is chosen in order to maximize the operating range [3], the dimensions of M1 are fixed. M2 allows us to fix the output resistance, which must be much larger than the antenna resistance so that it is negligible in the parallel with the resistance seen from the power matching network. Since M2 has minimum size, the output resistance is of the order of few kΩ. An external inductance is put in parallel with the output of the modulator so that the imaginary part of the impedance seen by the antenna varies symmetrically with respect to zero. For a variation of the output capacitance of about 350 fF, as required to maximize the operating range [3], M1 has a channel width and length of 670 µm and 0.35µm, respectively. In order to limit the channel bandwidth occupation to 250 KHz, the bandwidth of the input signal of the modulator is reduced with a capacitor C_{IN} of 650 fF. The modulator, when transmitting, consumes a power of 15 nW.

VI. Conclusions

We have presented the implementation of the entire RF section of a passive RFID transponder with the AMS 0.35 µm BiCMOS IC technology. Post-layout simulations show that a voltage supply of 0.6 V is generated with a PSRR larger than -50 dB, at the critical frequencies, and with an AC/DC power efficiency larger than 20%. The correct operation of the PSK backscatter modulator and of the PWM demodulator has been verified. The entire section has an area occupation smaller than 0.1 mm^2.

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