Performance of carbon nanotube field effect transistors with doped source and drain extensions and arbitrary geometry

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Performance of Carbon Nanotube Field Effect Transistors with doped source and drain extensions and arbitrary geometry

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Abstract

In this work, we investigate the expected device performance and the scaling perspectives of Carbon NanoTube Field Effect Transistors (CNT-FETs), with doped source and drain extensions, by means of a novel three-dimensional NEGF-based simulation tool capable of considering arbitrary gate geometry and device architecture.

In particular, we have investigated short channel effects for different gate configurations and geometry parameters. Double gate devices offer quasi ideal subthreshold slope and DIBL also with not extremely thin gate dielectrics. In addition, we show that devices with parallel CNTs can provide On currents per unit width significantly larger than their silicon counterpart, and that high-frequency performance is very promising.

Introduction

Carbon NanoTube Field Effect Transistors (CNT-FETs) are actively investigated by the research community as promising devices for integrated circuit technology at the end or beyond the ITRS roadmap (1). They promise intrinsic performance comparable to silicon based MOSFET technology (2) and better scaling perspectives. Most of the literature deals with Schottky Barrier CNT-FETs, in which the current in the channel is mainly determined by the field-induced modulation of the potential at the CNT ends. Such a working principle, however, strongly limits device performance, because of the ambipolar behavior and of the poor control of the channel through the gate, which limits the attainable transconductance.

To alleviate these problems different solutions have been proposed for obtaining ohmic contacts either by tuning the source and drain workfunctions (3), or by doping the CNT at the source and drain ends (4).

In this work, we focus on CNT-FETs with doped source and drain and evaluate their performance against the requirements at the end of the ITRS. We have developed a code for the simulation of CNT-FETs with arbitrary and realistic three dimensional geometry, in the limit of ballistic transport. The novelty of our approach consists in the possibility to fully take into account details of the geometry, without oversimplifications, such as the coaxial symmetry (5). Our code solves self-consistently the 3D Poisson, and the Schrödinger equations by means of the NEGF formalism, using a tight-binding Hamiltonian with an atomistic (p_z orbital) real space basis (6).

Results and Discussions

First, we consider a (11,0) CNT embedded in SiO_2, with a diameter d of 0.9 nm, an undoped channel of varying length L and n-doped CNT extensions of 10 nm at the source and drain ends (Fig. 1).

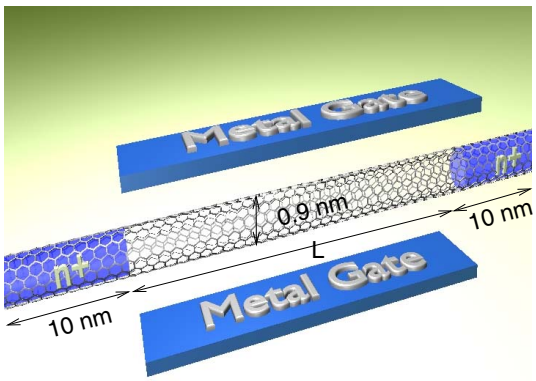

FIG. 1: Three-dimensional structure of the simulated CNT-FETs.

The CNT extensions have a stoichiometric ratio f of fully ionized donors.

As a first attempt for studying CNT-FET performance, we have considered the impact of the molar fraction f on the current in the off-state regime. Fig. 2 shows the current for $V_{DS} = 0.5\ V$ and $V_{GS} = 0\ V$ as a function of f, for a double gate (DG) CNT-FET with L=7 nm and t_{ox}=2 nm. As can be seen, for the considered device the current is extremely sensitive to f, and a small variation in the number of ionized atoms in the source and drain extensions can determine a variation of the current of almost two orders of magnitude. As a consequence, since the number of donors is of the order of tens, current dispersion due to random dopant fluctuations can be problematic.

As far as DC properties are concerned, we evaluate the devices in terms of short channel effects, I_{on} and I_{off} currents. We first consider short channel effects for different gate layouts (single, double and triple gate) for the same channel length $L = 15$ nm (Fig. 3).

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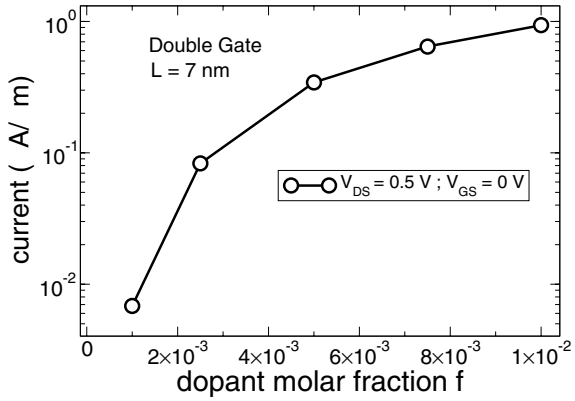

FIG. 2: Current for $V_{DS} = 0.5\ V$ and $V_{GS} = 0\ V$ as a function of the molar fraction of doping atoms f for a Double Gate CNT-FET with L=7 nm.

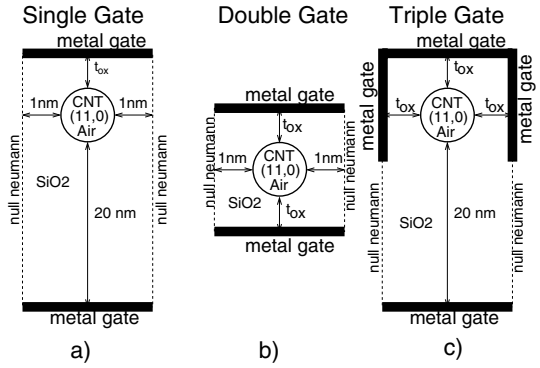

FIG. 3: Transversal cross section of the CNT-FETs with different gate structures : a) single gate; b) double gate; c) triple gate. Null Neumann boundary condition are imposed on lateral ungated surfaces.

The sub-threshold swing S and Drain Induced Barrier Lowering (DIBL) as a function of the oxide thickness are plotted in Figs. 4a and 4b. Null Neumann boundary conditions are imposed on the lateral faces of the transversal cross sections, in order to consider an array of CNTs. As expected, the more gates surround the channel, the better is channel control. Triple gate devices show an ideal behavior even for the thickest oxide we have considered (5 nm), while quasi-ideal S, is obtained for the double gate structure in the whole range of performed thicknesses of SiO_2 dielectrics. A single gate instead gives acceptable S and DIBL for oxides thinner than 3 nm.

From here on, we will focus our attention on a double gate structure, with t_{ox}=2 nm and the cross section shown in Fig 3b. Fig. 5a shows the on-current I_{on} per unit width defined as the current obtained for $V_{GS} = V_{DS} = 0.8\ V$, as a function of channel length, assuming a lateral dielectric separating adjacent nanotubes

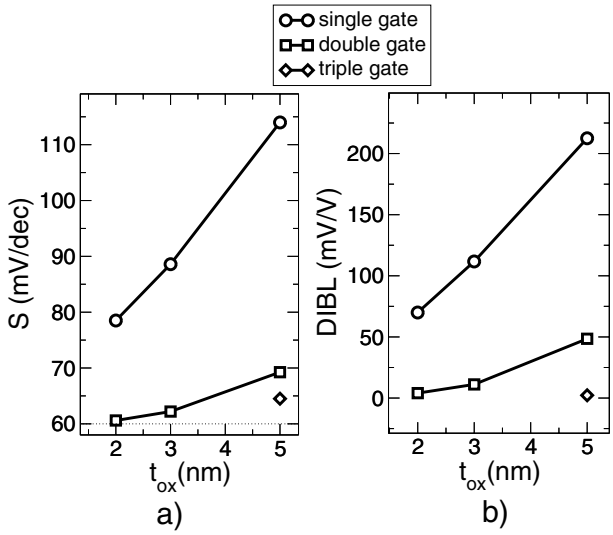

FIG. 4: a) Subthreshold slope and b) Drain Induced Barrier Lowering as a function of the oxide thickness, for L=15 nm and for different gate layouts. $f = 10^{-3}$.

of 2 nm. In Fig. 5b, the On current per nanotube is plotted as a function of the nanotube diameter.

As the channel length is decreased, short channel effects become more important, and at the same biasing conditions, shorter devices show larger I_{on} currents, since lowering of the channel barrier occurs. Moreover, as far as the CNT diameter is increased, quantized states along each atom ring are closer in energy so that more subbands participate to electron transport, increasing channel conductance.

In Fig. 6 we show the On current as a function of the normalized tube density per unit length $\rho = \frac{d}{T}$, where T is the distance between the center of two nanotubes, as shown in the inset of Fig. 6. All the results show that CNT-FETs can drive significant currents. As compared to the ITRS requirements, in the case of the most densely packed array, the current per unit length is almost 7 times larger than that expected for high performance devices at the 32 nm technology node (hp32 : effective gate length equal to 13 nm), and 6 times for the 22 nm technology node (hp22 : effective gate length equal to 9 nm).

The off-current (I_{off}), defined as the current obtained for $V_{GS} = 0\ V$ and $V_{DS} = 0.8\ V$, is instead 15 times larger than that required both for the hp32 and hp22 nodes (Fig. 7).

As observed also in (7), this is due to the presence of bound states in the valence band, which, for high doping and for large drain-to-source voltages are occupied by holes tunneling from the drain reservoir (Fig. 8). For smaller V_{DS}, bound states are quite far from the drain Fermi level, so the linear behavior in the semilog plot of the transfer characteristics in the sub-threshold regime is almost recovered, as shown in Fig. 9.

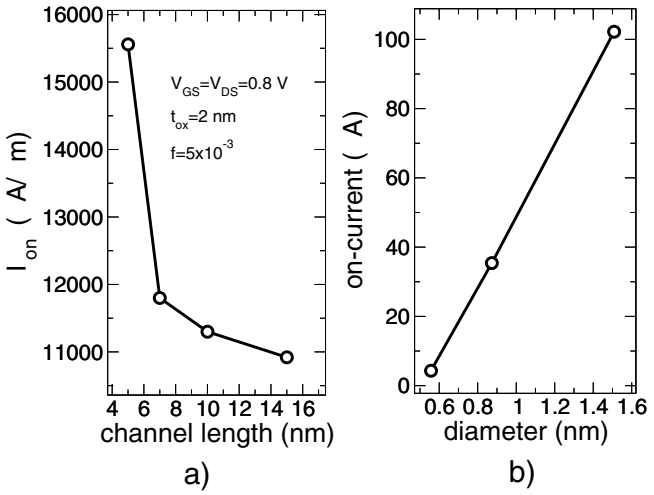

FIG. 5: a) On Current per unit width as a function of the channel length for a double gate CNT-FET (2 nm lateral dielectric between adjacent nanotubes); b) I_{on} current per nanotube as a function of the nanotube diameter, for a L=7 nm double gate CNT-FET. $t_{ox} = 2$ nm, $f = 5 \times 10^{-3}$.

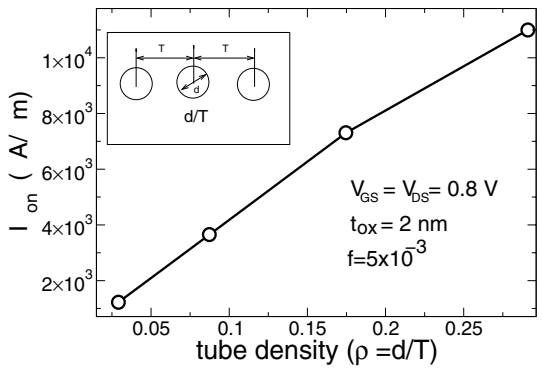

FIG. 6: On current as a function of the nanotube normalized density per unit length $\rho = \frac{d}{T}$ for a L=15 nm double gate CNT-FET.

Fig. 10 shows the transconductance g_m as a function of the gate voltage for the L=10 nm device and $V_{DS} = 0.8$ V. The transconductance peak is in correspondence of the gate voltage at which the first one-dimensional subband crosses the source Fermi level.

We now focus our attention on switching and high-frequency performance of CNTs. The typical figure of merit for digital applications is the intrinsic device speed, defined as $\tau = \frac{C_G V_{DD}}{I_{on}}$, where V_{DD} is the supplied voltage and C_G is the differential gate capacitance for $V_{GS} =$ 0.8 V (Fig. 11a). This quantity is a typically used estimate of the time it takes a NOT port to switch from the ON(OFF) state to the OFF(ON) state, when its output drives another NOT port, represented as a load capacitance C_G. Compared to the ITRS requirements, the

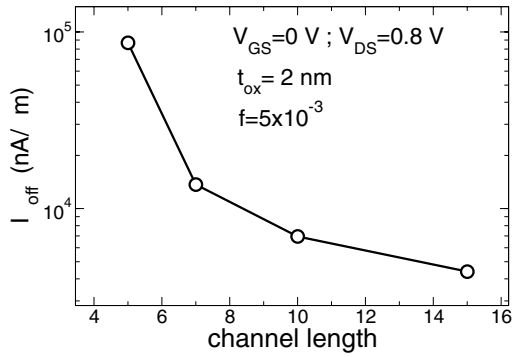

FIG. 7: Off-current as a function of the channel length for a double gate CNT-FET.

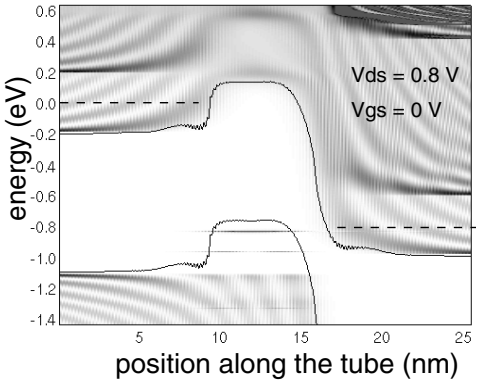

FIG. 8: Density of states computed for the L=7 nm device, for $V_{GS} = 0$ V and $V_{DS} = 0.8$ V as a function of the energy and the coordinate along the nanotube axis. Dashed lines are in correspondence of the source and drain Fermi level.

obtained τs are at least 12 times faster.

CNT-FETs have also good potential to be applied for THz applications (8). In Fig. 11b, the cut-off frequency defined as $f_T = \frac{g_m}{2\pi C_G}$ is shown as a function of the channel length : f_T is of the order of tens of THz, and the values obtained by simulations are larger than that found in (8), since the gate capacitance is overestimated in (8).

As a word of caution, we must consider that additional stray capacitances could reduce the estimated f_T and τ.

Conclusion

We have developed a novel 3D NEGF-based simulation tool for arbitrary CNT-FET architectures, which has enabled us to investigate the performance perspectives of CNT-FETs from an engineering point of view.

We have shown that double-gate structures exhibit very small short channel effects even with rather thick silicon

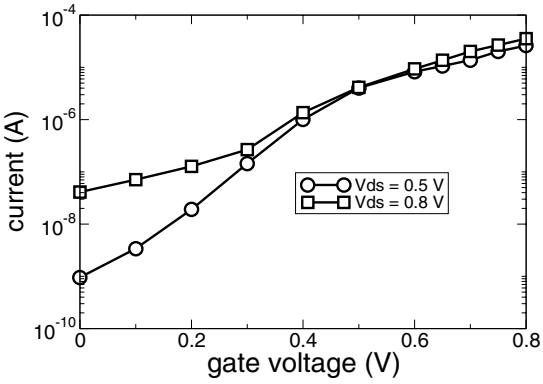

FIG. 9: Transfer characteristics for the double gate CNT-FET with L=7 nm, for $V_{DS} = 0.5\ V$ and $V_{DS} = 0.8\ V$. $t_{ox} = 2$ nm, and $f = 5 \times 10^{-3}$.

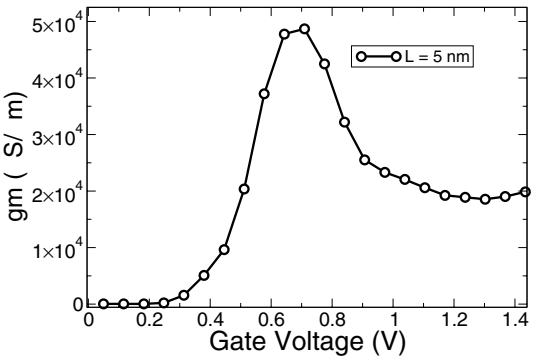

FIG. 10: Transconductance as a function of the gate voltage for the double gate CNT-FET with L=10 nm, $t_{ox} = 2$ nm, $V_{DS} = 0.8$ V, and $f = 5 \times 10^{-3}$.

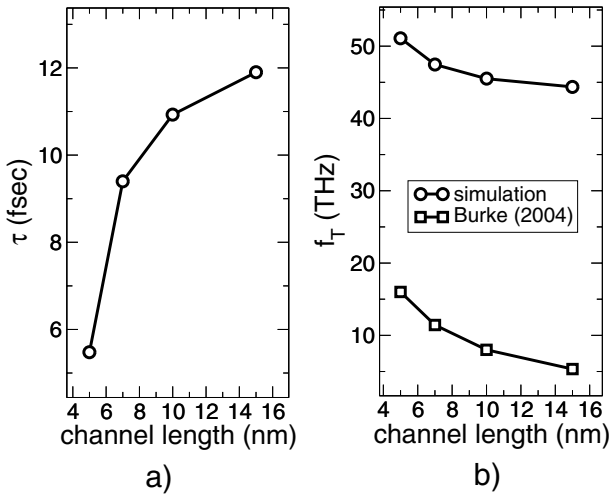

FIG. 11: a) Inverse of the intrinsic device speed, defined as $\tau = \frac{C_G V_{DD}}{I_{on}}$ as a function of the channel length for double gate CNT-FET. $V_{DD} = 0.8V$ and C_G is the gate capacitance. b) Cut-off frequency as a function of the gate length, for the double gate CNT-FET. $t_{ox} = 2$ nm,$f = 5 \times 10^{-3}$.

oxide gate dielectric (5 nm), that the driving currents and the transconductance are very good compared to the ITRS requirements, while the I_{off} may pose some problems due to the presence of localized hole states in the channel. We have also shown the double gate CNT-FETs are very promising for THz applications if stray capacitances can be maintained under control.

Acknowledgments

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