Università di Pisa

A Sub-1 V, 10 ppm/Â°C, Nanopower Voltage Reference Generator

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G. De Vita, G. Iannaccone, *A Sub-1 V, 10 ppm/Â°C, Nanopower Voltage Reference Generator* , European Solid State Circuit Conference – ESSCIRC 2006, pp. 307-310, Montreaux, Switzerland 2006

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Abstract— **An extreme low power voltage reference generator operating with a supply voltage ranging from 0.9 to 4 V has been implemented in AMS 0.35 µm CMOS process. The maximum supply current measured at the maximum supply voltage and at 80 °C is 70 nA. A temperature coefficient of 10 ppm/°C is achieved by means of a perfect suppression of the temperature dependence of the mobility, the compensation of the channel length modulation effect on the temperature coefficient and the absence of the body effect. The power supply rejection ratios without any filtering capacitor at 100 Hz and 10 MHz are lower than -53 and -42 dB, respectively. The occupied chip area is 0.045 mm^2.**

I. Introduction

Low voltage and extreme low power are essential design requirements for circuits and systems to be deployed in a pervasive electronics scenario, where battery replacement can be very costly or where other scarce energy scavenging techniques are used. This leads to a strong demand for circuit building blocks operating with low supply voltage and sub microwatt power. Among them, voltage reference generators are used in almost all analog and digital systems to generate a DC voltage independent of the supply voltage and of temperature variations and they are preferentially implemented with a standard CMOS process for compatibility with the rest of the system. A common way to generate a reference voltage is to use a bandgap voltage reference, which can be implemented in any standard CMOS technology by exploiting the parasitic vertical BJTs [1, 2]. Bandgap voltage references typically provide a voltage around 1.25 V and then require an even larger supply voltage. Such problem can be solved by resistive subdivision methods [2] that allow us to scale down the reference voltage allowing sub-1 V operation.

Other voltage references are based on the availability of transistors with two different threshold voltages in the same CMOS technology. Such feature can be obtained by using a selective channel implant [3, 4], by using different materials for the gate stack [5], by doping differently the polysilicon gates [6]. Such solutions can not be implemented in a standard CMOS technology because they require additional fabrication steps. Other types of voltage references, implemented with a standard CMOS technology, are based on a weighted difference between the gate-source voltages of two MOS transistors [7-9] but they can not usually operate in the sub-1 V regime.

In this paper we present a CMOS voltage reference, which exploits the MOS characteristics in the saturation and in the subthreshold regions, able to operate with a supply voltage smaller than 1 V and with a power consumption smaller than 100 nW.

II. Circuit Description

The proposed voltage reference generator is shown in Fig. 1. A circuit formed by transistors numbered from M_1 to M_8 generates a current I_0 as independent as possible of the supply voltage V_{DD}. Such current is then injected into the diode-connected NMOS transistor M_{10}. The temperature dependence of I_0 is compensated by the temperature dependence of the gate-source voltage of M_{10} generating a temperature compensated reference voltage V_{REF}.

The core of the current generator circuit is represented by transistors M_1-M_4, which determine the value of the current I_0, whereas transistors M_5 and M_6 impose equal current I_1 in M_1 and M_3 and transistors M_7 and M_8 impose equal current I_0 in M_2 and M_4. Transistors M_1 and M_3 (indicated in Fig. 1 with a symbol with a thicker line for the gate) are 5V-NMOS transistors with a threshold voltage of 0.7 V; all the other transistors are 3.3V-MOS transistors with a threshold voltage of 0.45 V and -0.75 V for NMOS and PMOS, respectively. The two different threshold voltages allow us to bias M_1 and M_3 in the subthreshold region and, at the same time, to bias M_2 and M_4 in the saturation region. Such behavior is achieved by setting the gate-source voltages of M_1, M_2 and M_3, M_4 to a value between 0.45 V and 0.7 V. The I-V characteristics of an NMOS transistor that operates in the saturation and in the subthreshold region can be approximated by (1) and (2), respectively:

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{th}\right)^2\left(1 + \lambda V_{DS}\right), \qquad (1)$$

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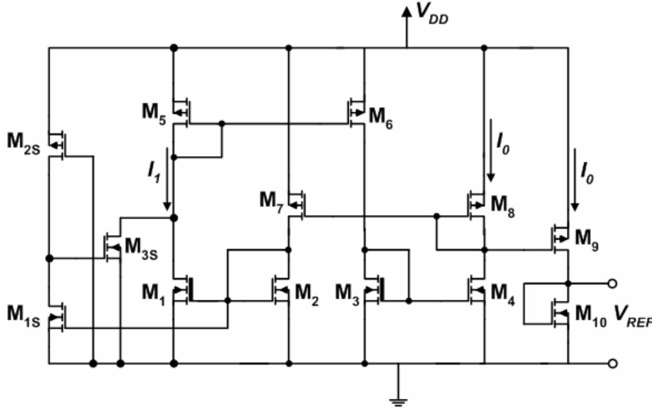

Fig. 1: Proposed Voltage Reference Circuit.

$$I_D = \mu V_T^2 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{th}}{mV_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right], \quad (2)$$

where μ is the electron mobility in the channel, V_T is the thermal voltage, V_{th} is the threshold voltage, m is the subthreshold swing parameter, λ is the channel length modulation coefficient, W and L are the channel width and length, respectively. In the following, the integer subscript i will be added to quantities referred to transistor M_i. The gate-source voltages of M_1 and M_2 (M_3 and M_4) are identical and can be extracted from (1) and (2) by considering M_1 and M_3 in subthreshold with drain current I_1 and M_2 and M_4 in saturation with a drain current I_0. Then, by enforcing $V_{GS1} = V_{GS2}$ and $V_{GS3} = V_{GS4}$, we have

$$V_{th1} + mV_T \ln\left(\frac{I_1}{\mu V_T^2 W_1 / L_1}\right) = V_{th2} + \sqrt{\frac{2I_0}{\mu C_{ox} W_2 / L_2}}, \quad (3)$$

$$V_{th3} + mV_T \ln\left(\frac{I_1}{\mu V_T^2 W_3 / L_3}\right) = V_{th4} + \sqrt{\frac{2I_0}{\mu C_{ox} W_4 / L_4}}, \quad (4)$$

where we have neglected channel length modulation (λ=0) and have set the term between square brackets in (2) to unity. Obviously, since the source terminals of all NMOS transistors are grounded, the body effect plays no role and $V_{th1} = V_{th3}$ and $V_{th2} = V_{th4}$. By subtracting (3) from (4), we can extract the expression of the current I_0:

$$I_0 = \frac{\mu C_{ox} W_4 / L_4}{2(N-1)^2} m^2 V_T^2 \ln^2\left(\frac{W_3 / L_3}{W_1 / L_1}\right), \quad (5)$$

where we define $N = \sqrt{(W_4 / L_4)/(W_2 / L_2)}$.

Such current is then injected into the diode connected transistor M_{10}, in order to generate a temperature compensated reference voltage. M_{10} operates in the saturation region and then by using (1) and (5), we can derive the output voltage V_{REF}

$$V_{REF} = V_{th10} + \frac{mV_T}{N-1}\sqrt{\frac{W_4 / L_4}{W_{10} / L_{10}}} \ln\left(\frac{W_3 / L_3}{W_1 / L_1}\right). \quad (6)$$

The proposed configuration of the voltage reference generator allows us to generate the current I_0 without using any resistance, that are conversely used in similar types of circuits [2, 8]. This is particularly important in the case of an ultra-low-power voltage reference generator because a very large resistance would be necessary to generate the small required current I_0 (some tens of nA). As a consequence, the proposed circuit topology allows us to drastically reduce the area occupation on the chip, as will be shown later from comparison with the literature

Since transistors M_2, M_3, M_5, M_8 and M_{10} are diode-connected, almost all the variation of the supply voltage drops on the drain-source voltages of transistors M_6, M_7, M_9 of the current mirrors, and on the drain-source voltages of transistors M_1, M_4. As a consequence, in order to drastically reduce the channel length modulation effect, the channel length of all the transistors in the current mirrors and of M_4 must be quite large and the drain-source voltage of M_1, which operates in the subthreshold region, must be much larger than V_T so that the V_{DS} dependence of the current in (2) becomes negligible.

The minimum power consumption of the proposed voltage reference generator and then the minimum acceptable value of the bias current I_0 is imposed by M_2, M_4 and M_{10}, which must operate in the saturation region. By assuming that $W_4/L_4 > W_2/L_2$, if M_4 operates in the saturation region with $V_{GS4} > V_{th4}$ then M2, which has the same drain current, will work in the saturation region as well. In such condition, the minimum current I_0 can be evaluated by imposing that M_4 operates in the saturation region with $V_{GS4} = V_{th4}$. The minimum currents I_{0MIN} and I_{1MIN} have thus the following expressions,

$$I_{0MIN} = \frac{\mu C_{ox} W_2 / L_2}{2} m^2 V_T^2 \ln^2\left(\frac{W_3 / L_3}{W_1 / L_1}\right), \quad (7)$$

$$I_{1MIN} = \mu V_T^2 (W_3 / L_3) \exp\left(-\frac{V_{th3} - V_{th4}}{mV_T}\right). \quad (8)$$

As clear from (7) and (8), in order to achieve a small power consumption, we have to choose small k_2 and k_3. In order to ensure the operation of M_{10} in the saturation region when $I_0 = I_{0MIN}$, k_{10} must be smaller than k_4.

Since the reference voltage generator has two stable states, corresponding to the current given by (5) and to zero current, a start-up circuit (formed by M_{1S}-M_{3S}) is used to ensure that the former stable state is achieved.

III. Supply Voltage Dynamic Range

The minimum supply voltage is imposed by the current generator circuit. In particular, we have to ensure that M_5 operates in the saturation region with $V_{GS5} < V_{th5}$ (V_{th5} = -0.75 V) and that M_1 has a drain-source voltage of at least 100 mV so that the V_{DS} dependence of the current in M_1

can be neglected. Consequently, the following expression has to be satisfied,

$$V_{DD} > |V_{GS5}| + V_{DS1MIN} \,. \tag{9}$$

Then the supply voltage must be larger then 0.9 V in the AMS 0.35 µm CMOS process. Such voltage is also sufficient to ensure the operation of M_4 and M_8 in the saturation region. The maximum supply voltage is imposed by the maximum drain-source voltage allowed for MOS transistors, as shown below,

$$V_{DD} < |V_{DS9MAX}| + V_{REF} \,. \tag{10}$$

Since in the AMS 0.35 µm CMOS process the maximum value for the drain-source voltage of a MOS transistor is 3.3 V, the maximum value of the supply voltage is about 4 V.

IV. TEMPERATURE COMPENSATION

As a first approximation we can consider that the threshold voltage of an NMOS transistor decreases linearly with the temperature:

$$V_{th}(T) = V_{th}(T_0) - K_{tn}(T - T_0) \,, \tag{11}$$

where K_{tn} is a BSIM3v3 coefficient and in our technology it is 0.33 mV/°C. By differentiating (6) with respect to the temperature and taking into account (11), one obtains

$$\frac{\partial V_{REF}}{\partial T} = -K_{tn} + \frac{m}{N-1}\frac{k_B}{q}\sqrt{\frac{W_4/L_4}{W_{10}/L_{10}}}\ln\left(\frac{W_3/L_3}{W_1/L_1}\right), \tag{12}$$

where k_B is the Boltzmann constant and q is the electron charge. As clear from (12), the temperature coefficient is independent of the temperature dependence of the carrier mobility. Indeed, in virtue of the topology used, a perfect suppression of the temperature dependence of the mobility is achieved; this leads to a smaller temperature coefficient compared to cases in which the temperature dependence of the mobility is compensated only at the reference temperature [8], degrading the temperature coefficient when moving away from the reference temperature. By setting (12) to zero, we obtain the condition

$$\sqrt{\frac{W_4/L_4}{W_{10}/L_{10}}} = \frac{K_{tn}(N-1)}{m\frac{k_B}{q}\ln\left(\frac{W_3/L_3}{W_1/L_1}\right)} \,. \tag{13}$$

Therefore, if (13) is satisfied, we obtain that the temperature coefficient (12) is zero for any temperature. It is clear that this is true within the approximation done in (11) and the simplified transistor characteristics (1) and (2).

V. CHANNEL LENGTH MODULATION EFFECT

In order to take into account the channel length modulation effect on the temperature coefficient, we have to consider that $\lambda \neq 0$ for a MOS in the saturation region. For the transistors in the subthreshold region, instead, if the drain-source voltage is larger than V_T, we can neglect V_{DS}. Since M_2 is diode-connected, we have only considered the channel

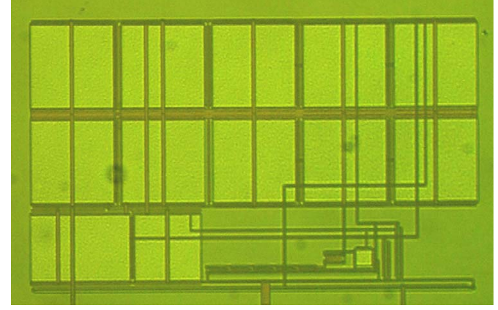

Fig. 2: Die Photograph (core).

length modulation effect on M_4. By assuming that the channel length of M_4 is sufficiently large to ensure $\lambda V_{DS} \ll 1$, and by following the same procedure used to calculate (12), the temperature coefficient is, to first order in λV_{DS} and when (13) holds:

$$\frac{\partial V_{REF}}{\partial T} = -\frac{\lambda K_{tn}}{N-1}\left[V_{DD} - |V_{th8}| - (V_{REF0} - V_{th10})\left(2\sqrt{\frac{W_{10}/L_{10}}{W_8/L_8}} - \frac{K_{tp}}{K_{tn}}\right)\right] \tag{14}$$

where K_{tp} is the temperature coefficient for the threshold voltage of a PMOS and V_{REF0} is the reference voltage for λ=0. We can choose to dimension M_8 so that for a supply voltage in the middle of the supply voltage range (V_{DD} = 2.45 V), expression (14) becomes zero, obtaining,

$$\sqrt{\frac{W_{10}/L_{10}}{W_8/L_8}} = \frac{K_{tp}}{2K_{tn}} + \frac{V_{DD} - |V_{th8}|}{2(V_{REF0} - V_{th10})} \,. \tag{15}$$

From (14) it is evident that, for $V_{DD} > 2.45$ V ($V_{DD} < 2.45$ V), the temperature coefficient is negative (positive), as shown later.

VI. EXPERIMENTAL RESULTS

The proposed voltage reference has been implemented with AMS 0.35 µm CMOS process. The die photograph is shown in Fig. 2. Measurements show that the proposed voltage reference generates a mean reference voltage of about 670 mV with a variation of 5.67 mV at room temperature, when the supply voltage varies from 0.9 V to 4 V, as shown in Fig. 3a. The power supply rejection ratio, without any filtering capacitor, is -47 dB at 100 Hz and -40 dB at 10 MHz, for the smallest supply voltage. At larger supply voltage the power supply rejection ratio decreases to -53 dB at 100 Hz and to -42 dB at 10 MHz, as shown in Fig. 3b. Fig. 4 shows the output voltage dependence on temperature for different values of the supply voltage. The measured temperature coefficient at V_{DD} = 2 V and V_{DD} = 3 V is 10 ppm/°C and 13 ppm/°C, respectively, and increases to 18 and 20 ppm/°C at V_{DD} = 4 V and V_{DD} = 0.9 V, respectively, corresponding to the maximum and minimum supply voltage. At 80 °C the current drawn at the maximum supply voltage is 70 nA and at the minimum supply voltage is 50nA. At room temperature, instead, the current drawn at the maximum supply voltage is 55 nA and at the minimum

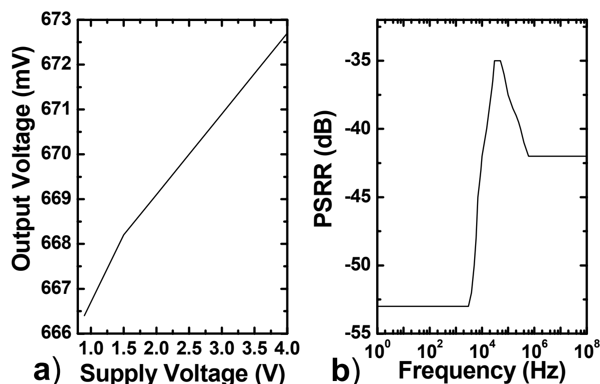

Fig. 3: Experiments: a) Output Voltage vs. Supply voltage at room temperature, b) PSRR at room temperature and for a supply voltage of 2 V.

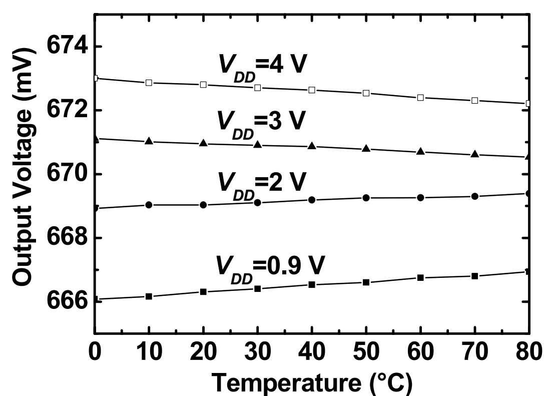

Fig. 4: Measured output voltage vs. temperature for 4 values of the supply voltage.

supply voltage is 40 nA. The occupied chip area is 0.045 mm^2. A comparison with best performing published voltage reference circuits fabricated with a standard CMOS process is shown in Table I. It can be noted that the proposed voltage reference has the smallest temperature coefficient, the minimum supply voltage and by large the smallest power consumption, in the tens of nW range. The PSRR and the line sensitivity are comparable to other solutions already presented in the literature.

VII. Conclusion

A low-voltage, extreme low-power voltage reference generator implemented in AMS 0.35 µm CMOS has been presented. The design conditions to minimize the power consumption and the temperature coefficient are described in detail. The complete suppression of the temperature dependence of mobility in a wide temperature range, the compensation of the channel length modulation effect on the temperature coefficient, and the elimination of the body effect have allowed us to obtain a very small temperature coefficient of 10 ppm/°C. The minimum supply voltage of only 0.9 V and the maximum quiescent current of only 70 nA leads to a total absorbed power in the decananowatt range, that makes the circuit very attractive for nanopower applications.

TABLE I: Comparison With Voltage Reference Generators Available in the Literature

	This work	Leung et al. [8]	Leung et al. [2]	De Vita et al. [9]
Technology	0.35 µm CMOS	0.6 µm CMOS	0.6 µm CMOS	0.35 µm CMOS
Supply Voltage (V)	0.9 to 4	1.4 to 3	0.98 to 1.5	1.5 to 4.3
Supply Current (µA)	0.04@0.9V 0.055@4V	<9.7	<18	0.08@1.5 V 0.11@4.3V
V_{ref}	670 mV	309.3mV	603 mV	891.1 mV
TC (ppm/°C)	10	36.9	15	12
Line Sensitivity	0.27 %/V	0.08 %/V	0.73 %/V	0.46 %/V
PSRR @100 Hz @10 MHz	V_{DD}=0.9 V -47 dB -40 dB	V_{DD}=1.4 V -47 dB -20 dB	V_{DD}=0.98 V -44 dB -17 dB	V_{DD}=1.5 -59 dB -52 dB
Die area (mm^2)	0.045	0.055	0.24	0.015

Acknowledgment

This work has been supported by Fondazione Cassa di Risparmio di Pisa. The authors wish to thank Prof. P. Bruschi for support in the characterization.

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