Physical Model for NAND operation in SOI and Body-Tied Nanocrystal FinFLASH memories

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Abstract

Here we present a semi-analytical model for nanocrystal-based (NCs) FinFLASH memories under uniform stress: Fowler-Nordheim (FN) write/erase, gate disturb and data retention are addressed. This model is able to catch the essential features related to the non-uniform trapped charge distribution in such a complex 3D structure. Both body tied and SOI devices are included in the model. Main conclusions are related to the different characteristic times of charge trapping over fin corners or planar fin regions: double dynamics during programming, intrinsic disturb immunity of written state in FF cells. The aspect ratio impact on ΔV_{TH} is also evaluated showing a slightly better performance of body tied devices.

Introduction

The increasing demand of higher bit density in NAND Flash memories is pushing the research on novel architectures as trigate FinFLASH (FF) (Fig. 1)[1,2]. Conjugated to the discrete storage node approach, it offers the possibility of scaled dielectrics and operating voltages, along with high current drivability. Moreover the possibility of 3D integration [3] pushes the investigation towards both body-tied (BT) and SOI FF architectures.

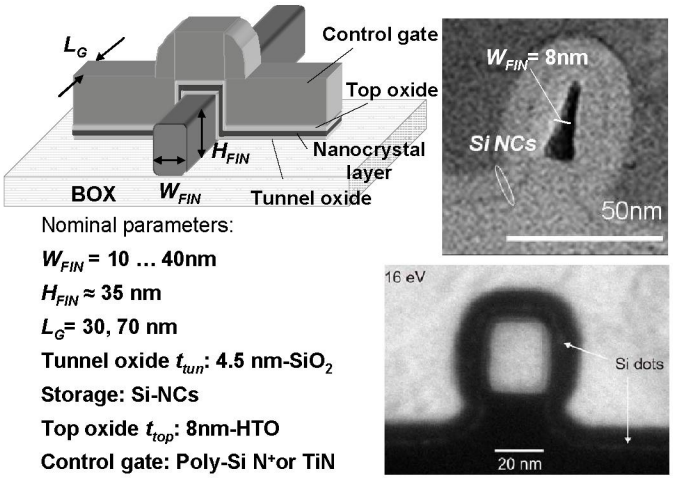

Fig. 1: Structure and TEM images (along vertical cuts) of NC SOI FF cells tested in this work [8]. Nominal parameters are indicated.

Physical models to capture the electrical behavior of these cells are needed, as 3D TCAD simulations are time consuming and sometime of difficult interpretation.

TCAD simulations and semi-analytical model

The purpose of our study is to provide a simple physical model to correctly describe the memory functionality of NC SOI and BT FinFLASH included in a NAND matrix. At cell level, notwithstanding the absence of body contact, SOI fins can be driven in inversion or accumulation with carriers supplied by source and drain regions. In particular during erase, the GIDL effect, strongly enhanced in trigate cells[4], provides holes to drive SOI fins into accumulation and to pin the fin potential at ground. This reasoning is extended to cells included in NAND matrix, if other cells on the same bitline are operated as on-pass gates [1, 3]. Based on these considerations herewith we will focus on cell electrical behavior.

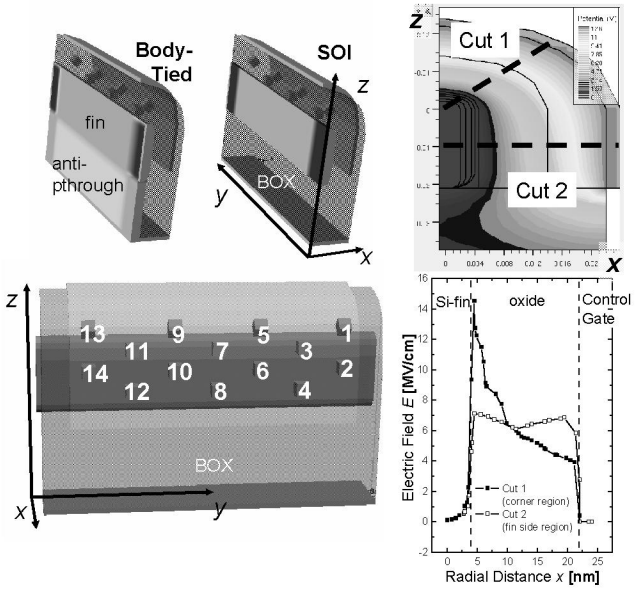

Fig. 2: **(left)** Bird's eye views of SOI and BT structures used in our simulations. Write/erase simulations use the self-consistent Fowler-Nordheim injection module [5]. **(right)** Analysis of the electric field distribution through two cuts at corner and fin side. Two different electrical behaviors are evident.

Provided the complex 3D structure, some insight given by 3D TCAD simulations [5] will be useful for the development of the semi-analytical model. In Fig. 2 we have represented three bird's eye views of SOI and BT structures used in our simulations and we highlighted two potential cuts at fin side and corner level, which put in evidence the different electrostatic behavior, common to both SOI and BT structures: the planar region where the electric field E is constant through the oxides and the corner region where E is strongly varying.

We have developed a semi-analytical model that decouples the FN write/erase step from the reading step of trapped charges in NC. Herewith are provided the main ideas.

Tunneling model – Based on Fig. 2, we can consider a FinFLASH device under uniform stress (see Fig. 3) as composed of planar regions along the top and sides of the fin, and of corner regions that can be approximated by circles of

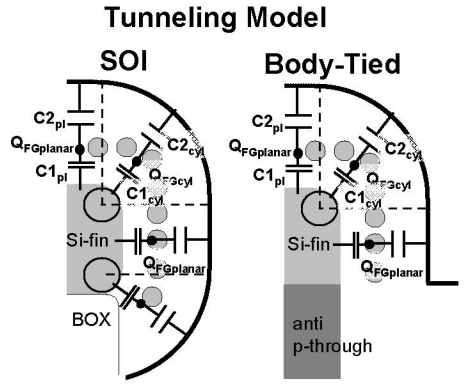

Fig. 3: Schematic illustration of the floating gate model for the tunneling model. During write/erase fin interfaces are approximated as infinite reservoirs of carriers (i.e. metals), with pinned interface potential. In the bottom region SOI structures present two bottom corner regions, result of Si body etch and subsequent oxidation steps.

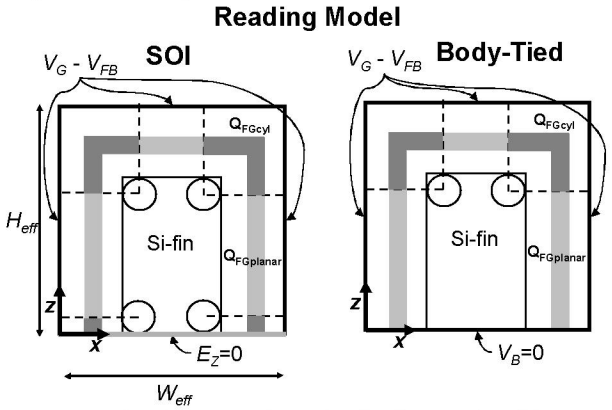

Fig. 4: Green's function approach to solve the electrostatics of the BT and SOI cells, in the reading model. The SOI structure is treated as a metallic box with mixed boundary conditions: the control gate provides (V_G-V_{FB}) boundary condition, while the SOI/BOX interface a null perpendicular E condition [7]. The BT structure is treated as a metallic box with Dirichlet boundary conditions: the control gate provides (V_G-V_{FB}) boundary condition, while the interface between the intrinsic fin and the anti-punchthrough doped region pins the potential at the back gate level.

curvature radius Rc. Indeed the tunnelling associated to planar/corner regions between the fin, nanocrystals, control gate can be treated through a Floating Gate approach [6], where dots are intrinsic and fin/control gates are metallic. Specific expressions for planar (fin top and side) and cylindrical (fin corner) regions are derived (Table 1), where the transparency is calculated through the WKB approach. It should be stressed that in our model tunneling is identical in SOI and BT structures, because, as explained in the introduction, in both architecture the fin potential is considered pinned at ground.

Reading model – Once the distribution of trapped charge over corners and planar regions is calculated, its impact on fin electrostatics is obtained through the Green's function approach [7], here extended to BT devices (see Fig. 4). In the SOI cell, the BOX/SOI interface is treated as an interface with null perpendicular electric field component, while in the BT cell, the bottom fin contact is treated as grounded. We remark that the impact of device aspect ratio is crucial in the reading module. This module can be efficiently integrated without modifications in a tunneling model tailored for SONOS FF cells.

Model vs 3D simulations

To test the solidity of our model we separately compare the analytical results from programming and reading operations with semiclassical numerical simulations [5], which are adequate for fins with minimum dimensions larger than 10 nm.

Tunneling model equations

$$\frac{dQ_{FG_i}}{dt} = J_{in_i} - J_{out_i} \qquad i = \text{cyl, planar}$$

tunnelling current equation (electrons)

$$|T_i|^2 = \exp\left(-2\sum_n \sqrt{\frac{2m}{\hbar^2}\cdot(V_i(r_n)-U)}\cdot\delta r_n\right)$$

$$i = \text{cyl, planar}$$

transparency (WKB approach)

Reading model equations

$$\Psi_{q_{SOI}} = \frac{-4q}{\epsilon_{si}\pi^2 W_{\text{eff}} 2H_{\text{eff}}}\sum_{m,p}^{\infty}\frac{\sin\left(\frac{m\pi x_0}{W_{\text{eff}}}\right)\sin\left(\frac{p\pi(z_0-H_{\text{eff}})}{2H_{\text{eff}}}\right)}{m^2/W_{\text{eff}}^2+p^2/4H_{\text{eff}}^2}\cdot$$

$$\cdot\sin\left(\frac{m\pi x}{W_{\text{eff}}}\right)\sin\left(\frac{p\pi(z-H_{\text{eff}})}{2H_{\text{eff}}}\right),$$

potential in (x,z) of point charge in (x_0, z_0) in SOI structure (see Fig. 4)

$$\Psi_{q_{BT}} = \frac{-4q}{\epsilon_{si}\pi^2 W_{\text{eff}} H_{\text{eff}}}\sum_{m,p}^{\infty}\frac{\sin\left(\frac{m\pi x_0}{W_{\text{eff}}}\right)\sin\left(\frac{p\pi z_0}{H_{\text{eff}}}\right)}{m^2/W_{\text{eff}}^2+p^2/H_{\text{eff}}^2}\cdot$$

$$\cdot\sin\left(\frac{m\pi x}{W_{\text{eff}}}\right)\sin\left(\frac{p\pi z}{H_{\text{eff}}}\right),$$

potential in (x,z) of point charge in (x_0, z_0) in BT structure (see Fig. 4)

Table 1: Highlights on equations involved in the model. The tunneling current equation [6], the transparency through WKB approach; the charge impact in the SOI [7] and BT structure ($J_{in(out)}$ are the incoming(outgoing) currents with respect to floating node; $V_i(r)$ barrier potential profile; U electron energy, r spatial coordinate; W_{eff}, H_{eff} specified in Fig. 4). Due to the discrete nature of NCs, we consider 2/3 of active area covered by dots [9] (parameter fixed in the model).

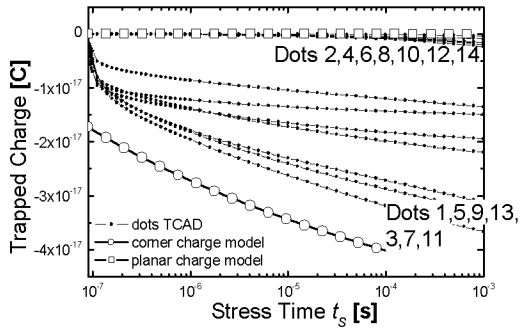

Fig. 5: Charging dynamics in nanocrystals around the fin from TCAD simulations. The model is able to capture the completely different charging dynamics of dots over fin side, with respect to dots over corners. For nanocrystal number look at Fig. 2.

Program operation – In Fig. 5 we compare with simulation the model dynamics in cylindrical and planar region. The model is able to capture the completely different charging dynamics of dots over corners as well that of dots over fin side, even with the same tunnel oxide thickness. We stress that program simulations provide identical results on BT and SOI cells (not shown here), except for nanocrystals near the bottom of the fin, where the dynamics is slightly different.

Read operation – In Fig. 6 we compare the reading model performance with TCAD simulations for SOI and BT devices, for a uniform distribution of trapped charge: a good agreement is noticed in the subthreshold slope and ΔV_{TH} for both device architectures.

Model vs data on SOI FinFLASH cells

We tested nanocrystal SOI FF whose nominal dimensions are provided in Fig. 1 on different aspects covering FN write/erase, data retention and disturb.

In Fig. 7 we fit a complete write/erase dynamics on an ultra scaled device (W_{FIN}/L_{FIN}=10/30 nm). It is worth noticing the similar program/erase transients that further confirm the hypotheses, on our tunneling model, to pin the SOI fin potential at ground during write/erase. In Fig. 8 we remark a fair agreement with data concerning ΔV_{TH} vs W_{FIN}. In Fig. 9, we use our model to fit data retention and disturb properties on written state. It is apparent the intrinsic immunity of FF cell in the written state to gate disturb. The explanation of this novel feature is given in Fig. 10-11. Indeed, after the write pulse we have very different trapped charge density on the corner and planar regions: during data retention, we see in Fig. 10 that corners are predominantly discharged through the tunneling oxide. The small amount of charge on planar region remains constant. Globally we have a ΔV_{TH} loss (Fig. 9). If we apply a gate disturb of V_G=8V, we have two competing behaviors: the corner charge leaks through top oxide, while planar charge is injected through the bottom oxide. Thus globally we obtain ΔV_{TH} that initially decreases and then increases (Fig. 9). This is intrinsically due to the different charge/discharge dynamics of corner and planar regions. On the other hand, due to the same effect, the gate disturb on the erased state could be a critical problem, due to the write boost at corners even at small V_G stress.

Extrapolation & Conclusion

We focus on the cell aspect ratio impact on ΔV_{TH} performance in Fig. 12a for SOI cell and Fig. 12b for BT cells. We note that, for the same aspect ratio, BT cells present higher ΔV_{TH} than SOI cells. Due to the injection boost at corners, reducing the fin dimensions is beneficial to the ΔV_{TH}, because of a better control of trapped charge over channel conduction.

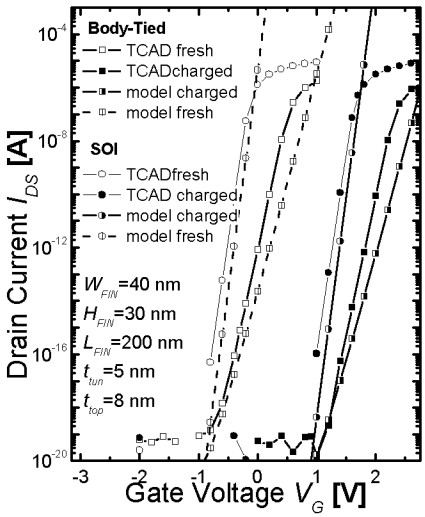

Fig. 6: TCAD simulations and model of BT and SOI cells uniformly charged around fin (5e12 electr/cm^2). The BT shows a higher subthreshold slope than SOI as the fin bottom region is strongly coupled to the back gate (V=0) through the antipunchthrough region.

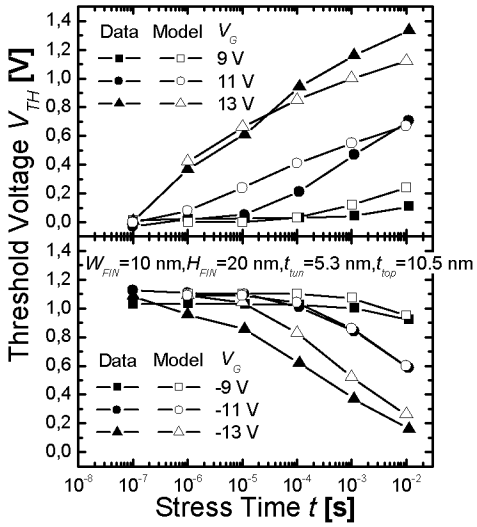

Fig. 7: Fit on write/erase characteristics of the most scaled device (W_{FIN}/L_{FIN}=10/30 nm).

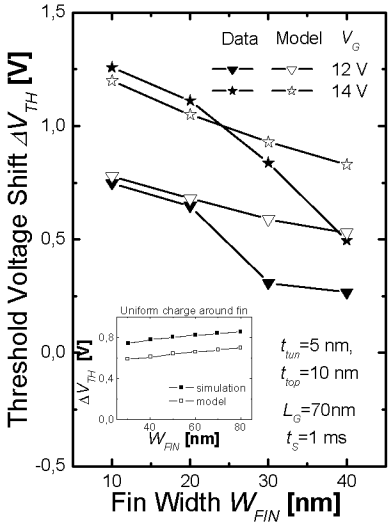

Fig. 8: Fit of data on ΔV_{TH} vs W_{FIN}. This electrical behavior is a typical mark of injection boost at corners. To be compared with the simulation [10] & model results of inset, where it is supposed that a uniform charge distribution is trapped around fin.

However, whereas in BT devices we can scale equally W_{FIN} and H_{FIN} obtaining the same effect, in SOI devices scaling H_{FIN} is more effective than scaling W_{FIN}, for H_{FIN}>2*W_{FIN}. In other words, from a ΔV_{TH} performance point of view, it is better to have short (small H_{FIN}) and wide (large W_{FIN}) SOI devices than tall and thin ones. Moreover, provided that cells with smaller fin suffer of less ΔV_{TH} fluctuation than thinner ones [11], the scaling efforts on SOI and BT devices should be addressed firstly to the reduction of H_{FIN}. This extrapolation encourages a vertical 3D stacked integration of these cells.

For the first time it has been presented a simple physical model, that highlights the essential electrical features of NC FF devices in SOI and BT architecture under uniform tunnelling. Among main results explained by our model we highlight the following:

- FF devices show different dynamics associated to corner vs planar region trapping, which allows to explain the intrinsic immunity of NC FF cells to gate disturb in the written state. Disturb remains a critical issue on erased state.
- Our model is able to provide contour plots as Fig. 12 that quantitatively show the impact of scaling on ΔV_{TH} in both SOI and BT architectures.

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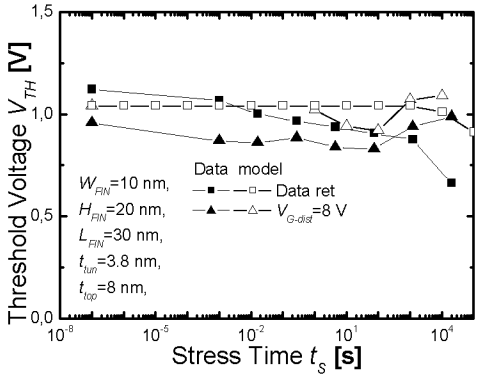

Fig. 9 : Data retention (room temperature) and gate disturb vs results from our model.

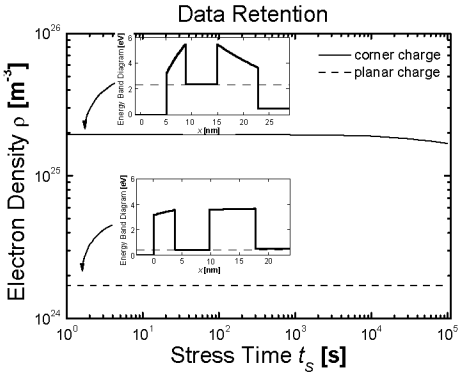

Fig. 10: Trapped electron density during data retention obtained by our model. A global charge loss is foreseen.

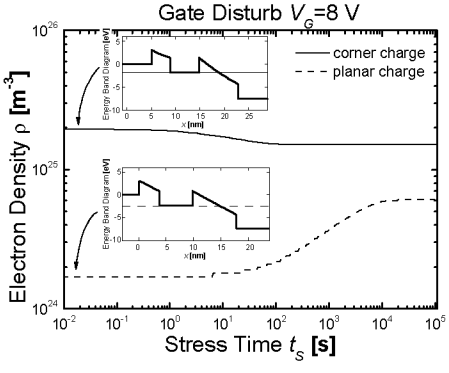

Fig. 11 : Trapped electron density during gate disturb at V_G=8 V obtained with our model. Two competing behaviors are apparent.

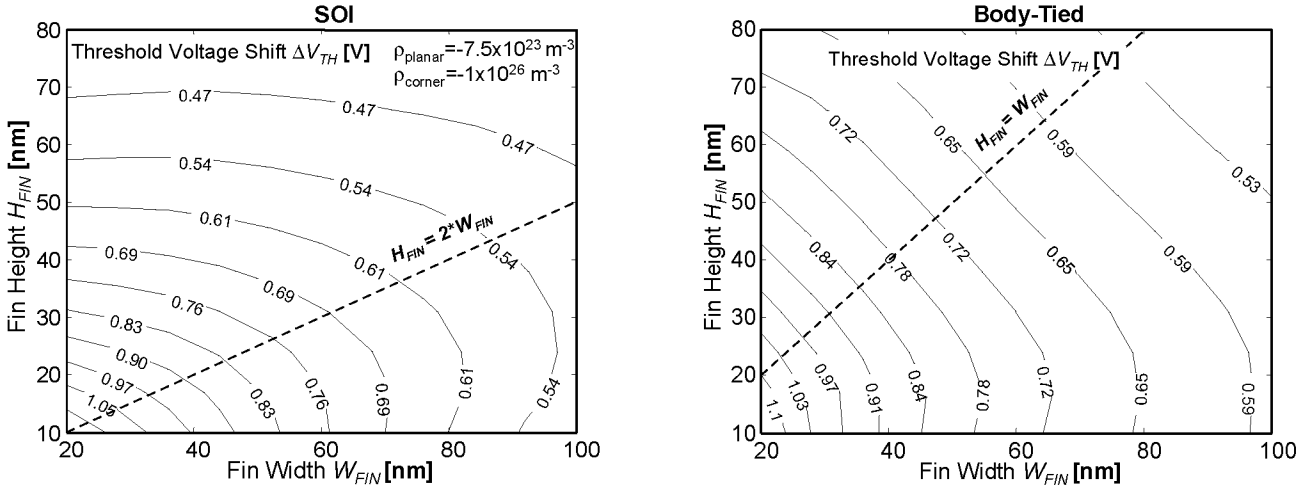

Fig. 12: Contour plot of the ΔV_{TH} with respect to fin width and height for ***(a)*** SOI and ***(b)*** BT cells. Hypotheses are a write step at V_G=15 V t=1 µs, and fin features as nominal values of Fig. 1. Reducing fin features is beneficial for both architectures. In SOI cells the region where H_{FIN}>2*W_{FIN} shows a weak dependence of ΔV_{TH} with respect to fin width. On the other hand, the impact of W_{FIN} and H_{FIN} on ΔV_{TH} in BT cells is almost symmetric.