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A model for MOS gate stack quality evaluation based on the gate current 1/f noise

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Modeling the gate current 1/f noise and its application to advanced CMOS devices

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Abstract

In this work we propose an analytical model for the gate current 1/f noise in CMOS devices. The model is based on a simple idea: one electron trapped in the dielectric switches-off the tunneling through the oxide over an effective blocking area. The model allows evaluating the effective trap density inside the gate dielectric as a function of energy from measurements of the gate current 1/f noise versus gate voltage. Experimental data on advanced CMOS devices confirm the validity and the usefulness of the proposed model.

1. Introduction

Large gate leakage in CMOS devices limits the accuracy of standard electrical measurement techniques used to evaluate the quality of the gate stack, such as charge pumping, combination of high frequency and quasi-static C-V and drain current 1/f noise measurements [1-3]. In this paper, we show how the same gate current which corrupts the information obtained by the standard analysis techniques can be used as a powerful source of information for assessing the quality of the gate stack in CMOS devices. This purpose is accomplished by introducing an analytical model for the gate current 1/f noise.

2. Gate current 1/f noise modeling

In this section we derive a model for the gate current 1/f noise in an n-channel MOSFET biased above the threshold voltage in the linear regime. The model is based on five assumptions:

i) The transfer of electrons from the channel conduction band to oxide traps and vice versa is due to elastic tunneling. We ignore the electron transfer between the oxide traps and the gate electrode.

ii) Electron trapping and detrapping cause a local fluctuation of the oxide conduction band profile thus causing an RTS in the gate current. We define the one-electron blocking area $a \equiv \Delta I / J_G$ where ΔI is the gate current RTS amplitude and J_G is the gate current per unit area when the trap is neutral. For simplicity a is assumed to be independent on trap location and gate bias.

iii) The oxide tunnel barrier seen by an electron is rectangular with height Φ_B. Since the wave function of an electron exponentially decays as the wave penetrates into the barrier, the tunneling time constant is given by

$$\tau = \tau_0 \exp(\alpha x) \quad (1)$$

where x is the distance from the substrate interface.

iv) The trap density per unit volume and energy N_T is assumed to be uniform in space.

v) The considered frequency interval is

$$f_{\min} << f << f_{\max} \quad (2)$$

where $f_{\min}$ and $f_{\max}$ can be obtained by evaluating the time constant (1) at the two interfaces.

Each trap causes an RTS in the gate current with amplitude $\Delta I = a J_G$, average time in the low state (filled trap) τ_{off} and average time in the high-state (empty trap) τ_{on}. Thus the power spectral density is

$$S_{RTS} = \frac{4(aJ_G)^2 R \tau_p}{(1+R)^2} \frac{1}{1+(2\pi f \tau_p)^2} \quad (3)$$

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where $(\tau_p)^{-1}=(\tau_{off})^{-1}+(\tau_{on})^{-1}$ and $R=\tau_{off}/\tau_{on}$. The power spectral density given by all the traps, assumed uncorrelated and with the same blocking area a, can be obtained as

$$S_{ig} = A\int_0^{t_{ox}}\int_{E_v}^{E_c} S_{RTS}(x,E)N_T(E)dEdx \quad (4)$$

where A is the device area, t_{ox} is the oxide thickness, E_V and E_C are the valence and conduction band edges of the oxide, respectively. By considering that the probability that a trap is filled is given by the Fermi-Dirac occupation factor and by taking into account only traps with energy E close to the Fermi level E_F, we obtain

$$S_{ig} = \frac{a^2 I_G{}^2 kTN_T(E_F)}{A\alpha f} \quad (5)$$

and hence

$$N_T(E_F) = \frac{A\alpha f S_{ig}}{a^2 I_G{}^2 kT} \quad (6)$$

Eq. 6 allows extracting the trap density as a function of energy from measurements of the gate current noise as a function of V_G. To this purpose the knowledge of the blocking area is required.

In order to estimate the one-electron blocking area, a semi-analytical model has been developed. If we assume that the tunnel current density is proportional to the tunneling probability, the one-electron blocking area is given by

$$a = \int_0^{\infty} 2\pi r\left[1-\frac{T(r)}{T_0}\right]dr \quad (7)$$

where $T(r)$ denotes the tunneling probability at a distance r from the trapped charge and T_0 is the tunneling probability when the trap is neutral. We can compute the tunneling probability with the WKB approximation for an electron at the Fermi energy

$$T(r) = \exp\left\{-\frac{4\pi}{\hbar}\int_0^{t_{ox}}\sqrt{2m^*[\phi_B - qFy + q\varphi(y,r)]}dy\right\} \quad (8)$$

where $\varphi(y,r)$ is the potential in the oxide at depth y from the channel and at a distance r from the trap and F is the electric field in the oxide. The potential $\varphi(y,r)$ has been computed with the method of the image charges, assuming that we have perfect conductors at both oxide interfaces. Fig. 1 shows the radius of the blocking area as a function of the trap relative position inside the dielectrics (0 corresponds to substrate interface and 1 to gate interface) for different values of the dielectric constant, oxide thickness and gate bias. Note that in all different conditions the blocking radius value can be approximated to 1 nm. As expected the radius decreases with the dielectric constant (see Fig. 1a), since the potential $\varphi(y,r)$ is inversely proportional to the dielectric constant. All the curves show a bell shape with maximum in the middle of the oxide layer and the radius increases with the oxide thickness (see Fig. 1b). These two observations can be easily explained since the radius increases if the metallic planes – that screen the electrostatic potential – are located at a higher distance from the trap. As shown in Fig. 1c, the blocking radius is almost independent on the applied gate voltage. These results indicate that the model assumption of the blocking area independence on trap position and gate bias is quite reasonable.

Eq. 5 suggests that the gate current 1/f noise scales as the square of the DC gate current I_G and the inverse of the gate area A. Thus it is natural to introduce a figure of merit for the quality of the gate stack as

$$GNP \equiv \frac{S_{ig} fA}{I_G^2} \quad (9)$$

which will be referred as gate noise parameter. From Eq. 5 and Eq. 9 we obtain

$$GNP = \frac{a^2 kTN_T(E_F)}{\alpha} \quad (10)$$

Although the trap density has a more direct physical meaning, in the experimental section we prefer to use this alternative parameter for two main reasons. First, the evaluation of the trap density from experimental data requires accurate estimations of a and α. Different values of these two parameters could be obtained by different researchers thus causing confusion in the gate

noise data comparison, while the GNP does not need such estimations. Second, GNP gives us a measure of the normalized gate current noise independent on the adopted model.

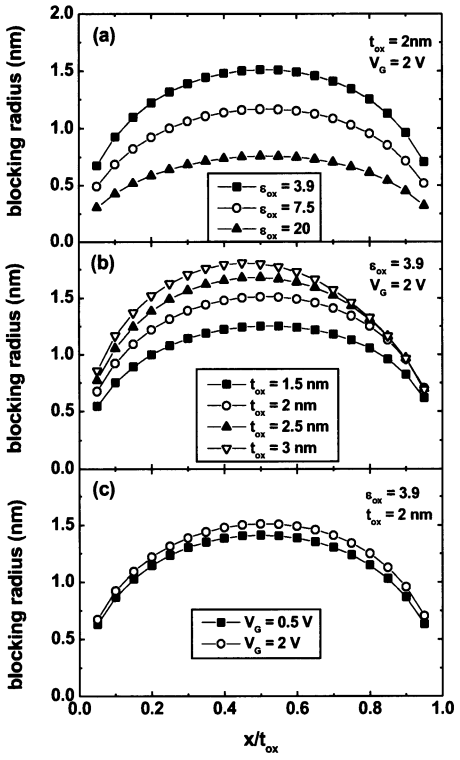

Figure 1. Radius of the one-electron blocking area as a function of the relative trap position inside the dielectric for different values of the dielectric constant (a), oxide thickness (b), gate voltage (c). In all cases a value close to 1 nm is obtained.

3 Model validation and application

The low frequency part of the gate current spectrum shows a typical $1/f^{\gamma}$ behavior. The cumulative distribution function (CDF) of γ for two different sample areas, 10^{-6}cm^2 and $2.8\text{x}10^{-8}$cm^2, are reported in Fig. 2. The devices have a gate stack composed by: 1nm of SiON as interfacial layer (IL), 2nm of HfSiON and a polysilicon gate (EOT=1.6nm). The higher dispersion of the γ value observed in smaller area devices indicates the presence of dominant RTS noise sources, as a consequence of the lower number of active traps. Fig. 3 shows the average value of the normalized gate current noise spectra AS_{ig}/I_G^2 for the two areas. In both cases a value of γ very close to 1 is obtained, thus supporting the idea that the 1/f noise originates from the superposition of RTS noise sources. In addition, these measurements confirm the area and the DC gate current dependence predicted by our model.

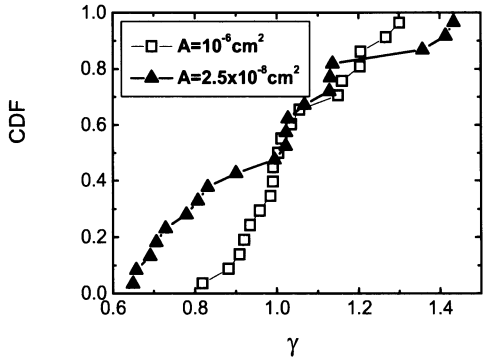

Figure 2. CDF of the γ value of the gate current noise spectrum for nMOSFETs with two different areas. A higher dispersion is observed for smaller area devices.

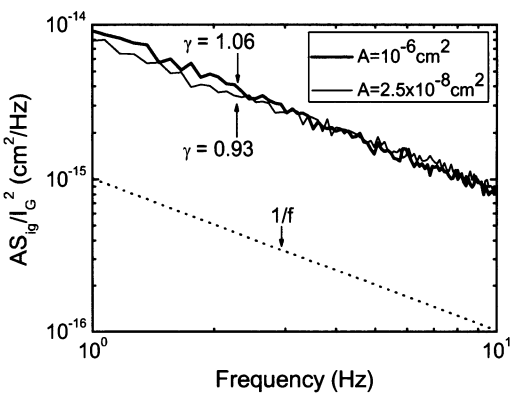

Figure 3. Normalized gate current noise spectra averaged over about 20 samples for the devices of Fig. 2. The two spectra are almost coincident with γ very close to 1.

Fig. 4 shows the GNP as a function of the gate bias for different gate dielectric materials: 2 nm SiO_2, 1nm SiON/2nm HfSiON (EOT=1.6nm) and 1nm SiON/4nm HfO_2 (EOT=1.8nm). All the devices are polysilicon gated. In samples with HfO_2 dielectric the GNP is three orders of magnitude higher with respect to the SiO_2 dielectric, while an intermediate value is observed for the HfSiON devices. The slightly different a and α values corresponding to the hafnium-based gate stacks cannot explain the large differences observed in the GNP values. Thus we conclude that the gate noise data indicate that hafnium-based dielectrics have a significantly higher trap density with respect to the reference SiO_2, in agreement with several other experimental works [4].

GNP values in high-k gate stacks with different IL thickness are reported in Fig. 5. One nMOSFET has the following gate stack: 0.4nm SiON IL/HfO_2 (EOT=0.9nm) and TiN/TaN as gate electrode. The gate stack of the other nMOSFET is constituted by: 0.9nm IL SiON/HfO_2 (EOT=1.4nm) and TiN as gate electrode. By increasing the IL thickness in the high-k gate stack, a lower GNP value is observed. This result is in agreement with other experimental works which report that the quality of the high-k gate stack improves by increasing the IL thickness [5].

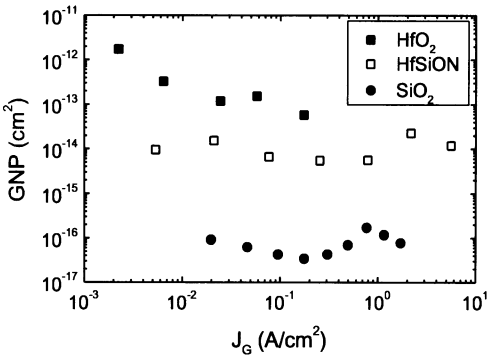

Figure 4. GNP as a function of the gate bias for different gate dielectric materials. Higher GNP values are observed for hafnium-based dielectrics.

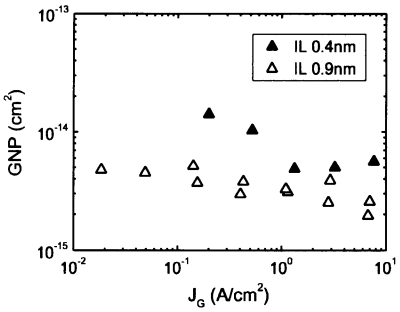

Figure 5. GNP as a function of the gate bias for high-k gate stacks with different SiON IL thickness. Higher GNP values are observed for thinner IL.

Conclusions

We have proposed an analytical model for the gate current 1/f noise in CMOS devices based on the assumption that one trapped electron switches off the conduction through the dielectric over an effective blocking area. We have reported that the radius of the blocking area depends smoothly on the gate bias and trap position and can be approximated to 1 nm. The main model advantage is that it allows evaluating the effective trap density in the dielectric from the gate current 1/f noise measurement. Experiments have confirmed the area and the DC gate current dependence predicted by the model. We have shown that the GNP, which is related to the effective trap density in the dielectrics on the basis of the proposed model, can be used as a sensitive probe of the gate stack quality in advanced CMOS devices.

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