Analytical and TCAD-supported Approach to Evaluate Intrinsic Process Variability in Nanoscale MOSFETs

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***Abstract*— We propose an approach to evaluate the effect on threshold voltage variability due to line edge roughness (LER) and to surface roughness (SR) fully based on analytical modeling or supported by a limited number of TCAD simulations to perform parameter sensitivity analysis. We show that in the case of a 32 nm ultra-thin-body SOI MOSFET and a 22 nm double-gate MOSFET our approach is capable to reproduce with very good accuracy the results obtained through 3D atomistic statistical simulation at a small computational cost. We believe the proposed approach can be a powerful tool to understand the role of the main variability sources and to explore the device design parameter space.**

I. INTRODUCTION

Intrinsic process variability is broadly considered one of the main factors limiting CMOS technology scaling [1]. The increased variability of device electrical parameters is already slowing down the adoption of the latest technology nodes by analog and mixed signal designers. For this reason, device structures and materials for the next CMOS technology nodes will also be chosen for their robustness to process variability. Indeed, one of the main reason ultra-thin-body MOSFETs with undoped channel and metal gate are considered for CMOS technology beyond the 32 nm node is the suppression of random dopant distribution as a source of threshold voltage variability. A methodology and modelling tools to quantitatively evaluate the variability of device electrical parameters as a function of device structure are therefore essential to guide device design and optimization.

In time, analytical models have been proposed to evaluate the impact of threshold voltage dispersion due to the discrete dopant distribution [2, 3] and to line edge roughness [4]. Analytical models are fundamental for understanding the main relevant physical mechanisms but are typically limited to simplified and idealized structures. Statistical simulations are very powerful for a quantitative assessment of the dispersion of electrical parameters of realistic devices [5-8], and also enable the use of doping profiles and geometry carefully calibrated with experiments. On the other hand, statistical simulations are very demanding from the computational point of view, and sometime may represent a "brute force" approach to an issue more easily accessible with other means [9, 10].

We believe that a complete analytical or quasi-analytical approach can provide important insights on the main sources of variability and on the ways to minimize their effect, and can enable a thorough exploration of the device design space, that would be prohibitive with a statistical simulation approach. In this paper, we propose an approach to evaluate the effect on threshold voltage variability due to line edge roughness (LER) and to Surface-Roughness (SR) fully based on analytical modeling or supported by a limited number of TCAD simulations to perform parameter sensitivity analysis.

We apply our proposed approach to two template devices used within the EC PULLNANO project for comparison of different simulation approaches: a 32 nm ultra-thin body SOI MOSFET and a 22 nm double-gate MOSFET. These structures are not close to devices used for the 32 nm and 22 nm CMOS technologies, but are good templates for comparing simulation approaches. Device structures are shown in Fig. 1, and details can be found in [11]. As we shall show, results obtained with our proposed approach are very close to those obtained through 3D atomistic statistical simulations on the same template devices [8]. Both devices have undoped channel.

II. APPROACH

The approach we propose requires the identification of the relevant quantities that translate process variability into variability of electrical parameters. It involves the following three steps:

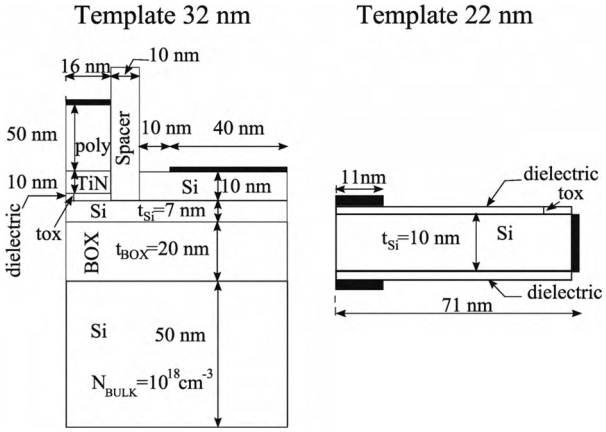

Figure 1: Template structures for the 32 nm UTB SOI MOSFET (left) and the 22 nm double-gate MOSFET (right). The device is symmetrical. Doping profiles for source and drain are described in [11]. The effective oxide thickness t_{ox} is 1.2 nm for the 32 nm template and 1.1 nm for the 22 nm template.

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- All variability sources (process and geometry) are translated in terms of dispersion of a set of synthetic parameters.
- Independent variability sources and synthetic parameters are identified.
- The contribution to the dispersion of electrical parameters (e.g. the threshold voltage V_{th}) of each independent source is evaluated through sensitivity analysis. This step is based on the assumption that the effect of each source is sufficiently small that linearization is applicable. Indeed, an ex-post evaluation of results obtained with 3D atomistic statistical simulations of separate and combined variability sources (for example [8]) confirms that linearization is applicable.

Let us consider the 32 nm template, with the help of Fig. 2. We can translate line edge roughness in terms of the dispersion of the average position of both gate edges along the y axis ($y = 0 + y_1$ and $y = L + y_2$) in Fig. 2a. This in turn translates into gate length dispersion. Surface roughness is translated into the dispersion of the average position of the interface between adjacent layers: the offsets are x_1, x_2, x_3 in Fig. 2b.

We assume that parameters y_1, y_2, x_1, x_2, x_3 are only affected by LER and SR and are physically independent. We start by considering the effect the offset of the position between two adjacent Si-SiO_2 layers $(x_i, i = 1,2,3)$. The first step is to evaluate the variance of x_i, $\sigma_{x_i}^2$. Interface roughness leads to a local fluctuation of the interface with respect to the nominal position that has zero mean value and exponential autocorrelation, with mean square amplitude Δ_S and correlation length Λ_S. The variance of the average position of the interface in the case of $L, W >> \Lambda_S$ is

$$\sigma_{x_1}^2 = \sigma_{x_2}^2 = \sigma_{x_3}^2 = \sigma_{SR}^2 = \frac{2\pi\Lambda_S^2\Delta_S^2}{LW} \tag{1}$$

Then, using linearization and the hypothesis of independence of the different parameters, the variance of V_{th} due to surface roughness is:

$$\sigma_{V_{th}SR}^2 = \left(\frac{\partial V_{th}}{\partial x_1}\right)^2 \sigma_{x1}^2 + \left(\frac{\partial V_{th}}{\partial x_2}\right)^2 \sigma_{x2}^2 + \left(\frac{\partial V_{th}}{\partial x_3}\right)^2 \sigma_{x3}^2 \tag{2}$$

The partial derivatives can be expressed as:

$$\begin{aligned} &\frac{\partial V_{th}}{\partial x_1} = -\frac{\partial V_{th}}{\partial t_{ox}}; \qquad \frac{\partial V_{th}}{\partial x_2} = \frac{\partial V_{th}}{\partial t_{ox}} - \frac{\partial V_{th}}{\partial t_{Si}}; \\ &\frac{\partial V_{th}}{\partial x_3} = \frac{\partial V_{th}}{\partial t_{Si}} - \frac{\partial V_{th}}{\partial t_{BOX}}. \end{aligned} \tag{3}$$

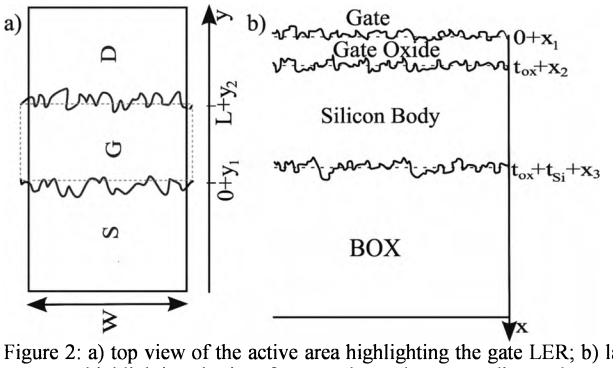

Figure 2: a) top view of the active area highlighting the gate LER; b) layered structure highlighting the interface roughness between adjacent layers in the 32 nm template.

As far as LER is concerned, assuming an exponential autocorrelation function of correlation length Λ_L and mean square amplitude Δ_L, one finds:

$$\sigma_{y1}^2 = \sigma_{y1}^2 = \sigma_{LER}^2 = \frac{2\Lambda_L\Delta_L^2}{W}\left\{1 - \frac{\Lambda_L}{W}\left[1 - \exp(-W/\Lambda_L)\right]\right\} \tag{4}$$

The variance of V_{th} due to line edge roughness is:

$$\sigma_{V_{th}LER}^2 = \left(\frac{\partial V_{th}}{\partial y_1}\right)^2 \sigma_{y_1}^2 + \left(\frac{\partial V_{th}}{\partial y_2}\right)^2 \sigma_{y_2}^2 = 2\left(\frac{\partial V_{th}}{\partial L}\right)^2 \sigma_{LER}^2 \tag{5}$$

All required derivatives can be computed with TCAD simulations or with an appropriate analytical model. The total variance of the threshold voltage is computed by summing the variances due to all independent physical effects.

As can be seen, if the appropriate independent parameters are identified, the evaluation of the dispersion of the threshold voltage only requires the computation of a limited number of derivatives (of order 10), each obtainable from a single device simulation. Even using derivatives obtained from TCAD, the computational cost of the procedure is extremely reduced with respect to a statistical simulation. The price to pay is the initial analysis of variability sources and the consequent assumptions.

III. ANALYTICAL MODEL

The analytical model for the threshold voltage of ultrathin body SOI and double gate MOSFET is obtained from a simple derivation of surface potential profile $\phi_s(y)$ at the interface between the silicon body and the gate dielectric. We devise a simple extension of Liu's approach [12] along the lines proposed in [13]. Let us consider, for example, Fig. 3, in which an ultrathin body SOI MOSFET is considered. We assume that the channel can be divided in three regions: the central undoped region under the gate, and two external highly doped source and drain regions where the influence of the gate voltage is negligible. In the external regions ($y < 0$ and $y > L$) we assume complete depletion, and therefore a parabolic potential profile given by

$$\frac{d^2\phi_s}{dy^2} = -\frac{qN_D}{\varepsilon_{Si}}, \tag{6}$$

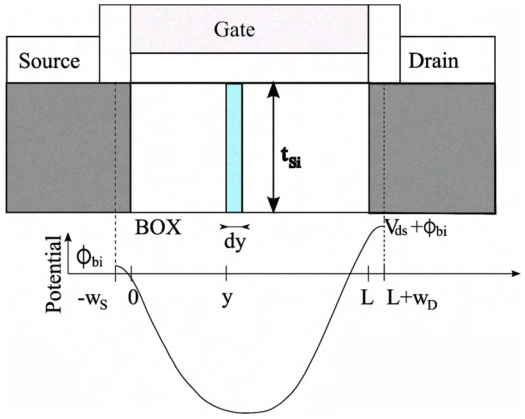

Figure 3: Illustration of the method derived from [12] to obtain an analytical expression of the surface potential profile.

where q is the electron charge, N_D the average doping in the source and drain regions, and ε_{Si} is silicon dielectric permittivity. In the central region $(0 < y < L)$ we use Gauss' theorem to write that the electric field flux through the surface of a slice of thickness dy (shown in Fig. 3) is zero [11, 12]. This allows us to write

$$\frac{d^2\phi_S(y)}{dy^2} - \frac{\eta}{\varepsilon_{Si}t_{Si}}\frac{\varepsilon_{ox}}{t_{ox}}\phi_S(y) = \frac{\eta}{\varepsilon_{Si}t_{Si}}\frac{\varepsilon_{ox}}{t_{ox}}(V_{FB} - V_{GS}), \quad (7)$$

where ε_{ox} is the oxide electric permittivity, V_{FB} is the flatband voltage, V_{GS} is the gate-to-source voltage, and η is a fitting parameter that takes into account the fact that the electric field is not constant along x and that is not zero in the BOX. Solving (7) we have

$$\phi_S(y) = \phi_P + C\frac{\sinh(y/\lambda)}{\sinh(L/\lambda)} + D\frac{\sinh[(L-y)/\lambda]}{\sinh(L/\lambda)}, \quad (8)$$

where $\phi_P = V_{GS} - V_{FB}$, $\lambda = \sqrt{\varepsilon_{Si}t_{Si}t_{ox}/\eta\varepsilon_{ox}}$. Unknown terms w_S, w_D, C, D are obtained by enforcing continuity of ϕ_S and its derivative and by the boundary conditions:

$$\begin{cases} \phi_S(-w_S) = \phi_{bi} \\ \dfrac{d\phi_s}{dy}(-w_S) = 0 \end{cases}; \begin{cases} \phi_S(L+w_D) = V_{DS} + \phi_{bi} \\ \dfrac{d\phi_S}{dy}(L+w_D) = 0 \end{cases} \quad (9)$$

Once $\phi_S(y)$ is known we can extract its minimum value in the channel $\phi_{SMIN}(V_{GS}, V_{DS})$ and obtain the threshold voltage as the gate voltage required to have $\phi_{SMIN} = \phi^*$, corresponding to the drain current used in the definition of V_{th}.

IV. Results

First, we want validate our analytical model for the surface potential and the threshold voltage by comparison with TCAD results [14] on the template devices with the full doping profiles. In Fig. 4 the surface potential profiles for the 32 nm template MOSFET are compared for $V_{DS} = 50$ mV and 1 V, and for different values of V_{GS}. We use a single fitting parameter ($\eta = 1.2$) with the same value for the 32 nm and the 22 nm templates at the price of a suboptimal fitting. Nevertheless, agreement is very good. Also the comparison of the threshold voltage profiles in Fig. 5 is very good (V_{th} is defined as the V_{GS} corresponding the current of 10^{-5} $A/\mu m$ as in [8]). Very good agreement is obtained also for the 22 nm template MOSFET (Figs. 6-7).

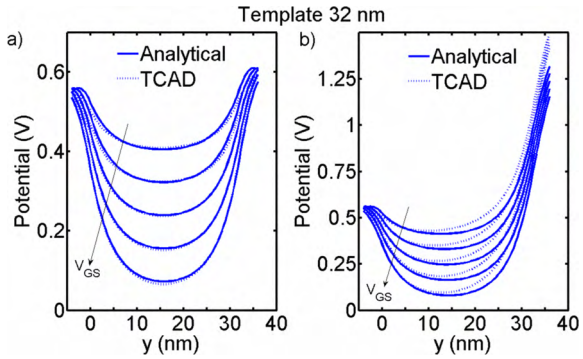

Figure 4: Surface potential profile of the 32 nm template MOSFET as a function of y for different V_{GS} (0-0.5 V in steps of 0.1 V) for $V_{DS} = 50$ mV (a) or $V_{DS} = 1$ V (b).

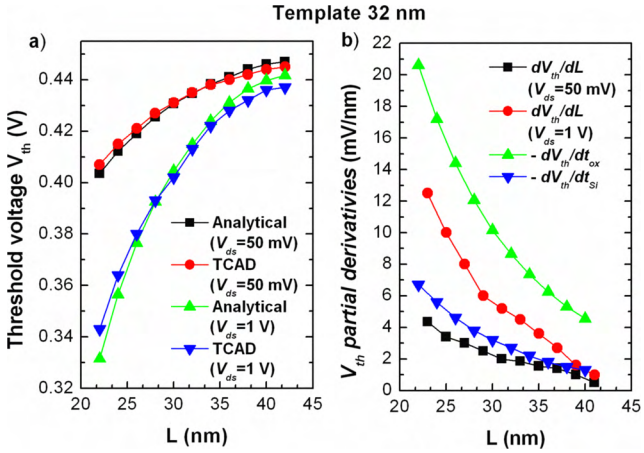

Figure 5: Threshold voltage as a function of L from analytical model and TCAD (a) and analytical partial derivatives of V_{th} (b) of the 32 nm template MOSFET.

Finally, we use our approach described in Section II to compute the variance of V_{th} due to LER and to SR, and to compare our results with those obtained with atomistic statistical simulations in [8]. As in [8], we assume for all interfaces a roughness with exponential autocorrelation function with mean square amplitude $\Delta_S = 0.15$ nm, correlation length $\Lambda_S = 1.8$ nm. For the LER, we assume an exponential autocorrelation function with $\Delta_L = 1.3$ nm, $\Lambda_L = 25$ nm.

Results are shown in Table I. The columns *An.An* and *An.TCAD* indicate results from our analytical approach described in Section II where the partial derivatives of V_{th} are computed analytically or with TCAD, respectively. The column *Atom* indicates results reported in [8]. As can be seen

the agreement, for the LER data, is always extremely good. Very good agreement is obtained between columns *An.An* and *An.TCAD*, for the effect of SR, for which data from [8] are not available.

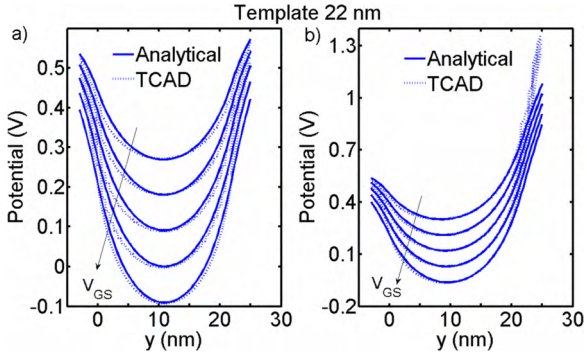

Figure 6: Surface potential profile of the 22 nm template MOSFET as a function of y for different V_{GS} (0-0.5 V in steps of 0.1 V) for $V_{DS} = 50$ mV (a) or $V_{DS} = 1$ V (b).

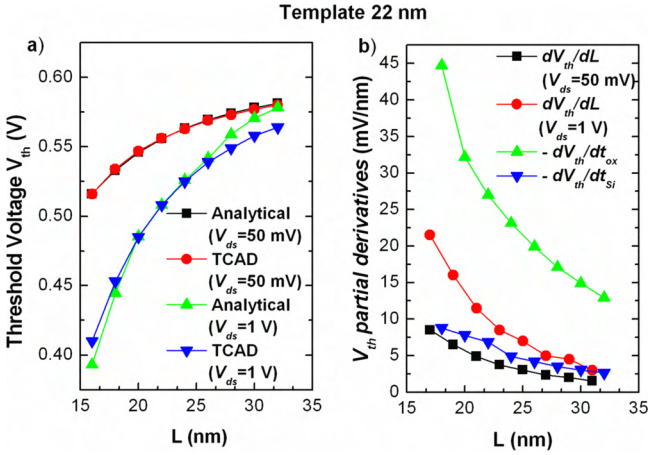

Figure 7: Threshold voltage as a function of L from analytical model and TCAD (a) and analytical partial derivatives of V_{th} (b) for the 22 nm template MOSFET.

V. CONCLUSION

We have proposed an analytical approach to the quantitative evaluation of the effect of line edge roughness and surface roughness that is based on the careful analysis of the main independent physical parameters affecting threshold voltage variability. The approach requires the calculation of partial derivatives of V_{th} with respect to device structure parameters that can be obtained with an analytical model or with a very limited number of TCAD simulations. We have shown that in both ways we are able to obtain results in very good agreement with 3D atomistic statistical simulations [8].

We believe that our approach has multiple advantages over statistical modeling, obviously in terms of computational requirements (by several orders of magnitude), but also in terms of providing a good framework for understanding the physical relevant effects affecting device variability and in the possibility of providing a quick way to evaluate V_{th} variability of candidate devices.

The main advantages of statistical simulation, on the other hand, are that it does not require preliminary device analysis and assumptions, and that it would work even when the linear approximation does not hold, for example in the presence of very large and critical variability.

Table I: Standard deviation of the threshold voltage due to LER and SR for the 32 nm and 22 nm template MOSFETs obtained with different method.

	Vds = 50 mV	**Approach**		
		An.An	***An.TCAD***	***Atom[8]***
32 nm	σ_{Vth} LER (mV)	*2.96*	*3*	*3.3*
	σ_{Vth} SR (mV)	*0.23*	*0.25*	*N/A*
22 nm	σ_{Vth} LER (mV)	*6*	*5.6*	*5.8*
	σ_{Vth} SR (mV)	*1.4*	*1.4*	*N/A*
	Vds = 1V	***Approach***		
		An.An	***An.TCAD***	***Atom[8]***
32 nm	σ_{Vth}LER (mV)	*7.9*	*8.3*	*8.6*
	σ_{Vth}SR (mV)	*0.66*	*0.6*	*N/A*
22 nm	σ_{Vth}LER (mV)	*14*	*13.6*	*13*
	σ_{Vth} SR (mV)	*4.3*	*4.4*	*N/A*

REFERENCES

[1] Kuhn, Kelin J., "Reducing Variation in Advanced Logic Technologies: Approaches to Process and Design for Manufacturability of Nanoscale CMOS" *IEEE International Electon Devices Meeting, IEDM 2007,* pp. 471-474.

[2] X. Tang , V. De, and J. D. Meindl, "Intrinsic MOSFET parameter fluctuations due to random dopant placement" *IEEE Trans. VLSI Syst.,* Vol. 5, pp. 369-376, 1997.

[3] P. A. Stolk, F. P. Widdershoven, and D. B. M. Klaassen, "Modeling Statistical Dopant Fluctuations in MOS Transistors", *IEEE Trans. Electron Devices*, Vol. 45 (9), pp.1960-1971, 1998.

[4] C. H. Diaz, H.-J. Tao, Y.-C. Ku, A. Yen, and K. Young, "An experimentally validated analytical model for gate line edge roughness (LER) effects on technology scaling." *IEEE Electron Device Letters*, Vol. 22, pp. 287–289, 2001.

[5] H.-S. Wong, Y. Taur, "Three-dimensional "atomistic" simulation of discrete random dopant distribution effects in sub-0.1 mm MOSFETs", *Tech. Dig. IEDM 1993*, pp. 705-708.

[6] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 mm MOSFET's: A 3-D "atomistic simulation study", *IEEE Trans. Electron Devices*, vol. 45, pp. 2505, 1998.

[7] A. Asenov, S. Kaya, J. Davies, "Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations", *IEEE Trans. Electron Devices*, vol. 49 (1), pp. 112-119.

[8] B. Cheng, S. Roy, A. Brown. C. Millar, A. Asenov, "Evaluation of intrinsic parameter fluctuations on 45, 32, and 22 technology node LP N-MOSFETs", *ESSDERC 2008*, pp. 47-50.

[9] E. Amirante, G. Iannaccone, B. Pellegrini "Three-dimensional statistical modeling of the effects of the random distribution of dopants in deep submicron nMOSFETs", *VLSI Design*, Vol. 13. pp. 425-429.

[10] G. Fiori, S. Di Pascoli, G. Iannaccone "Three-dimensional simulation of quantum confinement and random dopant effect in nanoscale nMOSFETs" *J. Computational and Theoretical Nanoscience*, Vol. 5, pp. 1115-1119, 2008.

[11] Pullnano Deliverable D4.5.1. www.pullnano.eu

[12] Z.-H. Liu et al."Threshold Voltage Model for Deep-Submicrometer MOSFET's" *IEEE Trans. Electron Devices*, vol. 40, pp.86-95, 1993.

[13] L. Perniola et al. "Analytical Model of the Effects of a Nonuniform Distribution of Stored Charge on the Electrical Characteristics of Discrete-Trap Nonvolatile Memories" *IEEE Trans. Nanotechnology*, vol. 4 (3), pp.360-368, 2005.

[14] Manual of TCAD Sentaurus (SYNOPSYS), Version 12.2007.