A picopower temperature-compensated, subthreshold CMOS voltage reference

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ABSTRACT

A voltage reference consisting of only two nMOS transistors with different threshold voltages is presented. Measurements performed on 23 samples from a single batch show a mean reference voltage of 275.4 mV. The subthreshold conduction and the low number of transistors enable to achieve a mean power consumption of only 40 pW. The minimum supply voltage is 0.45 V, which coincides with the lowest value reported so far. The mean TC in the temperature range from 0 to 120 °C is 105.4 ppm/°C, while the mean line sensitivity is 0.46%/V in the supply voltage range 0.45–1.8 V. The occupied area is 0.018 mm2. The power supply rejection rate without any filtering capacitor is −48 dB at 20 Hz and −29.2 dB at 10 kHz. Thanks to large area transistors and to a careful layout, the coefficient of variation of the reference voltage is only 0.62%. We introduce as a new figure of merit, the voltage temperature parameter (VTP), which gives a direct measure of the overall percentage variation of the reference voltage on the typical 2D domain of supply voltage and temperature. For the proposed circuit, the average VTP is 1.70% with a standard deviation of 0.21%. In order to investigate the effect of transistor area on process variability, a 4X replica of the proposed configuration has been fabricated and tested as well. Except for LS, the 4X replica doesn’t exhibit any appreciable improvement with respect to the basic voltage reference. Copyright © 2013 John Wiley & Sons, Ltd.

1. INTRODUCTION

As a consequence of the explosion of applications that require low power consumption, subthreshold circuits have gained much interest in the design community. Radio-frequency identification (RFID), implantable medical devices, micro-sensor networks, microcontroller unit and digital signal processor of portable devices are typical examples of applications that benefit from low energy operation [1].

In these devices, the requirement for small size and weight imposes the use of small batteries which provide a small amount of energy for the different building blocks. At the same time, many portable applications impose also the requirement of long lifetime such as in the case of passive RFIDs and implantable medical devices. Therefore, the energy and size requirements can be simultaneously guaranteed only by using circuits that operate at low supply voltage and with low power consumption.

Voltage references are used in all analog, digital and mixed-signal systems to generate a constant output voltage irrespective of temperature, process and supply voltage variations. There are several
approaches to design a voltage reference. The most common solution consists in the bandgap voltage reference (BGR) implemented in bipolar technology [2]. Nevertheless, in order to ensure a major compatibility with the rest of the system, several works have implemented the operating principle of the classical BGR in CMOS process by exploiting the parasitic vertical bipolar junction transistors [3–8]. However, all these solutions exhibit power consumption and a minimum supply voltage that are both too large for the typical low-power applications.

Alternative approaches employ MOSFETs working in strong inversion regime [9, 10], part in strong inversion and subthreshold regime [11–14] or all in subthreshold regime [15–18]. Some of them use MOSFETs with same threshold voltage [10, 11, 13–16], while in other cases MOSFETs with two different threshold voltages are employed [9,12,17, 18].

Among the different approaches, subthreshold design represents the most promising solution for extreme low-power, low-voltage applications. Subthreshold operation results in a minimum supply voltage of 0.45 V [17] and in a power consumption in picowatts order of magnitude [18].

Despite the significant advantages in terms of minimum supply voltage and power consumption, subthreshold operation poses several design issues. Of the utmost importance is the high process sensitivity due to the exponential relationship between the drain current and the threshold voltage, which is the most important process-dependent parameter.

Among the solutions proposed so far, the design reported in [18] represents a significant breakthrough in voltage reference design since it allows, for the first time, a power consumption in the order of picowatts.

In this work, we report an alternative configuration to that presented in [18]. Our solution, implemented in UMC 0.18 μm triple-well CMOS process, uses a different connection for the low-threshold voltage transistor. In addition, to improve the within die process variability, large area transistors have been used. Measurements performed on 23 samples of a single batch show a coefficient of dispersion for the reference voltage of only 0.62%. The mean power consumption at room temperature is 40 pW while the minimum supply voltage is 0.45 V which is coincident with the lowest value reported so far [17]. In order to investigate the effect of transistors’ areas on process variability, the basic circuit and its 4X replica have been compared.

The rest of this paper is organized as follows: Sections 2 and 3 report the operating principle and the main design considerations of the proposed solution. In Section 4, the measurement results and the comparison with the existing literature are reported. The main conclusions are summarized in Section 5.

2. OPERATING PRINCIPLE

The schematic of the proposed configuration is reported in Figure 1. The circuit consists of only two nMOS transistors, a high-threshold-voltage transistor $M_H$ ($V_{TH} = 600$ mV) and a low-threshold-voltage $M_L$.

![Figure 1. Schematic of the proposed temperature-compensated subthreshold CMOS voltage reference.](image)
transistor ML ($V_{TH} = 320$ mV). The configuration is similar to [18], but in our solution the body and the gate contacts of ML are both shorted with source.

As a consequence in the proposed solution, the body effect is compensated on both transistors instead on the load transistor only as in the case of [18].

The $I-V$ relationship for an nMOS transistor working in subthreshold regime is expressed as:

$$I_{sub} = \beta \frac{W}{L} V_T^2 \exp \left( \frac{V_{GS} - V_{TH}}{nV_T} \right) \left[ 1 - \exp \left( -\frac{V_{DS}}{V_T} \right) \right].$$

(1)

In (1), $\beta = \mu_n C_{ox}$ represents the subthreshold current factor, $C_{ox}$ is the oxide capacitance per unit area, $\mu_n$ is the electron mobility, $W$ and $L$ are the channel width and length, respectively, $V_T$ is the thermal voltage, $V_{GS}$ the gate-source voltage, $V_{TH}$ the threshold voltage, $V_{DS}$ the drain-source voltage and $n$ the subthreshold swing factor. If $V_{DS}$ exceeds the value of $4V_T$, the term in square bracket in (1) can be neglected. In this case, the following equations could be used to compute the drain current and the gate-source voltage:

$$I_{sub} = \beta \frac{W}{L} V_T^2 \exp \left( \frac{V_{GS} - V_{TH}}{nV_T} \right),$$

(2)

$$V_{GS} = V_{TH} + nV_T \ln \left( \frac{I_{sub}}{\beta \frac{W}{L} V_T^2} \right).$$

(3)

From (2), the current injected by ML into MH is expressed as

$$I_L = \beta_L \left( \frac{W}{L} \right)_L V_T^2 \exp \left( -\frac{V_{TH,L}}{n_L V_T} \right),$$

(4)

while from (3), the reference voltage, which is coincident with the gate-source voltage of MH, is expressed as

$$V_{REF} = V_{TH,H} + n_H V_T \ln \left( \frac{I_H}{\beta_H \left( \frac{W}{L} \right)_H V_T^2} \right).$$

(5)

Since $I_H = I_L$, we obtain the $V_{REF}$ expression by substituting (4) into (5):

$$V_{REF} = V_{TH,H} - \frac{n_H}{n_L} V_{TH,L} + n_H V_T \ln \left( \frac{C_{ox,L} \left( \frac{W}{L} \right)_L}{C_{ox,H} \left( \frac{W}{L} \right)_H} \right).$$

(6)

By considering as a first approximation the subthreshold swing factors almost constant with temperature, the only temperature-dependent parameters in (6) are the two threshold voltages and the thermal voltage. Since the threshold voltage decreases with temperature and the thermal voltage increases with temperature, a compensation of these two terms can be performed by choosing a proper transistor size ratio. To find it, we have to introduce the temperature dependence of the threshold voltage [19]:

$$V_{TH}(T) = V_{TH}(T_0) + \kappa(T - T_0).$$

(7)
In (7), $V_{TH}(T_0)$ represents the threshold voltage at room temperature $T_0$, while $\kappa < 0$ represents the temperature coefficient for the threshold voltage. Therefore, imposing (7) to $V_{TH,H}$ and $V_{TH,L}$ and expressing the thermal voltage as $kT/q$ (with $k$ Boltzmann’s constant and $q$ elementary charge), we can rewrite (6) in the following form:

$$V_{REF} = V_{TH,H}(T_0) - |\kappa_H|(T - T_0) - \frac{n_H}{n_L}(V_{TH,L}(T_0) - |\kappa_L|(T - T_0)) \quad (8)$$

$$+ n_H \frac{kT}{q} \ln \left( \frac{C_{ox,L}}{C_{ox,H}} \left( \frac{W}{L} \right)_R \right),$$

where $(W/L)_R = (W/L)_L/(W/L)_H$. The temperature variation of $V_{REF}$ is then obtained by differentiating (8) with respect to temperature:

$$\frac{\partial}{\partial T} V_{REF} = -|\kappa_H| + \frac{n_H}{n_L} |\kappa_L| + n_H \frac{k}{q} \ln \left( \frac{C_{ox,L}}{C_{ox,H}} \left( \frac{W}{L} \right)_R \right). \quad (9)$$

To obtain the condition of temperature-compensated voltage reference, we choose the transistor size ratio which sets (9) to 0:

$$\frac{(W/L)_L}{(W/L)_H} = C_{ox,H} C_{ox,L} \exp \left[ \frac{q}{n_H k} \left( |\kappa_H| - \frac{n_H}{n_L} |\kappa_L| \right) \right]. \quad (10)$$

The temperature-compensated reference voltage is then evaluated by substituting (10) into (8):

$$V_{REF} = V_{TH,H}(T_0) + |\kappa_H| T_0 - \frac{n_H}{n_L} (V_{TH,L}(T_0) + |\kappa_L| T_0). \quad (11)$$

A more simplified expression of $V_{REF}$ is obtained by considering $n_H \approx n_L$ and $\kappa_H \approx \kappa_L$. Under these assumptions

$$V_{REF} \approx \Delta V_{TH} = V_{TH,H}(T_0) - V_{TH,L}(T_0). \quad (12)$$

From (12), the reference voltage of the proposed configuration is approximated by the difference between the two threshold voltages, in contrast with the result obtained in [18] where a voltage reference equal to $\sim 0.75 \Delta V_{TH}$ is obtained. Despite its simplicity, expression (12) gives a very accurate estimation of the reference voltage as confirmed by measurement results. The error between the measured mean value of $V_{REF}$ and the value predicted from (12) by using the nominal values of $V_{TH,H}$ and $V_{TH,L}$ is only $1.67\%$.

3. DESIGN CONSIDERATIONS

3.1. Subthreshold conduction and threshold voltages constraint

In the proposed configuration, the low-threshold voltage transistor has the gate, the source and the body terminals shorted. As a consequence, the subthreshold conduction for this transistor is ensured if its threshold voltage is higher than 0 V at the maximum operating temperature:

$$V_{TH,L}(T_0) > |\kappa_L|(T_{max} - T_0). \quad (13)$$
On the other hand, the reference voltage is coincident with the gate-source voltage of a diode-connected, high-threshold-voltage transistor. To ensure subthreshold conduction, the output voltage has to be lower than the threshold voltage. This condition is clearly always satisfied. However, in the proposed operating principle, we have also assumed $V_{REF} > 4V_T$ in order to neglect, without significant loss of accuracy, the effect of $V_{DS}$ on drain current. The value of $V_{TH,H}(T_0)$ which ensures the condition $V_{REF} > 4V_T$ for all operating temperature is obtained by (11) and (13):

$$V_{TH,H}(T_0) > \frac{4kT_{max}}{q} + \frac{n_H}{n_L}\kappa_L T_{max} - |\kappa_H|T_0. \quad (14)$$

### 3.2. Minimum supply voltage

In our solution, as in [17] and [18], the supply voltage $V_{DD}$ can be expressed as the sum of transistor drain-source voltages:

$$V_{DD} = V_{REF} + V_{DS,L}. \quad (15)$$

As reported in Section 2, the current injected by $M_L$ into $M_H$ becomes almost independent of the drain voltage for $V_{DS,L} > 4V_{T,max}$. As a consequence, we can express the minimum supply voltage as:

$$V_{DD,\text{min}} > V_{REF} + 4V_{T,\text{max}}. \quad (16)$$

Since in our design we choose a maximum operating temperature of 120°C, the expected minimum supply voltage is about 135.5 mV larger than the reference voltage. By using (15), we can also evaluate the lowest value of $V_{DD}$ for the proposed solution to be $\sim 8V_{T,\text{max}}$, since we have to ensure the condition of $V_{REF} > 4V_{T,\text{max}}$.

### 3.3. Supply voltage variations

$V_{DS}$ can affect the drain current also because of drain-induced barrier lowering (DIBL). As a result, the current injected by $M_L$ into $M_H$ depends on $V_{DD}$ also if $V_{DS,L}$ is greater than $4V_T$. Neglecting DIBL effect on the load transistor, the variation $\Delta V_{REF}$ on reference voltage caused by a variation $\Delta V_{DD}$ on supply voltage is evaluated by considering the DIBL effect on $V_{TH,L}$:

$$\Delta V_{TH,L} = \lambda_D \Delta V_{DS,L}. \quad (17)$$

In (17), $\lambda_D$ is the DIBL coefficient of the low-threshold voltage transistor and $\Delta V_{DS,L}$ the variation of the drain-source voltage of $M_L$ which is equal to $\Delta V_{DS,L} = \Delta V_{DD} - \Delta V_{REF}$. From (11) and (17), a variation $\Delta V_{TH,L}$ causes a variation on reference voltage equal to

$$\Delta V_{REF} = \frac{n_H}{n_L} \Delta V_{TH,L}(T_0) = \frac{n_H}{n_L} \frac{\lambda_D}{1 + \frac{2n_H}{n_L} \lambda_D} \Delta V_{DD}, \quad (18)$$

which leads to a line sensitivity (LS), expressed as $\%$/V, equal to

$$LS[\%/V] = 100 \frac{n_H}{n_L} \frac{\lambda_D}{V_{REF} \left(1 + \frac{2n_H}{n_L} \lambda_D\right)}. \quad (19)$$
For LS minimization, the $M_{L}$ transistor must be as long as possible since the DIBL increases exponentially as the channel length decreases [20].

3.4. Voltage temperature parameter

The two fundamental figures of merit of a voltage reference are LS and TC. There are two drawbacks in the use of these two parameters. The first drawback is that although LS (TC) depends on the temperature (supply voltage), LS (TC) is typically evaluated at a single temperature (supply voltage), thus giving only a very limited information on the overall variations of the reference voltage with supply voltage and temperature. The second drawback is that the reference voltage does not depend linearly on supply voltage and temperature; therefore, the values of LS and TC measured in a given range do not allow to evaluate the LS and TC in a smaller or larger range. As an example, the voltage reference typically exhibits a higher sensitivity to the supply voltage close to the minimum voltage and a lower sensitivity at higher voltages; therefore, an apparently better LS can be simply obtained by increasing the maximum supply voltage under consideration. In order to overcome these drawbacks, we introduce as a new figure of merit the voltage temperature parameter (VTP), defined as

$$VTP[\%] = 100 \frac{V_{REF,\max} - V_{REF,\min}}{V_{REF,\text{mean}}} \tag{20}$$

where $V_{REF,\max}$, $V_{REF,\min}$ and $V_{REF,\text{mean}}$ are the maximum, the minimum and the mean value of the reference voltage in a given 2D voltage–temperature domain. In order to compare VTP obtained in the cases of different voltage references, we propose to use a voltage range of 1 V and a temperature range of 100°C.

In this work, we consider the 2D domain obtained by varying the supply voltage in the range $[V_{DD,\min} - V_{DD,\min} + 1\text{ V}]$ and the temperature range from 0 to 100°C. Note that VTP gives a direct measure of the overall percentage variation of the reference voltage on the typical 2D domain of operating supply voltage and temperature.

3.5. Process variations

Process variations are particularly important in subthreshold analog design as a consequence of the exponential sensitivity of the drain current to the threshold voltage variations induced by the random dopant fluctuations and oxide thickness variation. A common and simple way to estimate the effect of the process variations is proposed in [21] where the standard deviation of the threshold voltage of a pair of MOS transistors is evaluated as

$$\sigma_{V_{TH}} = \frac{A}{\sqrt{W_{\text{eff}}L_{\text{eff}}}} \tag{21}$$

where $A$ is a technology-dependent coefficient, while $W_{\text{eff}}$ and $L_{\text{eff}}$ are the effective channel width and length, respectively. In the proposed voltage reference, $V_{REF}$ is approximated by the difference between the two threshold voltages. For this reason, according to [21], to obtain a good process stability, a large area for both transistors is necessary. However, it is worth to note that (21) takes in account only the process mismatches induced by random variations but neglects the effect of the systematic mismatches such as temperature and stress. A compensation of these effects is obtained by using accurate layout techniques [22].

3.6. Transistor size

The transistor sizing for the proposed configuration has been performed by taking into account three constraints: LS, TC and process stability.
As reported in the previous sections: (1) LS decreases as the channel length of ML is increased; (2) the effect of process variability decreases by increasing the area of both transistors; (3) the reference voltage is temperature compensated by choosing a proper transistor size ratio.

For the chosen design kit, the maximum W and L are 100μm and 50μm, respectively. As a consequence, we impose a value of 50μm for L_L in order to ensure the minimum value of LS and, for the maximum process stability, a value of 50μm for L_H and 100μm for W_L. Since the temperature coefficient of the proposed solution depends only on transistor size ratio, we can obtain a temperature-compensated voltage by performing a proper dimensioning for W_H.

In Figure 2, we report the simulated TC as a function of transistor size ratio. The simulation is performed by keeping L_L = L_H = 50μm and W_L = 100μm and by varying W_H. The simulated optimal value is 1.85 (W_H = 54μm) very close to the predicted optimal transistor size ratio of 1.67 (W_H = 60μm).

3.7. Process stability improvement

Since robustness to process variability improves as the transistor area increases [21], we can gain further advantage by replicating the basic configuration an appropriate amount of times. The number of replicas is evaluated in order to find a proper trade-off among occupied area, power consumption and improvement in process variability. For a proper choice we first evaluate the theoretical improvement provided by a generic N X replica. From (12), the standard deviation of VREF is expressed as:

$$\sigma_{V_{REF}} = \sqrt{\sigma_{V_{TH,H}}^2 + \sigma_{V_{TH,L}}^2 - 2\rho \sigma_{V_{TH,L}} \sigma_{V_{TH,H}}}$$

(22)

where $\sigma_{V_{REF}}, \sigma_{V_{TH,H}}$ and $\sigma_{V_{TH,L}}$ are the standard deviations for $V_{REF}, V_{TH,H}$ and $V_{TH,L}$, respectively, while $\rho$ represents the correlation factor between $\sigma_{V_{TH,H}}$ and $\sigma_{V_{TH,L}}$. From (21) and (22), assuming $\rho$=0, an N times replicated version of our circuits decreases the standard deviation of the reference voltage by a factor equal to $\sqrt{N}$ which means that the most significant improvement in process stability is obtained with a low number of replicas. In our design, we choose $N$=4 since the improvement in process stability given by a larger number of replicas is not commensurate to the penalty in occupation area and power consumption. To investigate experimentally the effect of the transistor area on process variability, the basic and the 4X replicated version, with a common centroid layout, have been fabricated and tested as well.

Figure 2. Simulated optimal TC as a function of transistor size ratio obtained by keeping L_L = 50 μm, W_L = 100μm, L_H = 50 μm and by varying W_H. The simulated optimal transistor size ratio is equal to 1.85 instead of 1.67 predicted by (10).
4. EXPERIMENTAL RESULTS

The layout and the transistor sizes of the proposed voltage reference and its 4X replica are reported in Figure 3 and Table I, respectively. The active area is only 0.018 mm² for the basic voltage reference while an area of 0.056 mm² is necessary for its 4X replica. The on-wafer electrical measurements have been performed on 23 samples containing the basic voltage reference and its 4X replica by using a probe station SUMMIT 11861B Cascade with Temptronic thermal controller and a Keithley 4200-SCS parameter analyzer. Figures 4 and 5 report the performance of a typical proposed voltage reference, while in Figure 6, we report the distributions of its main figures of merit. In Figure 4(a), we report the reference voltage as a function of supply voltage for a typical chip. The circuit starts to work properly from $V_{DD}=0.45$ V, which is only 34 mV higher than the value predicted from (16) by considering a maximum operating temperature of 120 °C. The distribution of the measured reference voltage at 25 °C for $V_{DD}=0.45$ V, across the 23 dies, is reported in Figure 6(a). The mean reference voltage is 275.4 mV with a standard deviation of only 1.7 mV.

The measured mean value of $V_{REF}$ is only 4.6 mV lower than the value predicted by using (12), while the measured intra-die standard deviation is about four times greater than the value predicted by substituting in (22) the 3-sigma variation of $V_{TH,L}$ and $V_{TH,H}$ evaluated according to the matching report of our design kit.

Figure 4(b) shows the temperature dependence of $V_{REF}$ for a typical device. The reference voltage monotonously increases by decreasing the temperature and by increasing the supply voltage. The measured mean TC in the temperature range from 0 to 120 °C, averaged over the supply voltage range from 0.45 to 1.8 V, is 105.4 ppm/°C with a standard deviation of 18.2 ppm/°C (see Figure 6(b)). At 25 °C, the mean LS for $V_{DD}$ ranging from 0.45 to 1.8 V is 0.46%/V, which is only 0.03%/V higher than the value predicted by (19). The standard deviation in this specification is 0.15%/V (see Figure 6(c)). The dependence of the reference voltage on temperature and supply voltage, for a typical chip, can be simultaneously grasped by inspecting Figure 5. The average VTP evaluated in the supply voltage range from 0.45 to 1.45 V and in the temperature range from 0 to 100 °C is 1.70% with a standard deviation of 0.21% (see Figure 6(d)).

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Transistor</th>
<th>W/L</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic voltage reference</td>
<td>$M_L$</td>
<td>100 μm / 50 μm = (25 μm/50 μm) × 4</td>
</tr>
<tr>
<td></td>
<td>$M_H$</td>
<td>54 μm / 50 μm = (13.5 μm/50 μm) × 4</td>
</tr>
<tr>
<td>4X voltageReference</td>
<td>$M_L$</td>
<td>400 μm / 50 μm = (25 μm/50 μm) × 16</td>
</tr>
<tr>
<td></td>
<td>$M_H$</td>
<td>216 μm / 50 μm = (13.5 μm/50 μm) × 16</td>
</tr>
</tbody>
</table>
In Figure 4(c), we report the power consumption as a function of temperature and supply voltage. At room temperature, power consumption is 36.7 pW for $V_{DD} = 0.45$ V and 154 pW for $V_{DD} = 1.8$ V. At a maximum operating temperature of 120 °C, the power consumption is 2.9 nW for $V_{DD} = 0.45$ V and 12.2 nW for $V_{DD} = 1.8$ V. Across the 23 samples the mean power consumption at 25 °C and for $V_{DD} = 0.45$ V is 40 pW with a standard deviation of 3.3 pW (see Figure 6(e)).

Figure 4(d) reports the measured power supply rejection rate (PSRR) at room temperature for $V_{DD} = 0.45$ V. The PSRR without any filtering capacitor is 48 dB at 20 Hz and 29.2 dB at 10 kHz. All previous data are consistently obtained also for the 4X replica.

Table II compares the mean value and the dispersion of the main figures of merit for the basic voltage reference and its 4X replica. The only performance figure benefiting from the larger occupied area is the LS. The mean value of LS is 0.05%/V lower in the 4X version with respect to the basic version, and its standard deviation is three times smaller. The basic voltage reference is clearly more efficient in terms of power consumption, which is roughly four times smaller than in the case of the 4X replica. All the other parameters are practically coincident. In particular, we do not observe the improvement of the standard deviation of the reference voltage predicted by the $1/\sqrt{WL}$ law for the 4X version. We conclude that the transistor areas in the basic voltage reference are sufficiently large and that a further enlargement does not provide a significant improvement against process variability. In Table III, the basic voltage reference is compared with the other low-power, low-voltage CMOS voltage references reported in literature. In order to perform a fair comparison, we...
choose to report the results obtained in [18] before trimming and corresponding to a single batch with a similar number of dies. Except [18], our solution exhibits the lowest power consumption. The minimum supply voltage is equal to [17], which represents the best result proposed so far. The LS is similar to [17], while the temperature coefficient is comparable to [16] and [17]. Except [16] and [18], the proposed solution has the lowest occupied area. In the same Table III, we report also the comparison of the statistical analysis where data are available. The coefficient of variation of the reference voltage in a single batch is lower with respect to the other CMOS voltage references [12–18].

Table II. Comparison between the basic voltage reference and its 4X replica.

<table>
<thead>
<tr>
<th></th>
<th>Basic voltage reference</th>
<th>4X voltage reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD,,MIN}$ [V]</td>
<td>0.45</td>
<td>0.45</td>
</tr>
<tr>
<td>Area [mm$^2$]</td>
<td>0.018</td>
<td>0.056</td>
</tr>
<tr>
<td>$V_{REF}$ [mV]</td>
<td>$\mu=275.4$, $\sigma=1.7$</td>
<td>$\mu=275.0$, $\sigma=1.8$</td>
</tr>
<tr>
<td>$\mu=0.62%$</td>
<td>$\sigma=1.70$, $\mu=0.21$</td>
<td>$\sigma=1.71$, $\mu=0.22$</td>
</tr>
<tr>
<td>TVC[%]</td>
<td>$\sigma=12.3%$</td>
<td>$\sigma=12.9%$</td>
</tr>
<tr>
<td>$V_{TC}$ [ppm/°C]</td>
<td>$\sigma=105.4$, $\mu=18.2$</td>
<td>$\sigma=115.7$, $\mu=18.8$</td>
</tr>
<tr>
<td>$\sigma=17.3%$</td>
<td>$\sigma=0.46$, $\mu=0.15$</td>
<td>$\sigma=0.39$, $\mu=0.05$</td>
</tr>
<tr>
<td>$\mu=32.6%$</td>
<td>$\sigma=40$, $\mu=3.3$</td>
<td>$\sigma=40$, $\mu=6.9$</td>
</tr>
<tr>
<td>Power [pW]</td>
<td>$\sigma=8.3%$</td>
<td>$\sigma=4.9%$</td>
</tr>
<tr>
<td>$\sigma=1.7%$</td>
<td>$-48$ @ 20 Hz</td>
<td>$-48.4$ @ 20 Hz</td>
</tr>
<tr>
<td>$\sigma=0.15%$</td>
<td>$-29.2$ @ 10 kHz</td>
<td>$-23.7$ @ 10 kHz</td>
</tr>
</tbody>
</table>

Figure 6. Statistical analysis over 23 samples of the basic voltage reference: (a) reference voltage at 25 °C and $V_{DD}=0.45$ V, (b) TC, (c) LS at 25 °C, (d) VTP, (e) power consumption at 25 °C and $V_{DD}=0.45$ V (e).
### Table III. Comparison with low-voltage low-power CMOS voltage references.

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>0.18µm CMOS</td>
<td>0.13µm CMOS</td>
<td>0.18µm CMOS</td>
<td>0.18µm CMOS</td>
<td>0.18µm CMOS</td>
<td>0.35µm CMOS</td>
<td>0.35µm CMOS</td>
</tr>
<tr>
<td><strong>Supply voltage (V)</strong></td>
<td>0.45 to 1.8</td>
<td>0.5 to 3.0</td>
<td>0.45 to 2</td>
<td>0.6 to 2.3</td>
<td>0.85 to 2.5</td>
<td>0.9 to 4</td>
<td>1.1 to 4</td>
</tr>
<tr>
<td><strong>Power @ room</strong></td>
<td>40 pW@0.45 V</td>
<td>2.2 pW@0.5 V–</td>
<td>3.15 nW@0.45 V</td>
<td>&lt;40 nW@0.7 V</td>
<td>3.3 µW@0.85 V</td>
<td>36 nW@0.9 V</td>
<td>22 nW@1.1 V</td>
</tr>
<tr>
<td><strong>VREF (mV)</strong></td>
<td>0.18 nW@1.8 V</td>
<td>275.4</td>
<td>176.7</td>
<td>263.5</td>
<td>–</td>
<td>Average</td>
<td>220 nW@4 V</td>
</tr>
<tr>
<td><strong>TC (ppm/°C)</strong></td>
<td>105.4</td>
<td>62 (average)</td>
<td>142.1</td>
<td>127</td>
<td>194</td>
<td>10</td>
<td>11.4 [–20:80], vers-1</td>
</tr>
<tr>
<td><strong>T range(°C)</strong></td>
<td>[0:120]</td>
<td>[–20:80]</td>
<td>[0:100]</td>
<td>[–20:100]</td>
<td>[–20:120]</td>
<td>[0:80]</td>
<td>9.2 [–20:80], vers-2</td>
</tr>
<tr>
<td><strong>Line sensitivity (%)</strong></td>
<td>0.46</td>
<td>0.033</td>
<td>0.44</td>
<td>~2.73</td>
<td>0.905</td>
<td>0.27</td>
<td>0.09, vers-1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.17, vers-2</td>
</tr>
<tr>
<td><strong>PSRR (dB)</strong></td>
<td>VDD = 0.45 V</td>
<td>–</td>
<td>VDD = 0.45 V</td>
<td>–</td>
<td>–</td>
<td>VDD = 0.9 V</td>
<td>VDD = 3 V</td>
</tr>
<tr>
<td><strong>Low freq [≤100 Hz]</strong></td>
<td>–48</td>
<td>–53</td>
<td>–49.4</td>
<td>–41</td>
<td>–</td>
<td>–47</td>
<td>&lt;–60</td>
</tr>
<tr>
<td><strong>High freq [≥10MHz]</strong></td>
<td>–29.2@10kHz</td>
<td>–62</td>
<td>(–12.2 sim.)</td>
<td>–</td>
<td>–</td>
<td>–40</td>
<td>&lt;–40</td>
</tr>
<tr>
<td></td>
<td>VREF</td>
<td>0.62%</td>
<td>0.85%</td>
<td>3.9%</td>
<td>–</td>
<td>–</td>
<td>3.1%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.1% vers-1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.8% vers-2</td>
</tr>
<tr>
<td><strong>α/µ</strong> TC</td>
<td>17.3%</td>
<td>54.7%</td>
<td>60.6%</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td><strong>LS</strong></td>
<td>32.6%</td>
<td>–</td>
<td>13.1%</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>8.3%</td>
<td>–</td>
<td>26.9%</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td><strong>Die area (mm²)</strong></td>
<td>0.018</td>
<td>0.0135</td>
<td>0.043</td>
<td>0.004</td>
<td>0.0238</td>
<td>0.045</td>
<td>0.0189, vers-1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.0193, vers-2</td>
</tr>
</tbody>
</table>

*SUBTHRESHOLD CMOS VOLTAGE REFERENCE*
and even better than bipolar BGRs [5, 6]. The observed robustness against process variation is ascribed to the large transistor areas and to a careful layout. A complete comparison of the dispersion of the other parameters can be performed only with [17] since it is the only work in literature which reports this information ([18] gives information only on TC dispersion).

5. CONCLUSIONS

A temperature-compensated subthreshold CMOS voltage reference has been presented. The proposed solution, fabricated in UMC 0.18 μm triple-well CMOS technology, consists of only two nMOS transistors with different threshold voltages. A statistical experimental analysis of the proposed configuration has been performed over a set of 23 samples.

The mean reference value is 275.4 mV, which approximately corresponds to the difference between the two threshold voltages. The minimum supply voltage is 0.45 V, which coincides with the lowest value reported so far. The mean TC in the temperature range from 0 to 120 °C is 105.4 ppm/°C, while the mean LS is 0.46%/V in the supply voltage range from 0.45 to 1.8 V. The active area is 0.018 mm².

Thanks to the large area transistors and to a careful layout, the coefficient of variation of the reference voltage is only 0.62%. We have introduced as a new figure of merit, the VTP, which gives a direct measure of the overall percentage variation of the reference voltage on the typical 2D domain of operating supply voltage and temperature. For the proposed circuit, the mean VTP in the supply voltage range from 0.45 to 1.45 V and in the temperature range from 0 to 100 °C is equal to 1.70% with a standard deviation of 0.21%.

In order to investigate the effect of transistor area on robustness to process variability, a 4X replica of the proposed configuration has been fabricated and tested as well. The 4X replica exhibits an appreciable improvement only on the mean value and the standard deviation of LS at the cost of the obvious penalty in the area occupation and power consumption.

REFERENCES


