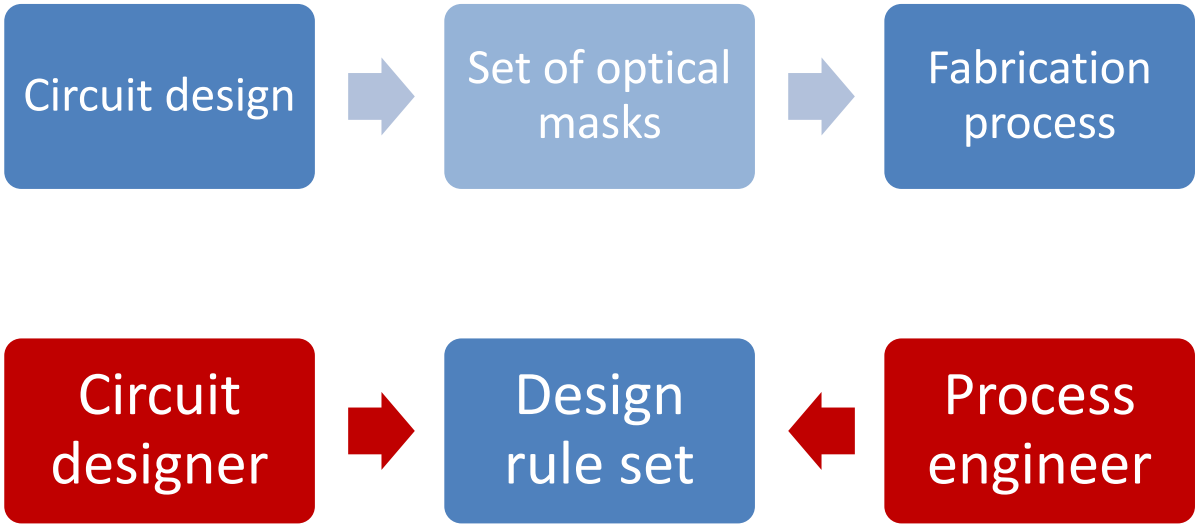
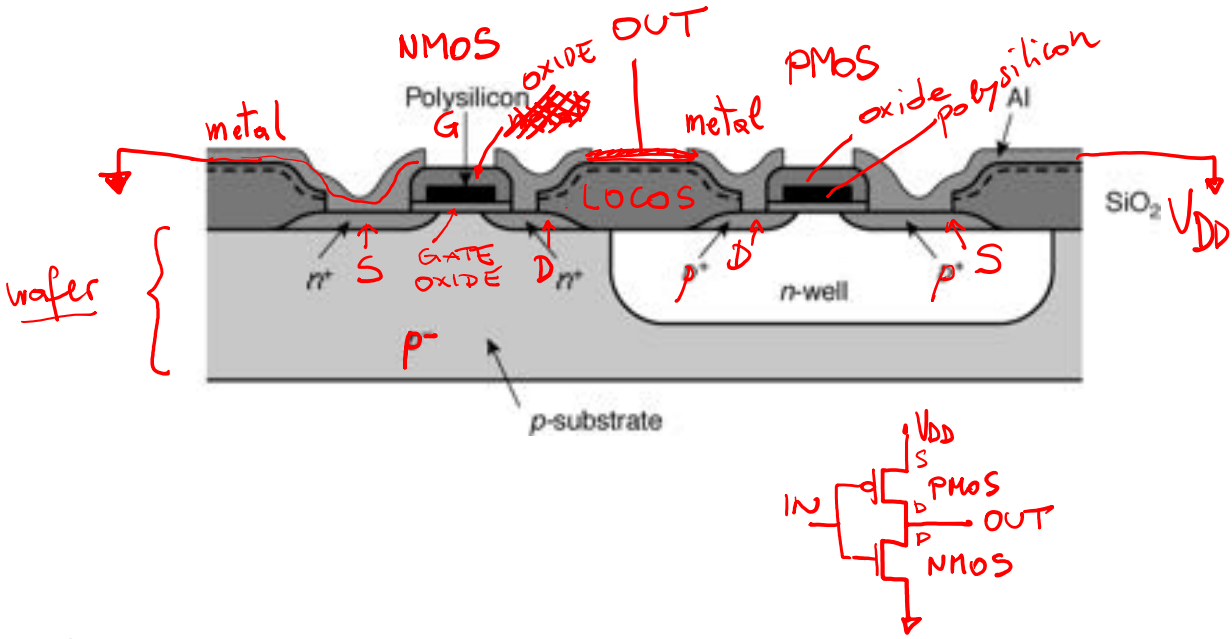
CMOS Manufacturing process



All material: Chapter 2 of J. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits, second edition, Prentice Halls, 2002

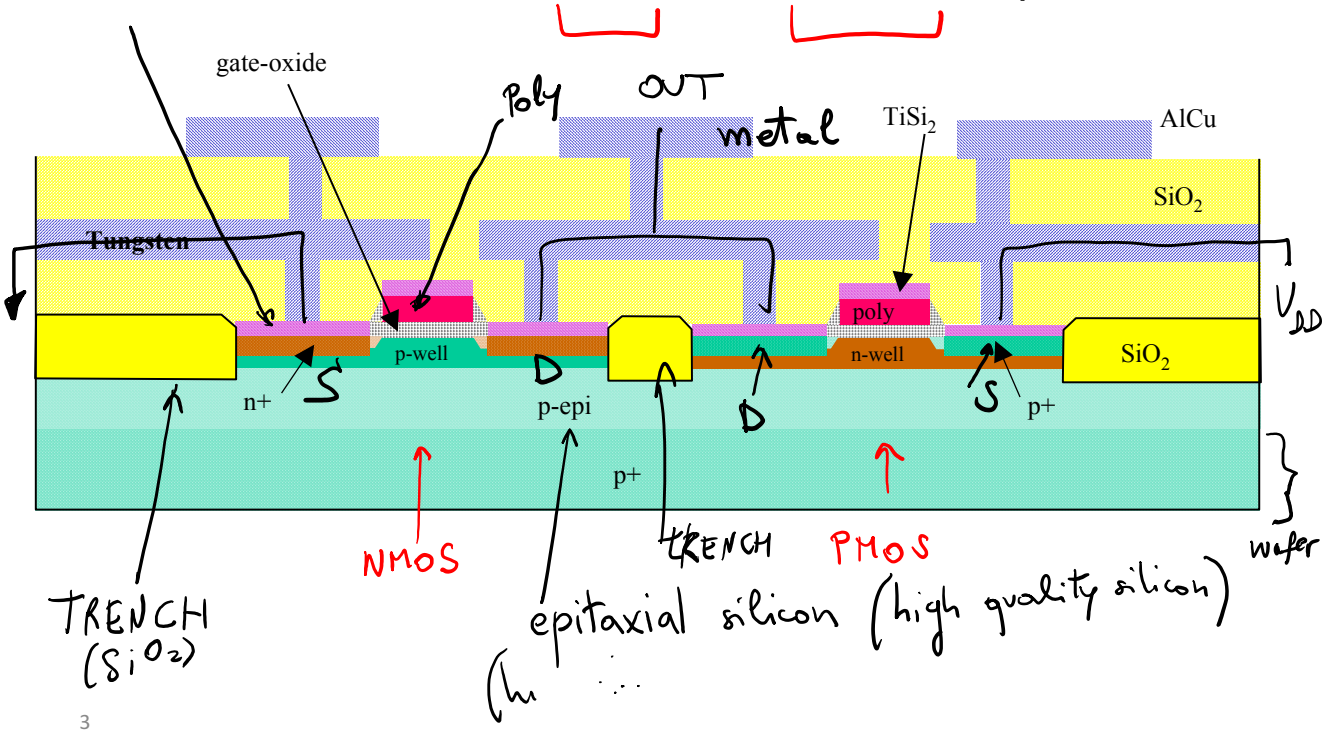
Simplified very basic CMOS Process

CMOS inverter – n-well process

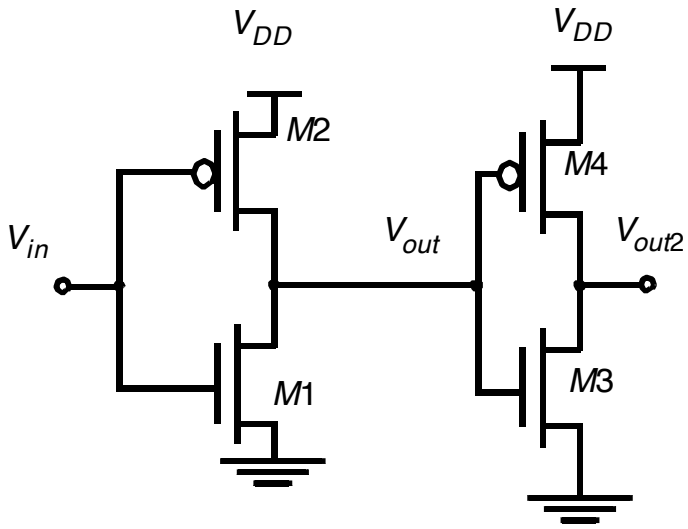


A Modern CMOS Process

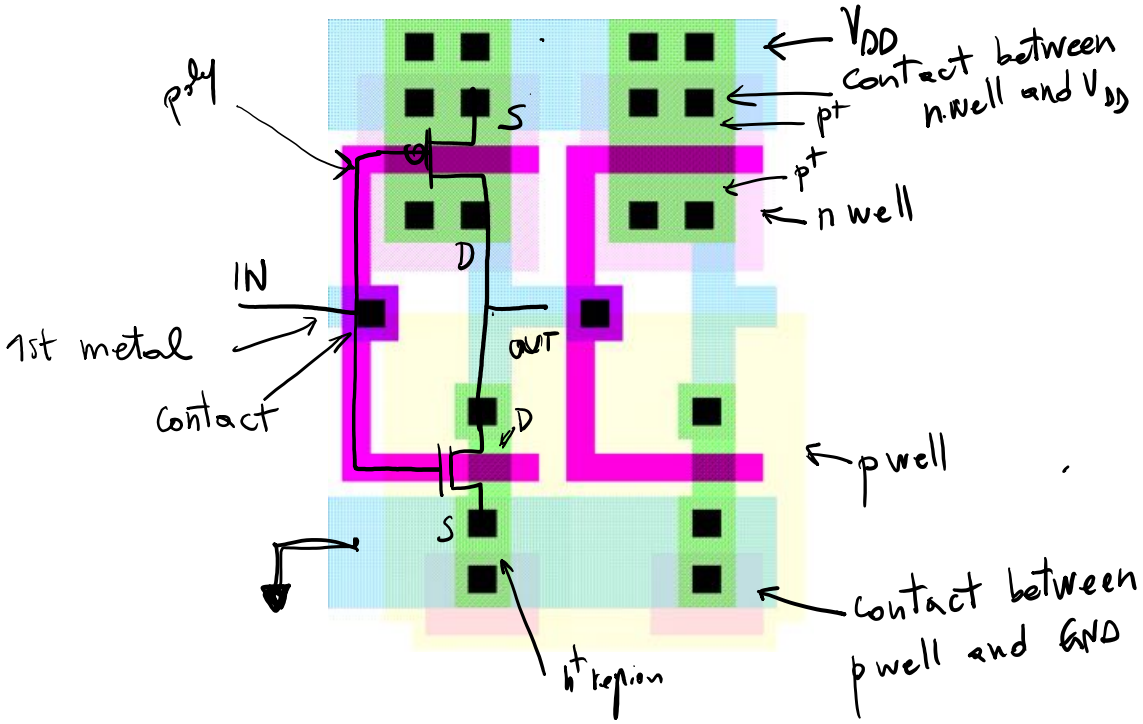
CMOS inverter – dual-well trench-isolated process



Two cascaded inverters



Two cascaded inverters - Layout View



Silicon ingot

Diameter
12 inches
(300 mm)

Weight
100 Kg

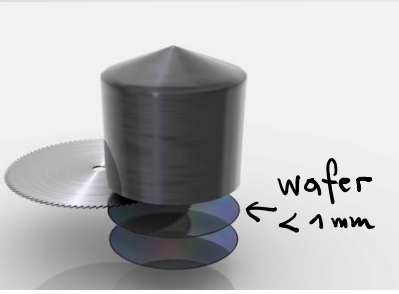
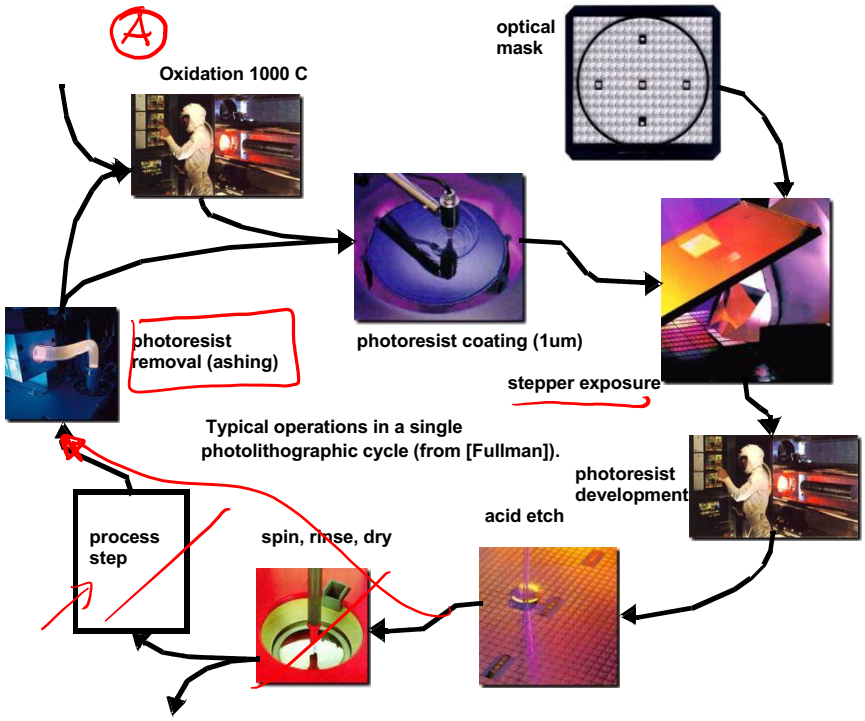


Photo-Lithographic Process

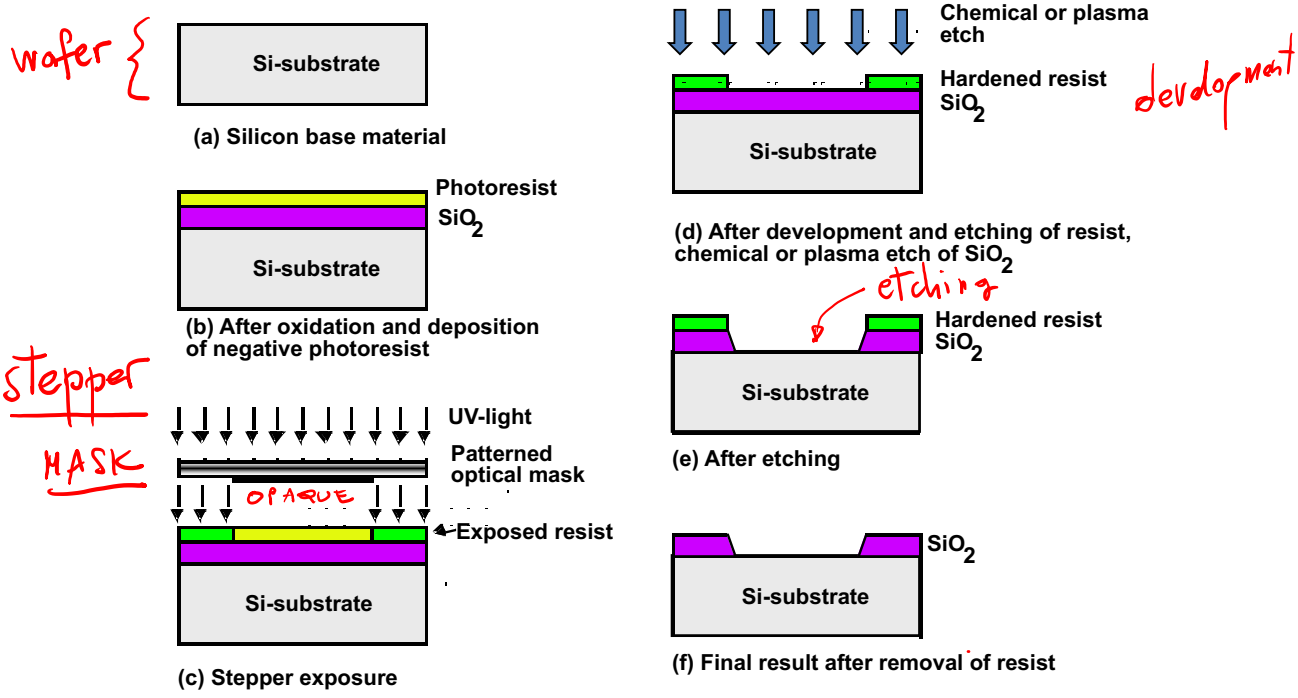


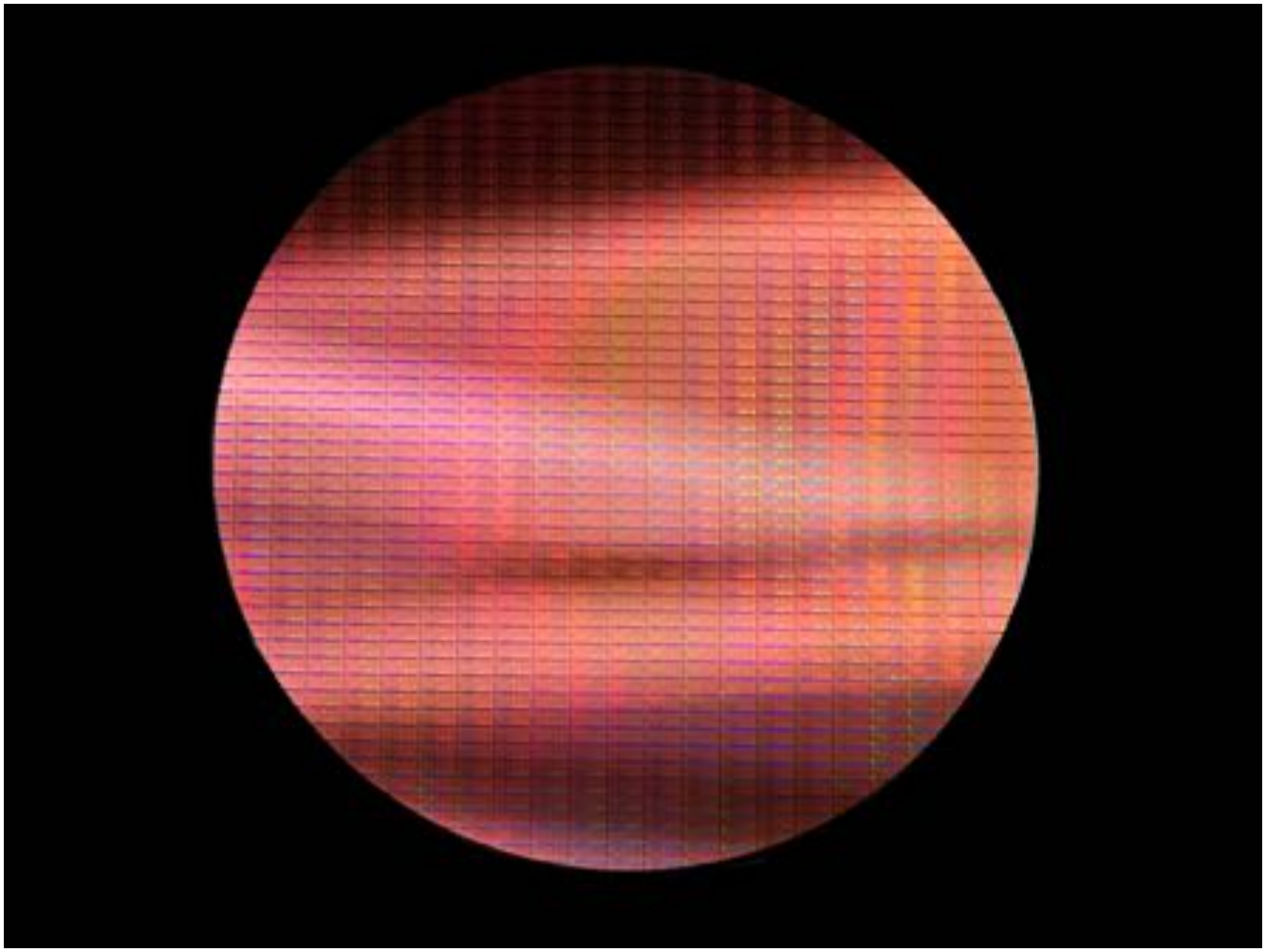
Clean room (class 1-10)

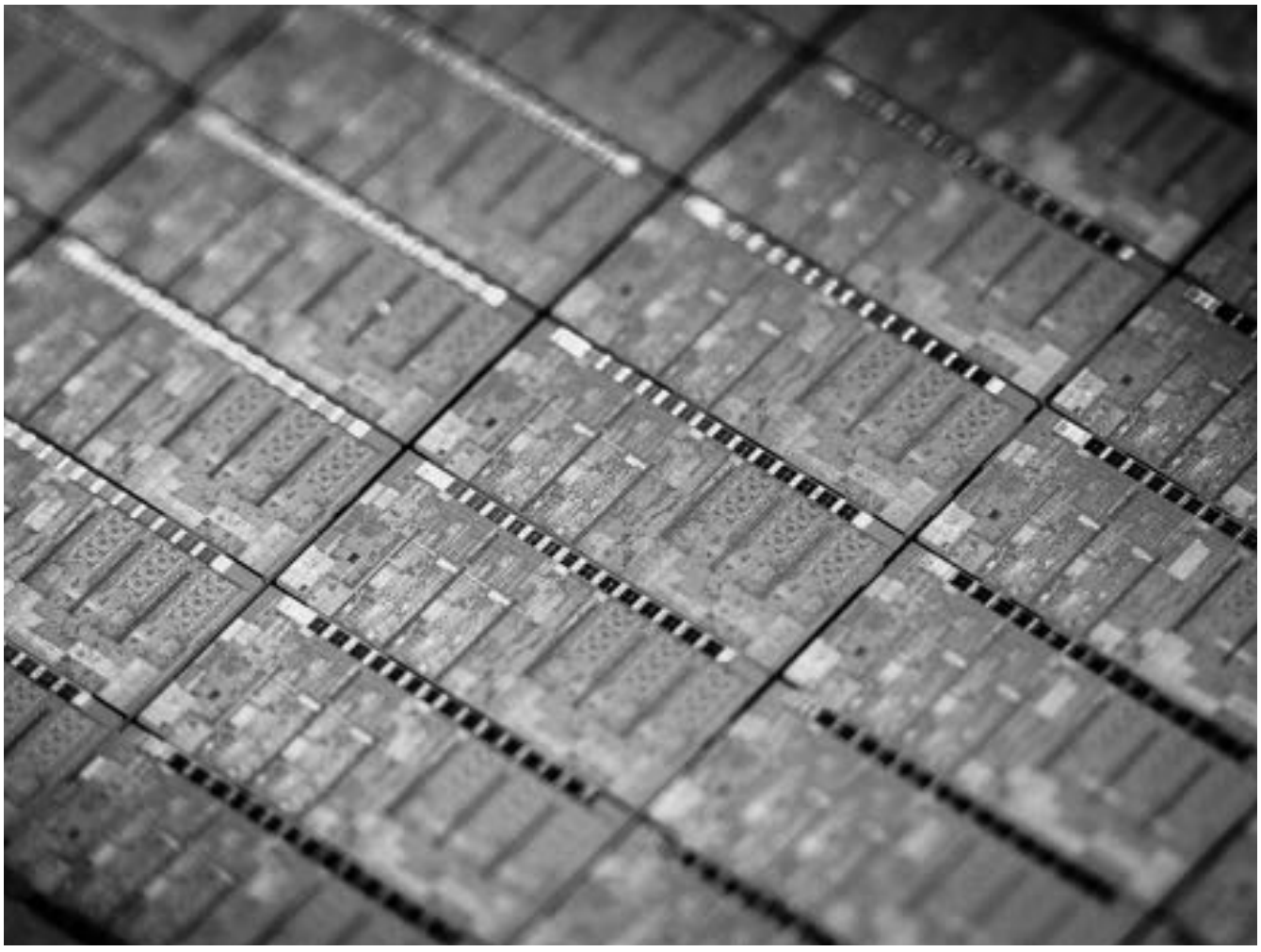
Def:
Class 1: <1 dust particle per cubic foot

In each processing step, an area of the chip is masked out using optical masks, so that the process step is selectively applied to the other regions

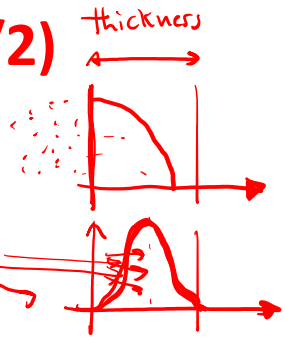
Example of process step: Patterning of SiO2







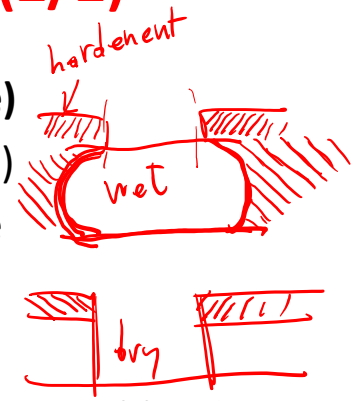
Recurring process steps (1/2)



- **Doping**
  - **Diffusion** (gas with dopant, 900-1100 °C)
  - **Ion implantation**
    - Lattice damage (displacement of atoms)

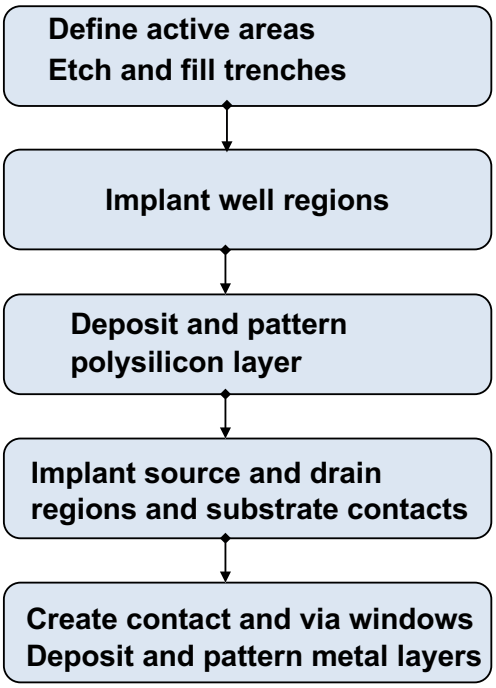
    → **Annealing** step (1000 °C for 15-30' + slow cooling)
- **Deposition** (of layers over the complete wafer)
  - **Oxidation** [silicon oxide]
  - **Chemical Vapor Deposition**: gas phase + heat (850 °C) [silicon nitride]
  - **Chemical deposition** (polysilicon: silane (SiH_4) gas over heated wafer (600 °C) → reaction an polysilicon formation
  - **Sputtering** (for aluminum): evaporation in vacuum chamber

Recurring process steps (2/2)



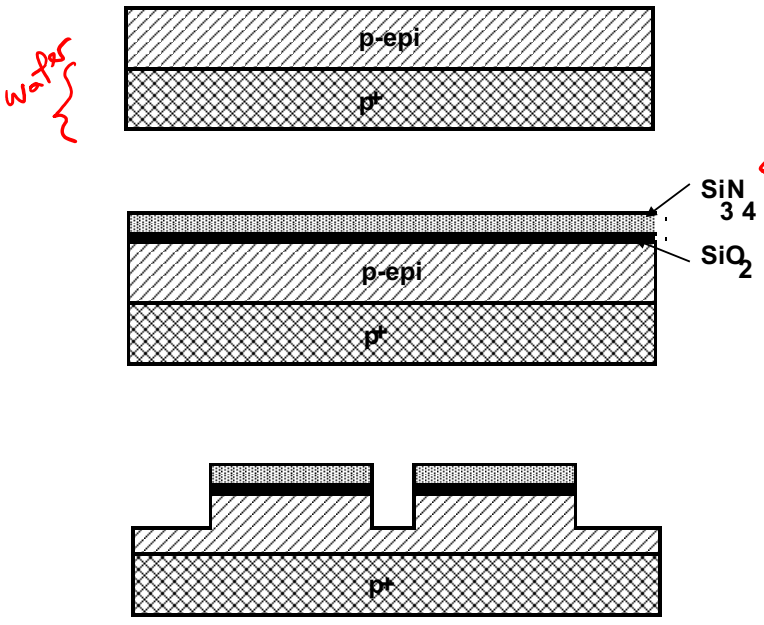
- **Etching (defines 3D patterns on the surface)**
  - **Wet etching** (with acid or basic solutions)
    - e.g. Hydrofluoric acid for silicon oxide
    - Almost isotropic
  - **Dry or plasma etching**
    - Plasma: mix of nitrogen, chlorine, boron trichloride
    - Strongly anisotropic (steep vertical edges)
- **Planarization (**flatten the surface to allow layer deposition)
  - **Chemical Mechanical Polishing (CMP)**
    - Liquid carrier with a suspended abrasive component

Simplified CMOS Process flow



- Active areas: where transistors are
- Field oxide: insulator between neighboring devices
- Wells in the active areas
- Gate stack
- Contact doping
- Metal Interconnects

CMOS Process Walk-Through



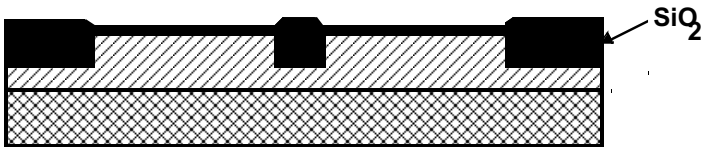
(a) Base material: p+ substrate with p-epi layer

← SILICON NITRIDE (sacrificial layer)

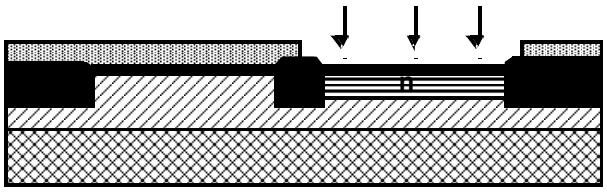
(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

(c) After plasma etch of insulating trenches using the inverse of the active area mask

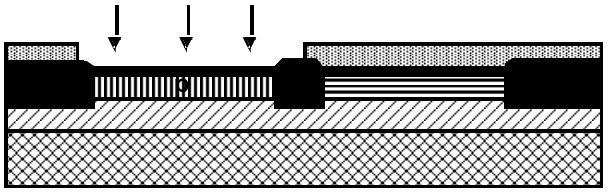
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

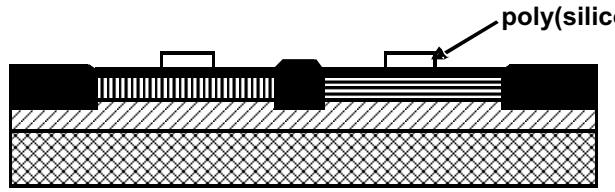


(e) After n-well and V_{Tp} adjust implants

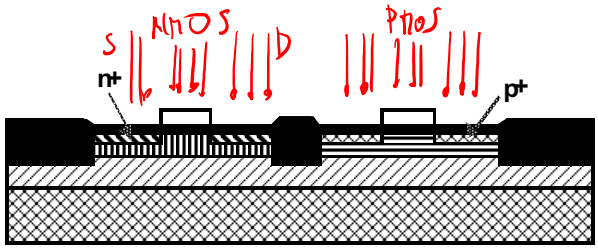


(f) After p-well and V_{Tn} adjust implants

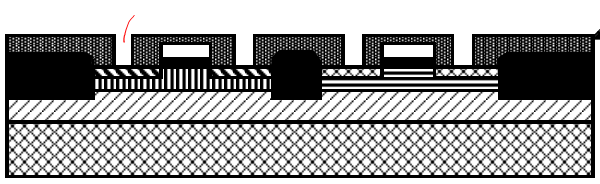
CMOS Process Walk-Through



(g) After polysilicon deposition and etch

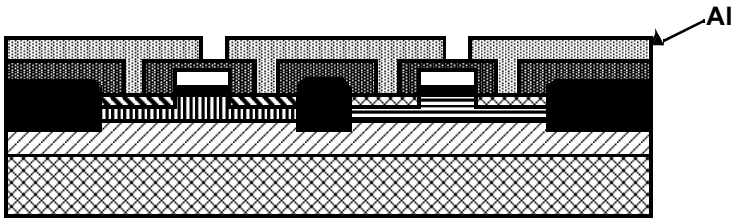


(h) After n+ source/drain and p+ source/drain implants. These steps also dope the polysilicon.

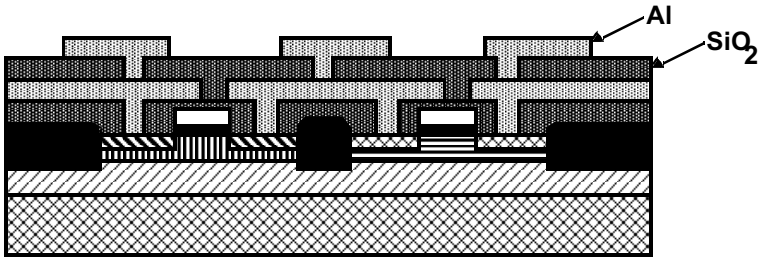


(i) After deposition of SiO_2 insulator and contact hole etch.

CMOS Process Walk-Through

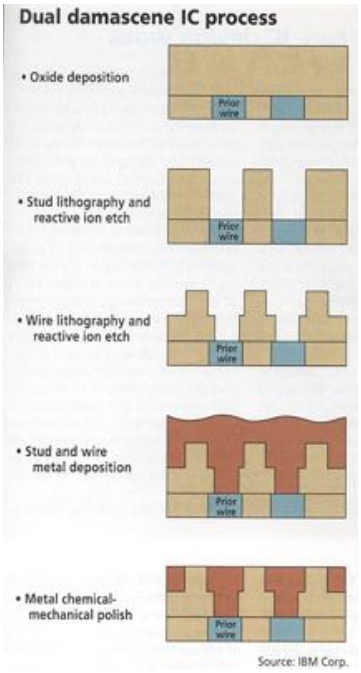


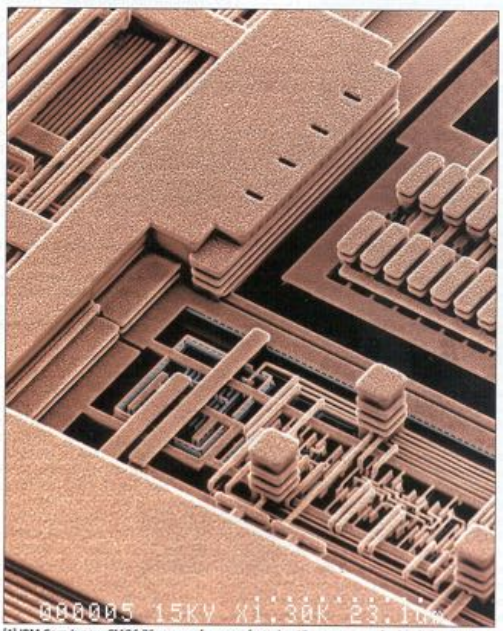
(j) After deposition and patterning of first Al layer.



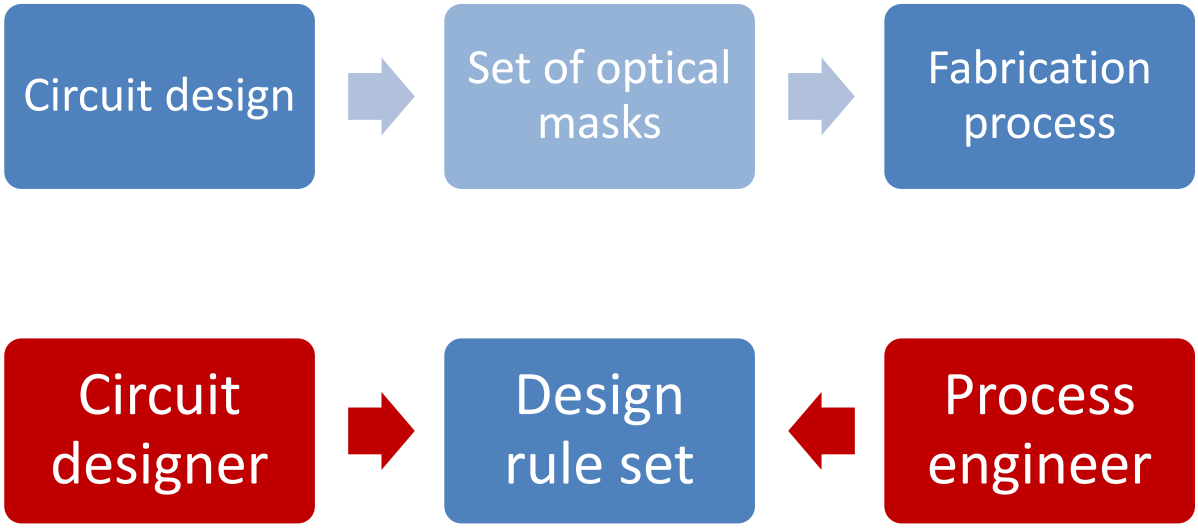
(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

Advanced Metallization





CMOS Manufacturing process

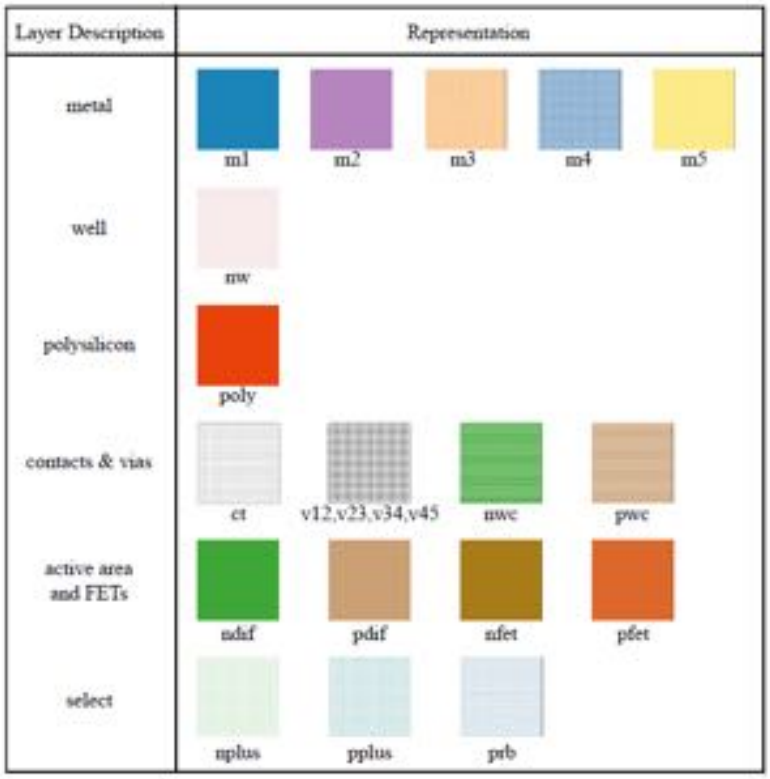


All material: Chap. 2 of J. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits, second edition, Prentice Halls, 2002

Design Rules

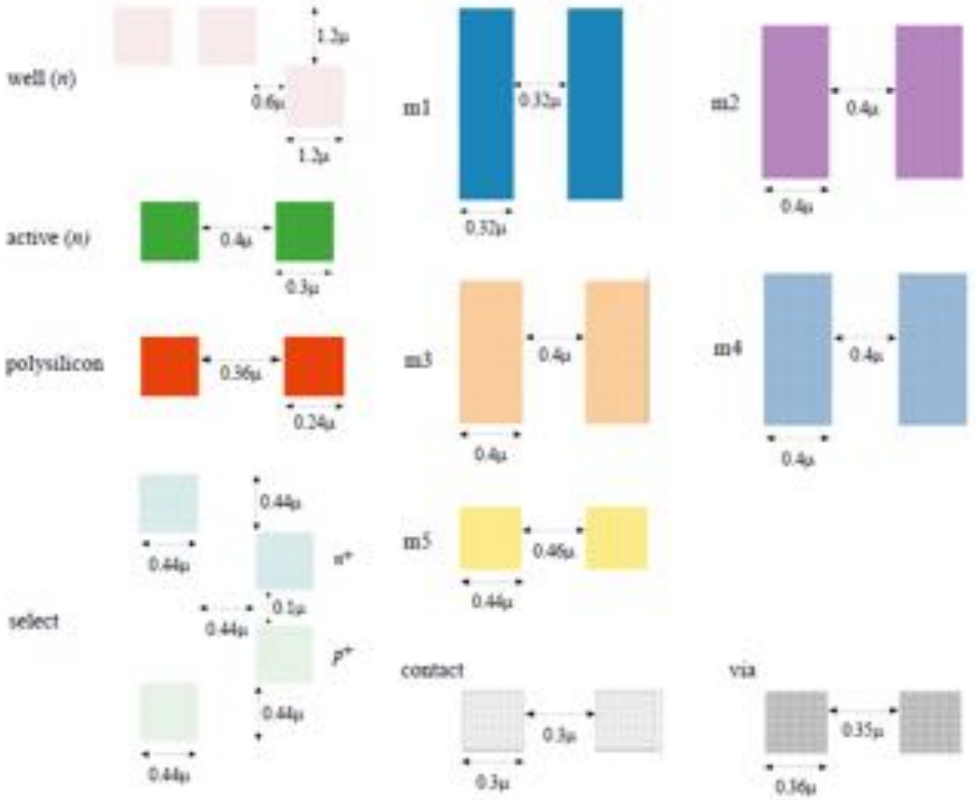
- Minimum line width depends on **lithography** and **process**
- **Micron rules: absolute dimensions** for intra-layer and inter-layer layouts

Example: Layers in 0.25 μm CMOS process



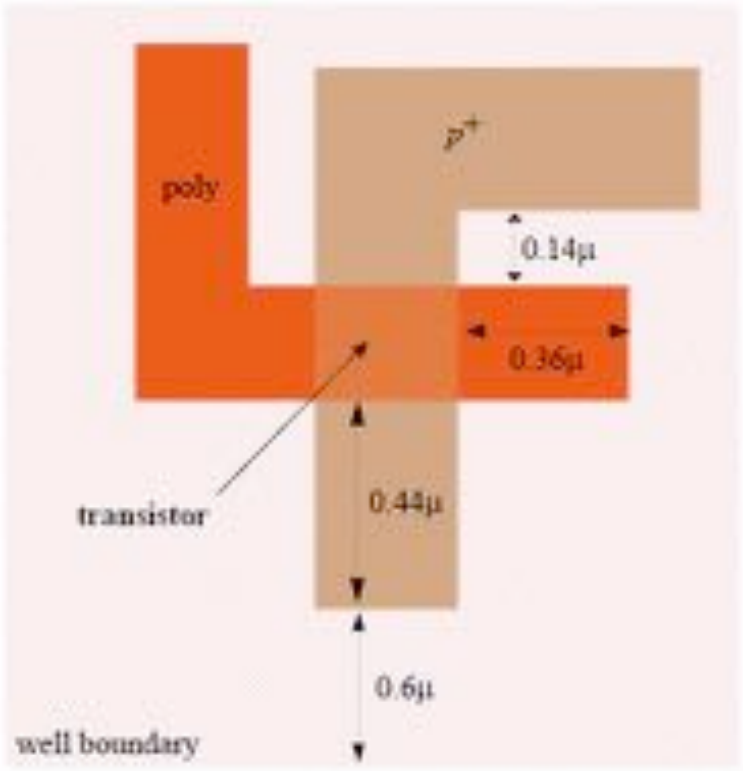
Colorplate 1. CMOS layers and representations (for vanilla 0.25 μm CMOS process)

Intra-Layer Design Rules



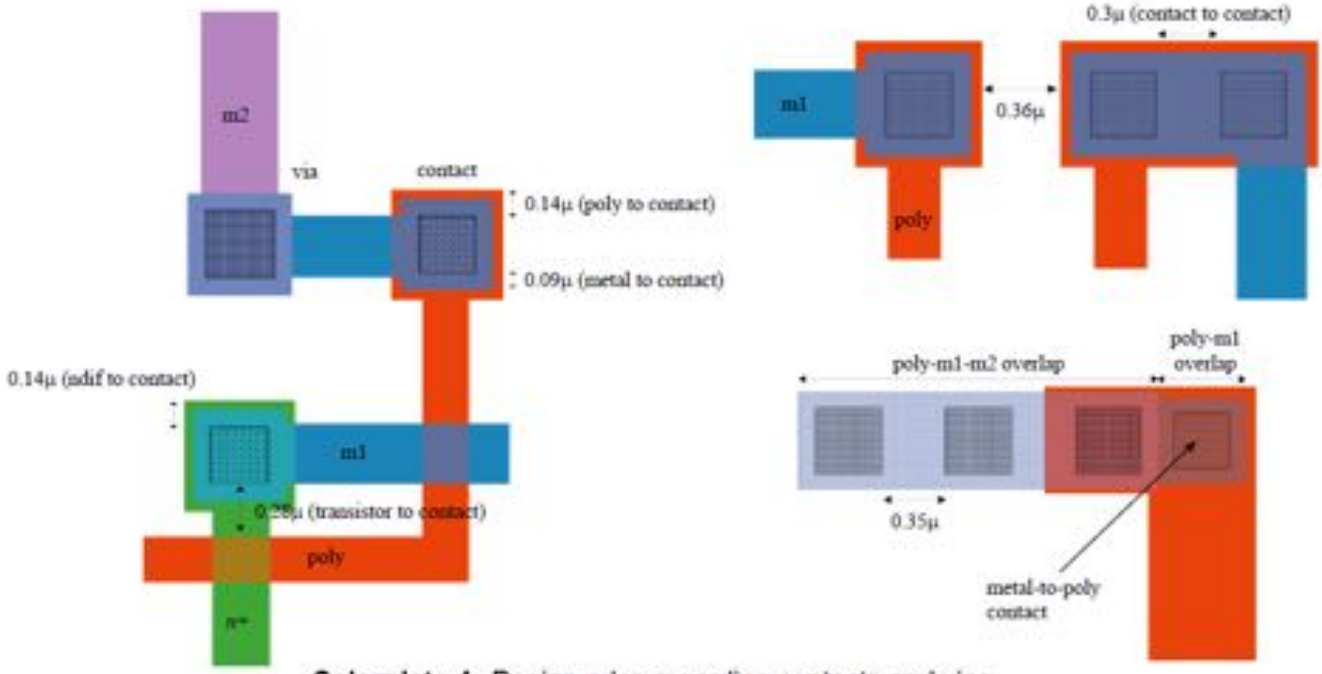
Colorplate 2. Intra-layer layout design rules, expressed as minimum dimensions and spacings.

Inter-layer rules: Transistor Layout



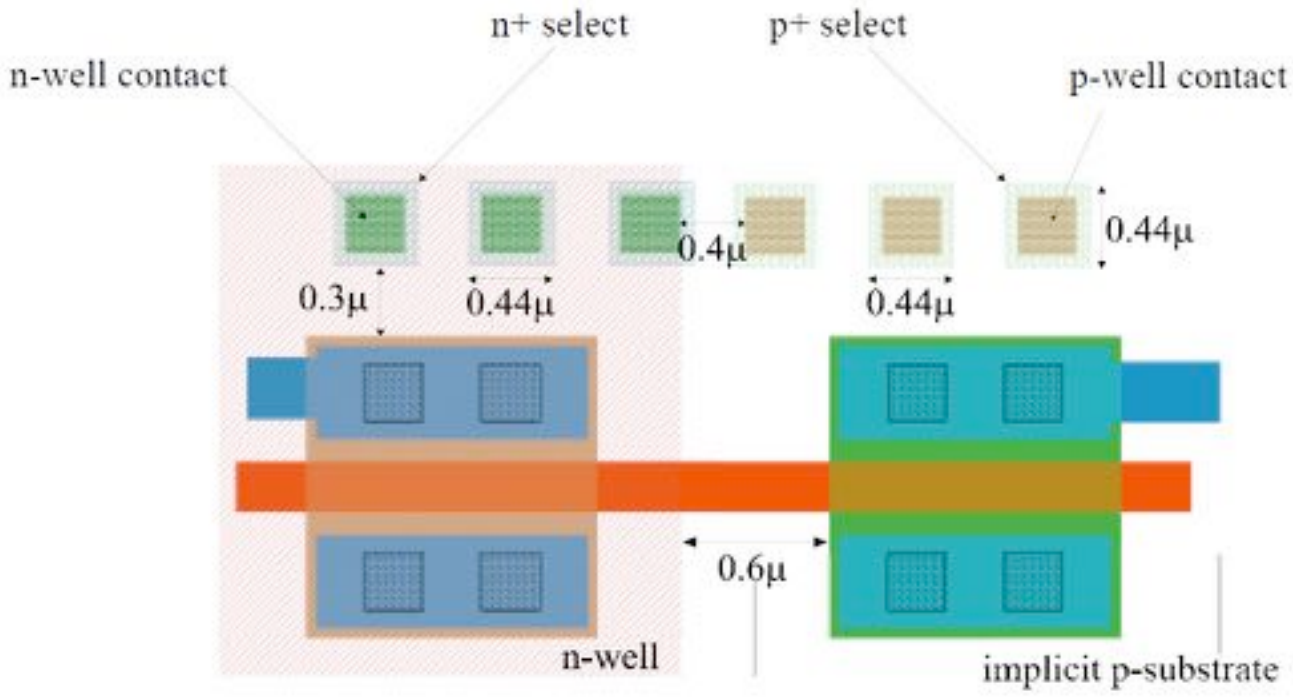
Colorplate 3. Design rules concerning transistor layout. The device shown is a PMOS transistor.

Inter-layer rules: Vias and Contacts



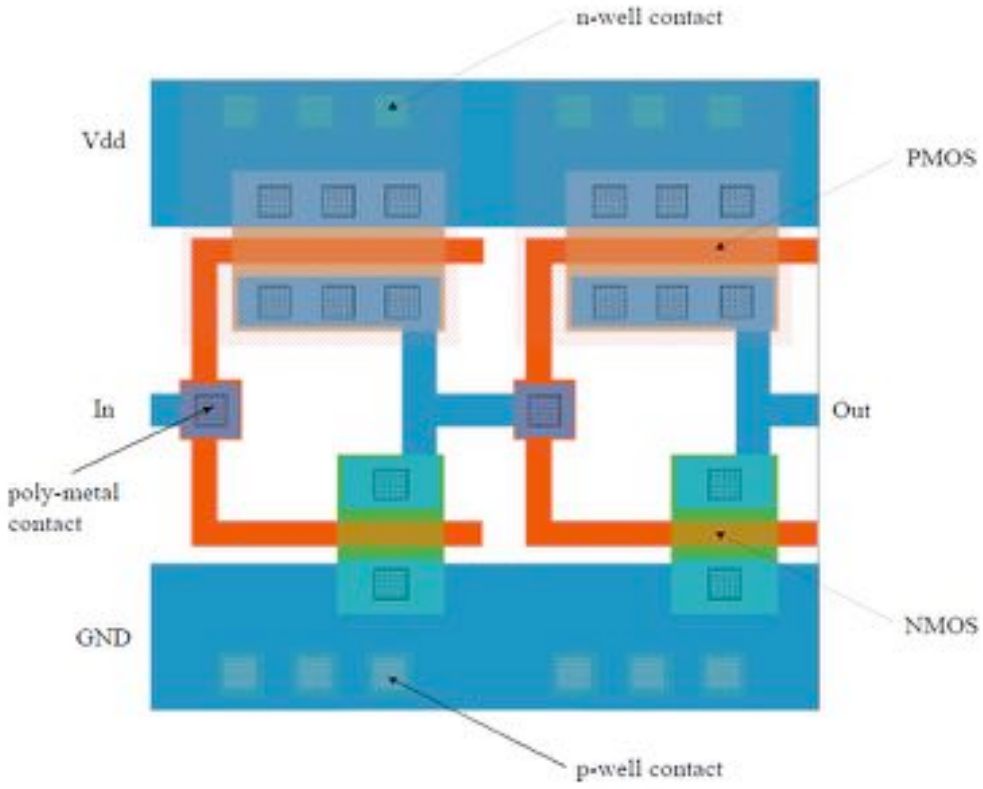
Colorplate 4. Design rules regarding contacts and vias. Overlapping layers are marked by merged colors.

Inter-layer rules: Select Layer



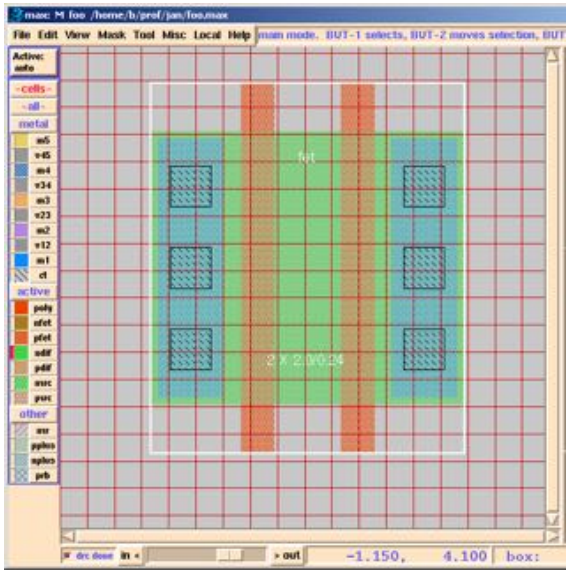
Colorplate 5. Design rules regarding well contacts and select layers.

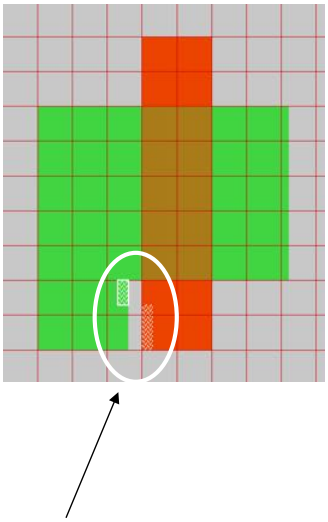
CMOS Inverter Layout



Colorplate 6. Layout of inverter in 0.25 µm CMOS technology.

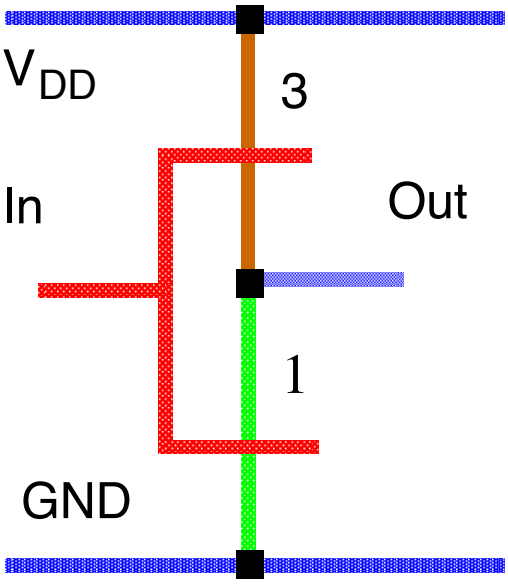
Layout Editor & Design Rule Checker





poly_not_fet to all_diff minimum spacing = 0.14 um.

Stick Diagram



Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by "compaction" program

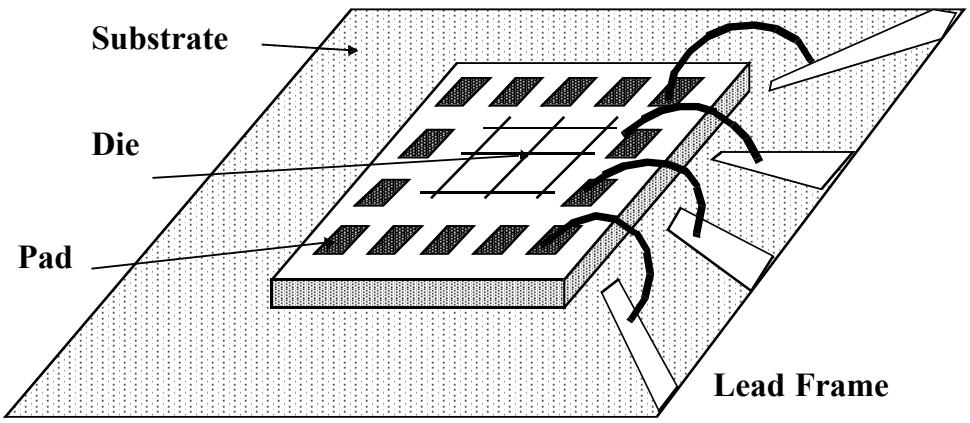
Packaging Requirements

Packages must satisfy different types of requirements

- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap

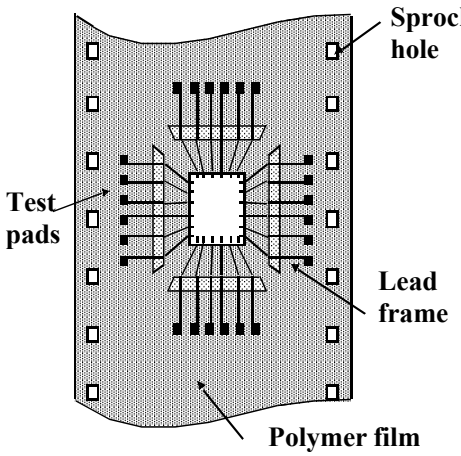
Bonding Techniques

Wire Bonding

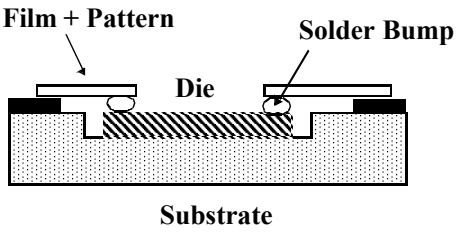


Gold wires, large inductance

Tape-Automated Bonding (TAB)

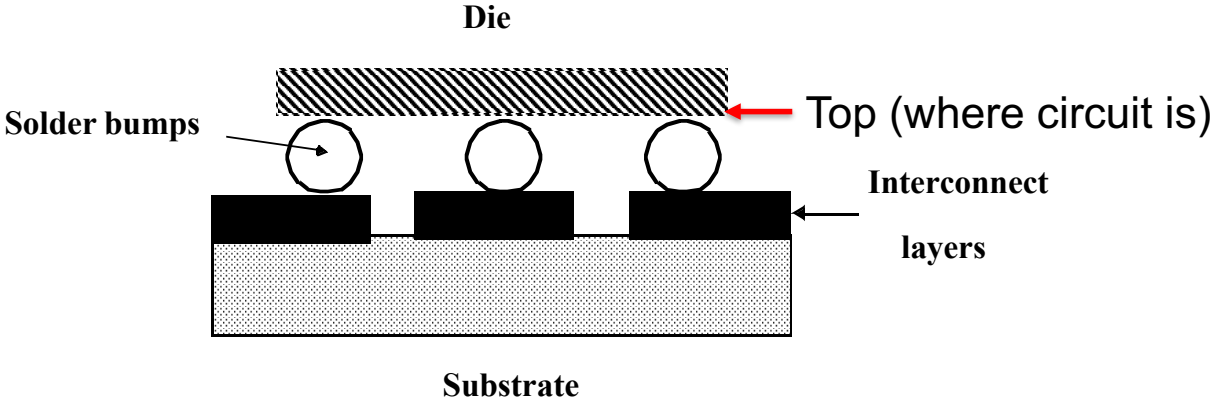


(a) Polymer Tape with imprinted wiring pattern.

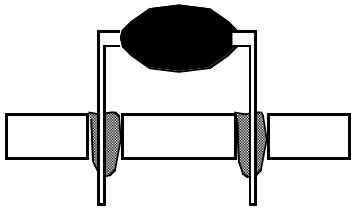


(b) Die attachment using solder bumps.

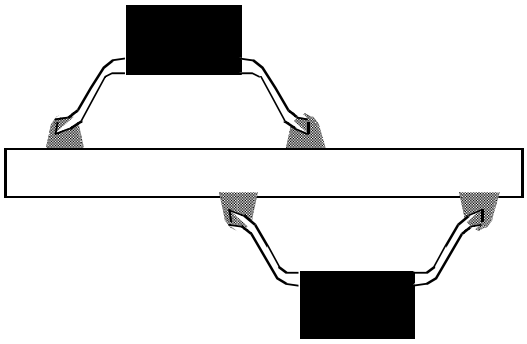
Flip-Chip Bonding



Package-to-Board Interconnect

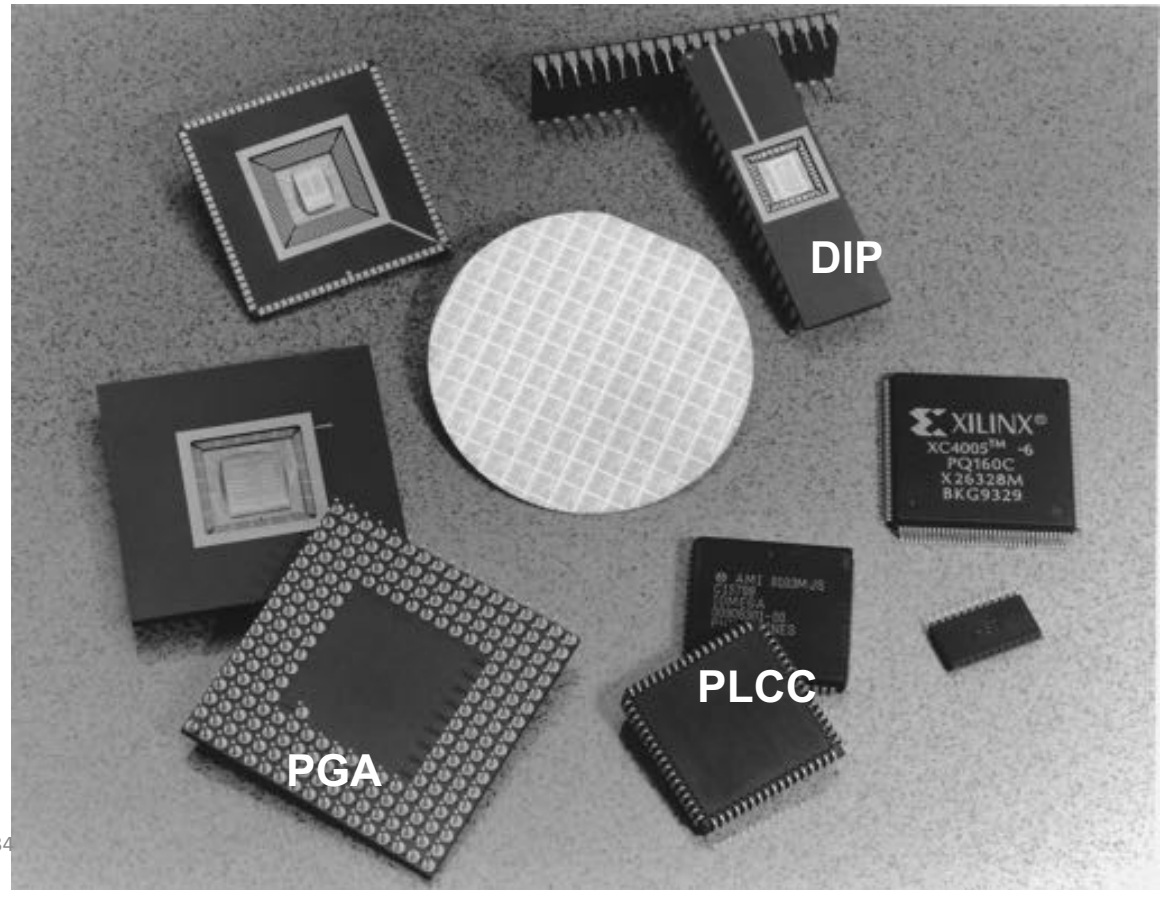


(a) Through-Hole Mounting



(b) Surface Mount

Package Types



Package Parameters

Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

Multi-Chip Modules