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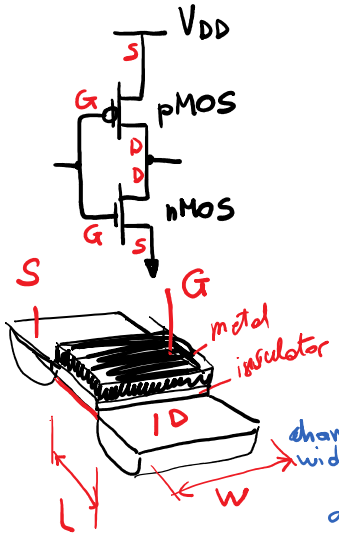
CMOS Inverter



NMOS

1) $V_{GS} < V_{Tn}$ ← OFF

V_{Tn}: threshold voltage of NMOS

2) $V_{GS} > V_{Tn}$ $\quad V_{DS} < V_{GS} - V_{Tn}$

Ohmic region

$$I_D = K_n \left[(V_{GS} - V_{Tn}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$(V_{GS} - V_{Tn})$: GATE OVERDRIVE

$$K_n = \frac{W}{L} \mu_n C_{ox} = \frac{W}{L} \mu_n \frac{\varepsilon_0 \varepsilon_r}{t_{ox}}$$

- $\frac{W}{L}$: channel width / channel length
- μ_n: electron mobility
- C_{ox}: gate dielectric capacitance per unit area
- ε_r: relative dielectric permittivity
- t_{ox}: oxide thickness

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3) $V_{GS} > V_{Tn}$ $\quad V_{DS} > V_{GS} - V_{Tn}$

SATURATION REGION

$$I_D = \frac{1}{2} K_n (V_{GS} - V_{Tn})^2$$

PMOS

$V_{Tp} < 0$

V_{Tp}: threshold voltage of PMOS

1) OFF $\quad V_{GS} > V_{Tp}$

2) OHMIC REGION

$V_{GS} < V_{Tp} < 0$

and $0 > V_{DS} > V_{GS} - V_{Tp}$ (by definition)

$$I_D = K_p \left[(V_{GS} - V_{Tp}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$K_p = \frac{W}{L} \mu_p C_{ox}$$

μ_p: hole mobility

3) SATURATION REGION

$V_{GS} < V_{Tp} < 0$ and $V_{DS} < V_{GS} - V_{Tp} < 0 \rightarrow I_D = \frac{1}{2} K_p (V_{GS} - V_{Tp})^2$

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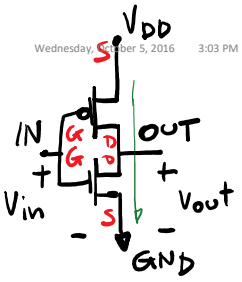
TRANSFER CHARACTERISTIC OF THE CMOS INVERTER



$V_{in} = V_{GSn}$

$V_{in} - V_{DD} = V_{GSp}$

$V_{out} = V_{DSn}$

$V_{out} - V_{DD} = V_{DSp}$

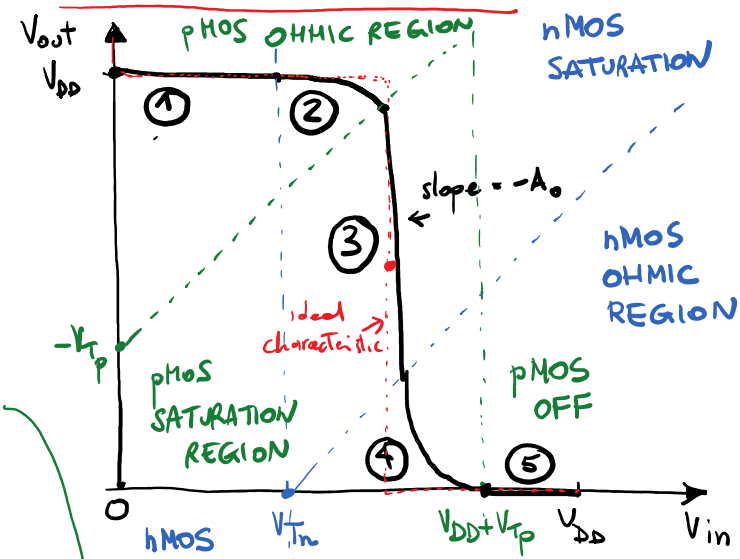
nMOS

) OFF $V_{in} < V_{Tn}$

) OHMIC REGION

$V_{in} > V_{th}$

$V_{out} < V_{in} - V_{Tn}$



pMOS

) OFF : $V_{GSp} > V_{Tp} \Rightarrow V_{in} - V_{DD} > V_{Tp}$

$V_{in} > V_{DD} + V_{Tp}$

) OHMIC REGION : $V_{in} < V_{DD} + V_{Tp}$

and $V_{DSp} > V_{GSp} - V_{Tp}$

$V_{out} - V_{DD} > V_{in} - V_{DD} - V_{Tp} \Rightarrow V_{out} > V_{in} - V_{Tp}$

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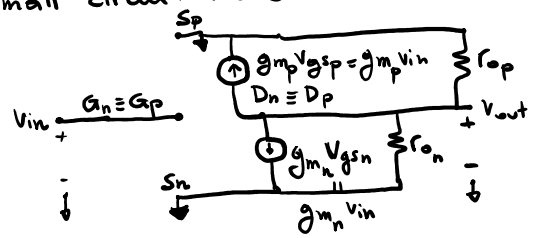
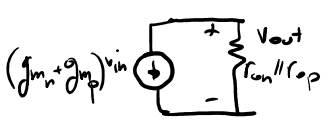
I-V Transfer characteristic of the CMOS inverter

1. PMOS OHMIC REGION – NMOS OFF
2. PMOS OHMIC REGION – NMOS SAT
3. PMOS SAT – NMOS SAT
   ↳ Small circuit model



4. PMOS SAT – NMOS OHMIC REGION

5. PMOS OFF
   NMOS OHMIC REGION



$\Rightarrow \frac{V_{out}}{V_{in}} = -r_{on} // r_{op} (g_{mn} + g_{mp})$

$\frac{V_{out}}{V_{in}} = -A_0$

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Balanced inverter

when $V_{in} = \frac{V_{DD}}{2}$ then $V_{out} = \frac{V_{DD}}{2}$

IF THE PMOS AND NMOS CHARACTERISTICS ARE COMPLEMENTARY

↳ $V_{Tp} = -V_{Tn}$ → (obtain with doping)

AND

$k_n = k_p \Rightarrow \frac{W_n}{L_n}\mu_n C_{ox} = \frac{W_p}{L_p}\mu_p C_{ox}$

(L_n: min L, L_p: min L)

$W_n\mu_n = W_p\mu_p$

) TRADITIONAL CMOS

$\mu_n \sim 2\mu_p \rightarrow W_p \sim 2W_n$

) MODERN CMOS

$\mu_n = \mu_p \Rightarrow W_p = W_n$

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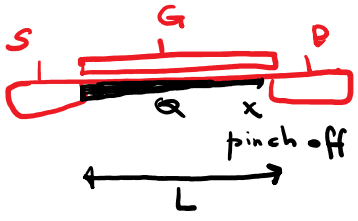
I-V CHARACTERISTICS FOR SMALL TRANSISTORS ($L < 100$ nm)

long transistor in SAT for $V_{GS} = V_{DD}$, $V_{DS} = V_{DD}$

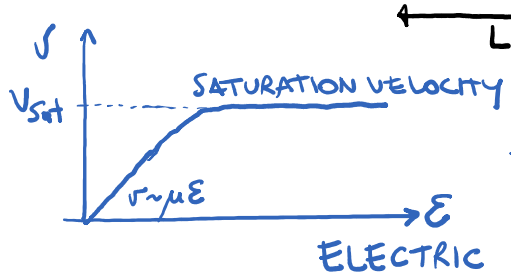
$I_D = \frac{k_n}{2}(V_{DD} - V_{Tn})^2 = I_{ON}$

(?) mobile charge

$Q \propto C(V_{DD} - V_{Tn})$



DRIFT VELOCITY



$v = \mu\mathcal{E} = \mu\frac{(V_{DD} - V_{Tn})}{L}$

$I \propto Qv \propto (V_{DD} - V_{Tn})^2$

→ IN SMALL TRANSISTORS

$Q \propto C(V_{DD} - V_{Tn})$

$v \sim v_{sat}$

$I \propto Qv \propto (V_{DD} - V_{Tn})$

$I_{ON} = \frac{W\varepsilon_0\varepsilon_r v_{sat}(V_{DD} - V_{Tn})}{t_{ox}}$

I_{ON} DOES NOT DEPEND ON L

Propagation delay

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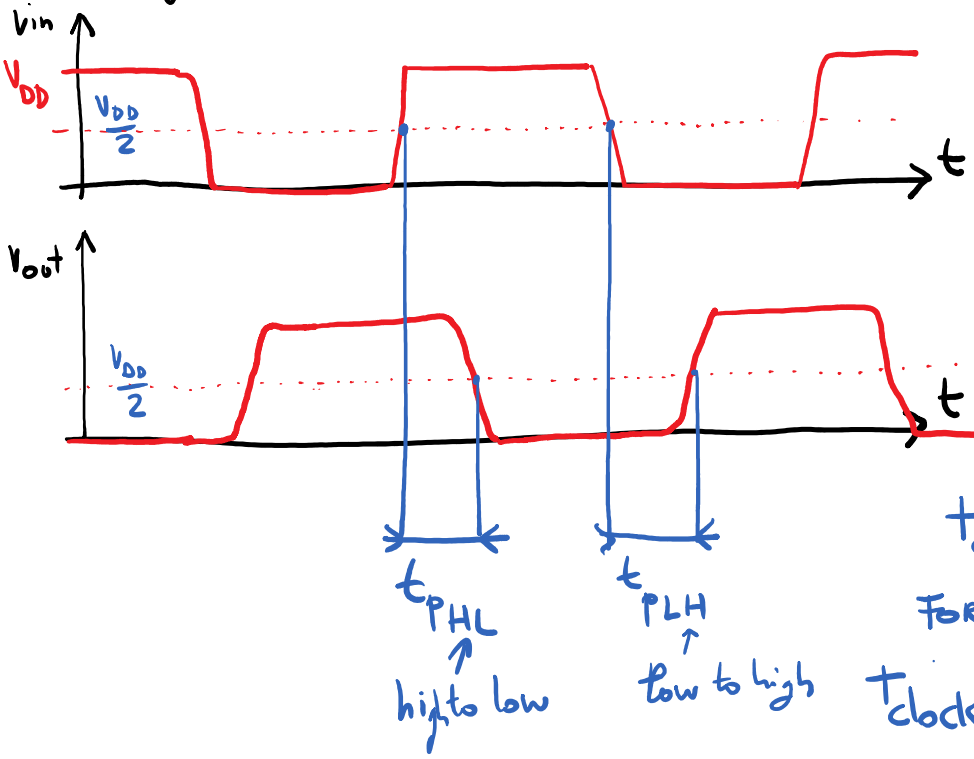

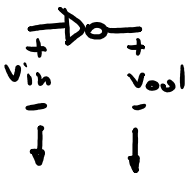

$t_{clock} \gg t_{PHL}, t_{PLH}$

FOR EXAMPLE

$t_{clock} \approx 20 \max(t_{PHL}, t_{PLH})$

t_{PHL}

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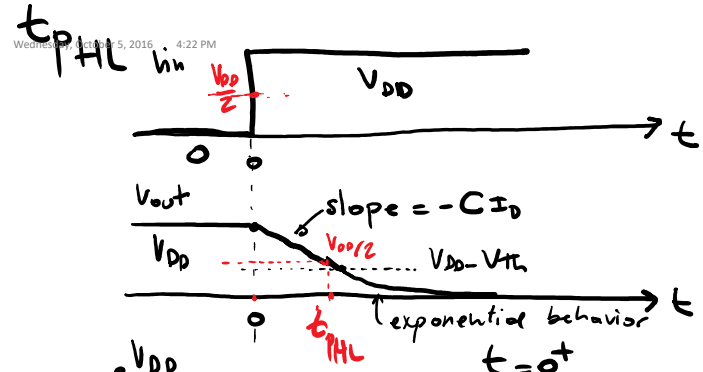
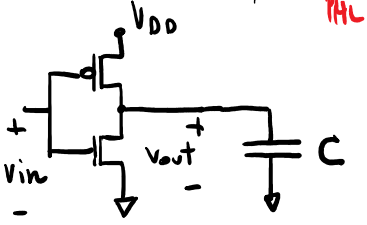
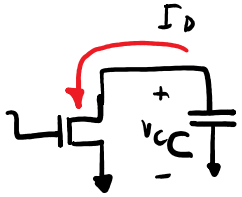




$t = 0^+$

PMOS OFF $(V_{GS_p} = 0)$

NMOS SAT $(V_{GS_n} = V_{DD}, V_{DS_n} = V_{out} > V_{DD})$



$I_D = \frac{1}{2} k_n (V_{DD} - V_{Th})^2$

CONSTANT CURRENT

$$-\frac{dV_c}{dt} = \frac{I_D}{C} \Rightarrow \frac{dV_{out}}{dt} = -\frac{I_D}{C}$$

until $V_{DS} < V_{GS} - V_{Th} \rightarrow V_{out} < V_{DD} - V_{Th}$

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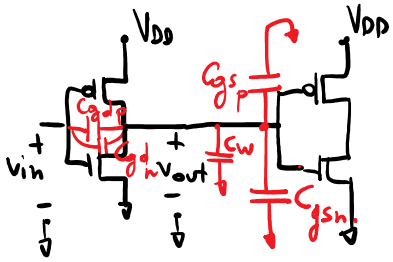
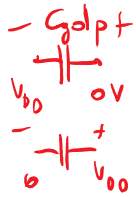
$$t_{pHL} = \frac{C V_{DD}/2}{I_D} = \frac{C V_{DD}}{2 I_D} = \frac{C V_{DD}}{\frac{k_n}{2}(V_{DD}-V_{th})^2} = \frac{C V_{DD}}{k_n (V_{DD}-V_{th})^2}$$

what is C ?



$$C = C_w + C_{gs_n} + C_{gs_p} + 2C_{gd_p} + 2C_{gd_n}$$

equivalent capacitance at the inverter output



$t<0 \; Q = -C_{gd_p} V_{DD}$

$t>0 \; Q = +C_{gd_p} V_{DD}$

$\Delta Q = 2C_{gd_p} V_{DD}$

$\Rightarrow$

$t<0 \; Q = 0$

$t>0 \; Q = 2C_{gd_p}$

$\Delta Q = 2C_{gd_p} V_{DD}$

LONGER MOSFETS

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$$t_{pHL} = \frac{C V_{DD}}{k_n (V_{DD}-V_{Th})^2} \qquad t_{pLH} = \frac{C V_{DD}}{k_p (V_{DD}-|V_{Tp}|)^2}$$

$\propto WL \propto L^2$

$k_n = \frac{W_n}{L} \mu_n C_{ox}$ $\quad k_p = \frac{W_p}{L} \mu_p C_{ox}$

1) IF THE INVERTER IS BALANCED THEN $t_{pHL} = t_{pLH} = t_p$

$$f_{clock} = \frac{1}{t_{clock}} \ll \frac{1}{t_p}$$

$t_p \propto L^2$

1) $V_{DD} \uparrow \quad t_p \downarrow \quad f_{clock} \uparrow$

2) $\mu_n \uparrow$ / $\mu_p \uparrow \quad t_p \downarrow \quad f_{clock} \uparrow$

3) $L \downarrow \quad t_p \downarrow\downarrow \quad f_{clock} \uparrow\uparrow$

Small mosfets ($L<100\,nm$)

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$$I_{DN} = \frac{W \varepsilon_0 \varepsilon_r}{t_{ox}} v_{sat} (V_{DD} - V_{Tn})$$

$\propto WL \propto L^2$

$$t_{pHL} = \frac{C V_{DD}}{2 I_{ON_n}} = \frac{C V_{DD} t_{ox}}{2 W_n \varepsilon_0 \varepsilon_r v_{sat_n} (V_{DD} - V_{tn})}$$

$W_n \propto L$

$$t_{pLH} = \frac{C V_{DD}}{2 I_{ON_p}} = \frac{C V_{DD} t_{ox}}{2 W_p \varepsilon_0 \varepsilon_r v_{sat_p} (V_{DD} - |V_{Tp}|)}$$

if $V_{DD}\uparrow$ $t_{pHL}\sim$ ← $t_p \sim L$

if $v_{sat_n}\uparrow$ $v_{sat_p}\uparrow$ $t_p\downarrow$ $f_{clock}\uparrow$

if $L\downarrow$ $t_p\downarrow$ $f_{clock}\uparrow$ ←

Power Consumption

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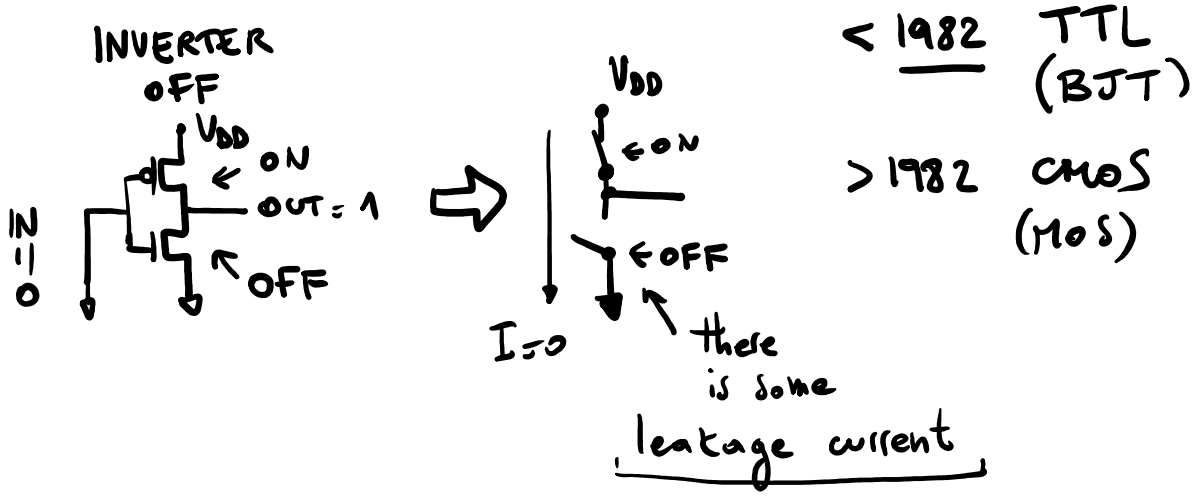

< 1982 TTL (BJT)

> 1982 CMOS (MOS)

NMOS TRANSISTOR

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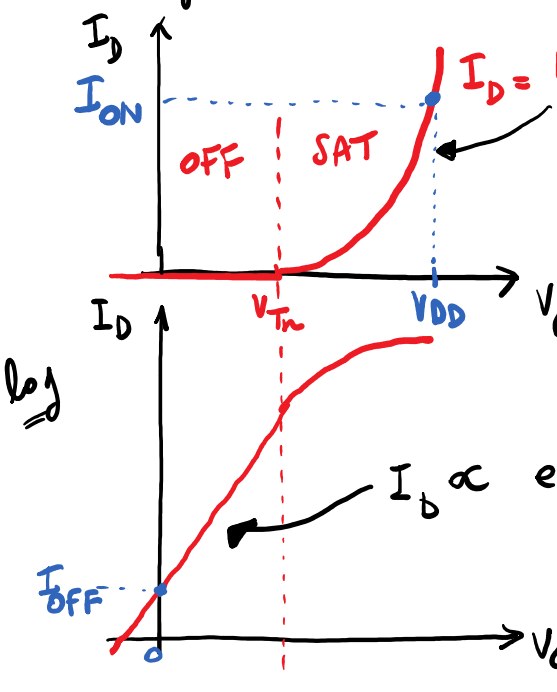
→ Transfer characteristics



$$I_D = k\left(V_{GS}-V_{tn}\right)^2 \quad \left[\frac{V_{GS}-V_{Tn}}{\phi_t} \gg 1\right]$$

$$\rightarrow I_D = 2K\phi_T^2\left\{\log\left[1+\exp\left(\frac{V_{GS}-V_{Tn}}{2\phi_t}\right)\right]\right\}^2$$

$$I_D \propto \exp\left(\frac{V_{GS}-V_{Tn}}{\phi_t}\right) \quad \text{if} \left(\frac{V_{GS}-V_{Tn}}{\phi_t} \ll 1\right)$$

thermal voltage $\phi_t = \frac{k_B T}{q}$

$[T = 300K \rightarrow \phi_t \simeq 26mV]$

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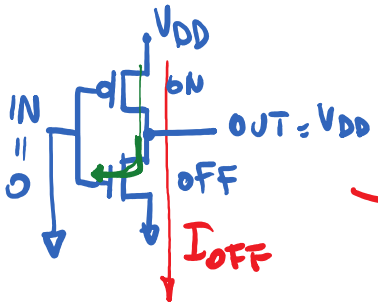
$$I_{ON} = I_D\Big|_{\substack{V_{GS}=V_{DD}\\ V_{DS}=V_{DD}}}$$

$$I_{OFF} = I_D\Big|_{\substack{V_{GS}=0\\ V_{DS}=V_{DD}}}$$



→ $P_S = V_{DD} I_{OFF} = V_{DD}\left[2K\phi_T^2 \exp\left(\frac{-V_{th}}{\phi_T}\right)\right]$

STATIC POWER CONSUMPTION

$P_S \propto V_{DD}$

$P_S \propto \exp\left(-\frac{V_{Tn}}{\phi_t}\right)$

Dynamic Power Consumption

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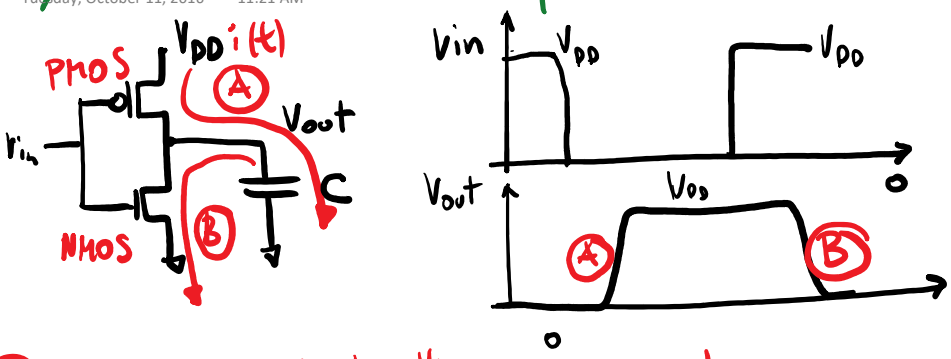

(A) Energy spent by the power supply

$$E = \int V_{DD} i(t)\,dt = V_{DD} \int i(t)\,dt = V_{DD} C V_{DD} = C V_{DD}^2$$

energy stored on the capacitance

$$E_C = \frac{1}{2} C V_{DD}^2$$

(B) Power supply spend NO energy

ENERGY CONSUMPTION PER CYCLE $E = C V_{DD}^2$

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Dynamic power consumption $P_D = C V_{DD}^2 f_{clk}$

$P_D = C V_{DD}^2 f_{clk}\, \alpha$ ← activity factor $0 < \alpha < 1$ (typically $\alpha \approx 0.1$)

for the whole chip

$$P_D = \sum_i C_i V_{DD}^2 f_{clk}\, \alpha = C_{TOT} V_{DD}^2 f_{clk} \alpha$$

$$P_S = \sum_i V_{DD} I_{OFF_i} = V_{DD} I_{OFF\_TOT}$$

$$P_{TOT} = P_D + P_S$$

Scaling of CMOS Technology

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- $P_D = CV_{DD}^2 f_{clock}$
- $P_S = V_{DD} I_{OFF}$
- $t_p = \frac{CV_{DD}}{2I_{ON}} = \frac{L}{2v_{sat}}\left(\frac{V_{DD}}{V_{DD}-V_{Tn}}\right)$
- $t_{clock} \sim 20 t_p$
- $C_{ox} \frac{WL}{t_{ox}}$

GENERALIZED SCALING

- scaling factor for VOLTAGE λ $(\lambda > 1)$
- scaling factor for GEOMETRY s $(s > 1)$

QUANTITY	SCALING FACTOR
W, L, t_{ox}	$1/s$
V_{DD}, V_{Tn}	$1/\lambda$
t_p	$1/s$
f_{clock}	s
P_D	$1/\lambda^2$
Area	$1/s^2$

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Phase 1 1980 ≃ 1992 CONSTANT VOLTAGE SCALING

V_{DD} : 5V

$\lambda = 1$ $s > 1$

$\frac{P_D}{A} \propto s^2$

INCREASE OF POWER DENSITY PER UNIT AREA

Phase 2 1992 – 2002 CONSTANT FIELD SCALING

$\lambda = s$ $\frac{P_D}{A}$ is CONSTANT CONSTANT POWER DENSITY PER UNIT AREA

Computational performance $\propto \frac{1}{A} f_{clock} \propto s^3$

	1992	2002			1992 – 2002
L	0.5μm	0.13μm	→	t_{ox}	7nm – 2nm
V_{DD}	5V	1.5V		V_{Tn}	1.5V – 0.4V

GATE LEAKAGE

Phase 3

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Almost stopped VOLTAGE SCALING $\lambda \sim 1$

geometry scaling S

NO INCREASE OR REDUCTION OF f_{clock}

$$P_D = C V_{DD}^2 f_{clock} \propto 1/S$$

$\uparrow \frac{1}{S} \quad \sim 1 \quad \sim 1$

$$A \propto 1/S^2 \qquad P_D/A \propto S$$

if λ is slight larger than 1
and f decreases we have $\frac{P_D}{A} \sim$ constant