Variability-aware design of 55 nA current reference with 1.4% standard deviation and 290 nW power consumption

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***Abstract*— In this paper we present the design of a 0.18 µm CMOS current reference, which is very robust with respect to process variations (1.4% relative standard deviation measured over 23 samples) and with low power consumption of 290 nW. This result was obtained with devices that have low intrinsic sensitivity to process variability, such as diffusion resistors in a nanopower "classic" BJT-based bandgap topology. At the cost of a larger die area, we obtain a significant reduction of dispersion with respect to the best results available in the literature, with a low power consumption.**

I. INTRODUCTION

The increase of process variability is one of the main problems introduced by the continuous scaling of semiconductor technology. It poses serious challenges to process innovation and circuit design [1]. Indeed, the issue involves both digital and analog design, and prevents circuits to take full advantage of the nominal improvements offered by aggressively scaled technologies.

One way to reduce process variability is through the use of complex feedback systems, based on monitor circuits that assess process variability and actuation knobs adjusting transistor bias points [2]. In other cases, ad-hoc trimming procedures are used. More recently, a method has been presented based on an "internal" compensation, where circuits use the combination of two quantities with reverse-correlated process variations [3]. This type of approach [3], [4], allows us to obtain a significant reduction of the relative standard deviation of the circuit output quantity, between few tenths and a factor 3.

Here we propose the design of a completely integrated reference current generator with low process sensitivity. This is not obtained with trimming or by applying a compensation technique, but with the use of devices intrinsically stable to process variations. This allows us to obtain robustness to process, achieving also low power consumption. The main drawback of the proposed solution is an increase in chip area.

II. THE REFERENCE CURRENT GENERATOR

The reference current generator is an important block for a wide range of analog and digital circuits and systems (for example, it is used as a bias source for oscillators, amplifiers and other analog circuits). It must have a very low sensitivity to supply voltage and especially to process. The continuous development of portable and implantable systems also leads to the requirement of low reference currents and therefore low power consumption.

A general way to achieve low process sensitivity is to "anchor" the reference quantity to an intrinsically stable physical quantity. This approach is useful for the design of a reference voltage, which can be anchored to the silicon bandgap if we choose a bipolar bandgap topology (proposed by Widlar in [5]). For example in [6] a relative standard deviation of the reference voltage of 0.97% is obtained.

While high-precision voltage references can be obtained with this approach, the problem of process variability in reference current generators seems difficult to solve. A reference current is generally obtained from a reference voltage [7], and therefore its expression contains a term corresponding to a voltage multiplied by a transconductive factor. This factor can be related to the MOSFET $\beta=\mu C_{ox}W/L$, where μ is the carrier mobility, C_{ox} is the gate oxide capacitance for unit area, W and L are the MOSFET width and length, respectively. Different architectures can be used for this purpose, mainly based on the self-biased one [8] implemented with MOSFETs and resistors [9], [10], or only MOSFETs [11], [12]. Another way to obtain this current is by applying a bandgap reference voltage on the gate of a MOSFET [13].

The transconductive factor can also be obtained using a resistor, if we choose a bandgap architecture which sums two currents with opposite temperature coefficients [14]-[16]. It can also be obtained by imposing a reference voltage on a resistor [17]. In every case the transconductive factor is more sensitive to process than the voltage term,

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and determines the reference current variability. Indeed, even if we cannot "anchor" the transconductive factor to a reference quantity, we can still use devices intrinsically less sensitive to the process, and available also in standard CMOS technology.

To this aim, here we consider the diffusion resistor. It can be used instead of poly resistor and its advantages in terms of robustness to process sensitivity are due to the lower doping, large volume and monocrystalline material. Lower doping implies that impurity activation is more complete and reliable. Larger volume and monocrystalline material imply a reduced impact of localized defects and grain borders [18].

We use diffusion resistors in the implementation of a bipolar bandgap current generator, that provides the reference voltage with the lowest process sensitivity. Indeed, MOSFET-based generators introduce an additional important source of variability represented by the MOSFET threshold voltage. The threshold voltage is not "anchored" to a reference quantity while the base emitter voltage of a bipolar transistor is determined by the silicon energy gap.

III. DESIGN OF THE CURRENT REFERENCE GENERATOR

The proposed bandgap core is shown in Fig. 1(a), whereas the complete current generator is shown in Fig. 1(b). The circuit is based on the sum of two currents with opposite temperature coefficients. Neglecting the offset voltages of the operational amplifiers, the reference current can be expressed as:

$$I_{ref} = \alpha_1 \frac{V_T \ln(nm)}{R_a} + \alpha_2 \frac{V_{be1}}{\alpha R_b}, \qquad (1)$$

where α_1 is the current mirror ratio of M2 and M3, m is the current mirror ratio of M1 and M2 ($I_1=mI_2$, where I_1 and I_2 are the emitter currents of Q1 and Q2, respectively), n is the ratio of the inverse saturation currents of Q2 and Q1, I_{s2} and I_{s1} ($I_{s2}=nI_{s1}$), α_2 is the current mirror ratio of M4 and M5 and α is a resistive partition. From Eq. (1) one can appreciate the main sources of variability for the reference current (in terms of inter-die and inter-batch variations) which are represented by resistors R_a and R_b. This is the reason we use diffusion resistors to implement R_a and R_b. The base emitter voltage of Q1, which is another source of variability for the current, can be anchored to the silicon energy gap, so it can be very stable versus process.

If we consider also the amplifier offset voltage, we must note that in the bandgap core the voltage drop ΔV_{Ra} across R_a is affected by the input offset voltage V_{io} of the core operational amplifier:

$$\Delta V_{Ra} = V_T \ln(nm) + V_{io} = \frac{(I_1 + I_2)R_a}{(m+1)} + V_{io}. \qquad (2)$$

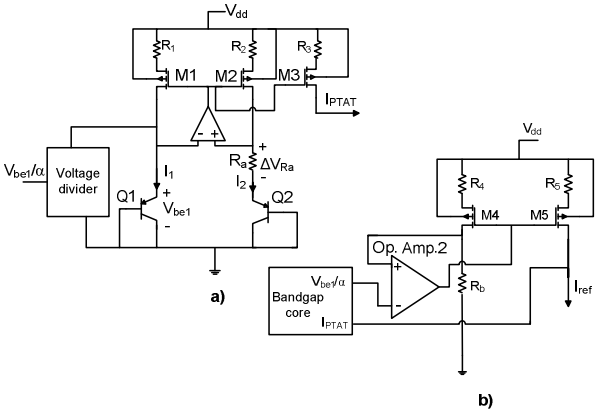

Figure 1. a) Bandgap core. b) Bandgap reference current generator.

We estimate for V_{io} a standard deviation of 0.59 mV using a single stage operational amplifier with input nMOSFETs of width W=120 μm and length L=50 μm (the offset voltage is reduced by large input nMOSFETs). On the basis of (2), in order to increase ΔV_{Ra} to make it insensitive to V_{io} without a large increase of the total current drawn from the power supply, it is important to have a small m (we choose m=2), large n (we choose n=20), and a large R_a (R_a=2.9 MΩ). The main drawback of this choice is the obvious increase of the total area occupation due to the large resistance and to the large n. We also choose α_1=1, α=4, α_2=1/6, R_b= 1.45 MΩ, obtaining ΔV_{Ra}=99.31 mV and V_{be1}/α =151.6 mV, so that the effects of the offsets of the core Op Amp and of OpAmp 2 have been estimated in a 0.39% and 0.12% relative standard deviation (RSD) of the reference current, respectively (the relative standard deviation is defined as the ratio of the standard deviation σ to the mean value μ).

Large resistances are useful to reduce the power consumption, at the price of a large area occupation. Other additional architectural choices are aimed at reducing total power consumption: for example we use single-stage operational amplifiers biased with a current of few nA, and we use a pMOS voltage divider (whose current consumption is of only few pA, negligible with respect to the bandgap core current) in order to impose only a fraction $1/\alpha$ of the V_{be1} voltage on R_b. The voltage divider consists of diode-connected pMOSFETs in series, with each well at source potential, in order not to have body effect. This solution is more complex from the architectural point of view with respect to a simple resistive divider, but leads to much lower power consumption.

It is also important to consider and to suppress the effect of mismatch in current sources, which adds to the intra-die process variability, by means of the use of large MOSFETs and source degeneration resistors. We estimate a reference current RSD of 0.31%, by considering pMOSFETs with W=100 μm and L= 50 μm, which implies σ_{Vth}=0.25 mV, and with the use of source resistors of about 100 kΩ. Also the mismatch in the voltage divider MOSFETs can be neglected, because it is responsible for an estimated RSD of V_{be1}/α of 0.066% (using pMOSFETs with W=60 μm and L= 20 μm we obtained σ_{Vth}=0.32 mV).

TABLE I. ANALYSIS OF THE EFFECT OF THE VARIOUS SOURCES OF MISMATCH ON THE REFERENCE CURRENT RSD

Variability source	**Corresponding relative standard deviation of the reference current**
Core amplifier offset	0.39%
Second amplifier offset	0.12%
Current mirrors	0.31% (worst)
Voltage divider	0.066%
pnp transistors	0.2%

The effect of mismatch of pnp transistors has been evaluated by means of a Monte Carlo analysis, obtaining a corresponding RSD of the reference current of 0.2%. We cannot perform a Monte Carlo analysis of diffusion resistors, since corresponding models are not available. The results obtained from the mismatch analysis are reported in Table I.

IV. EXPERIMENTAL RESULTS

The current generator has been realized in the UMC 0.18µm CMOS technology with the use of substrate pnp transistors and measurements have been performed on 23 packaged samples from a single batch. Its performance is summarized in Fig. 2. Chip layout is shown in Fig. 3. The chip photo is not shown because dies are passivated with dummy layers which prevent us to see circuit geometries.

The average reference current value is 54.08 nA at a nominal supply voltage of 1 V, with a standard deviation of 0.76 nA. The mean line sensitivity of the reference current is 0.21%/V by varying the power supply voltage from 0.8 V to 1.4 V, while the temperature sensitivity is 63 ppm/°C based on only one measure of the reference current from 0 to 80 °C. The current consumption is 288.84 nA when the power supply is 1 V.

Table II compares our results with the most relevant ones available in the literature. References [11] and [19] present MOSFET-based architectures, while [15] and [17] use resistors as a transconductive component. As we can note, the proposed reference current has the lowest process

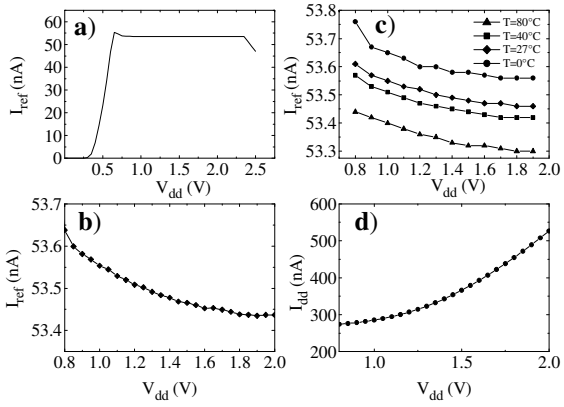

Figure 2. a) and b) Reference current I_{ref} as a function of supply voltage V_{dd}. c) I_{ref} as a function of V_{dd} for four different temperatures. d) Circuit current consumption as a function of supply voltage.

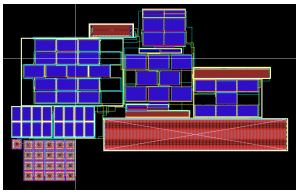

Figure 3. Chip layout (approx. 700 µm x 350 µm).

sensitivity but comparable with that of the other current generators using resistors. The advantages of the proposed solution with respect to [15] and [17] are the much lower reference current and lower power consumption. With MOSFETs it is possible to reduce the current and the power consumption maintaining a very low area occupation (see Ref. [11]), because MOSFETs can be biased in subthreshold, but the presence of the MOSFET β in the reference current expression implies a larger process sensitivity of the reference current, as we can see from Table II.

Better results in terms of process sensitivity of the reference current are obtained only introducing programmability [20], or with digital trimming [16], but this implies an additional phase of calibration after chip fabrication. Statistical results from a small but significant set of 23 samples from the same batch are reported in Fig. 4 and Fig. 5. The relative root mean square error on the standard deviation is therefore $1/\sqrt{2 \cdot 23} = 14.74\%$ .We can note that the relative standard deviation of the reference current is very good also for line voltages and temperatures far from the nominal ones. We do not have results from multiple batches, and also all results in the literature are from a single batch. However, we would like to point out that our proposed scheme is based on intrinsically more robust quantities, and therefore we expect that if multiple batches were considered the advantage of our solution in terms of accuracy would be even stronger. The main drawback of the proposed solution is the very large area occupation.

TABLE II. CURRENT GENERATOR PERFORMANCES AND COMPARISON WITH LITERATURE

	Literature references				
	[19]	***[11]***	***[15]***	***[17]***	***This work***
Techn. CMOS	3 µm	0.35µm	2 µm SIMOX	0.18 µm	0.18µm
I_{ref}	774 nA	9.14 nA	19.5 µA	7.81 µA	54.08 nA
V_{dd} *(V)*	3.5	1.5	5	1.2	0.8÷2
I_{dd}	2 µA@ 5V	36.6nA@ 1.5 V	300 µA@ 5V	27.2µA@ 1.2 V	288.8 nA@ 1 V
Temp. sens. (ppm/°C) (°C)	375 *(0÷80)*	44 *(0÷80)*	12 *(-15÷90)*	24.9 *(0 ÷100)*	63 *(0÷80)*
Line sens.(%/V)	0.013-0.015	0.0569	-	0.13	0.21
Process sens. (σ/µ)	2.58%	2.17%	1.67%	1.5%	1.4%
Area(mm²)	0.2	0.035	0.3	0.123	0.245
Variability factors	β std MOS	β std MOS	P+ resistors	Poly resistors	P+ resistors

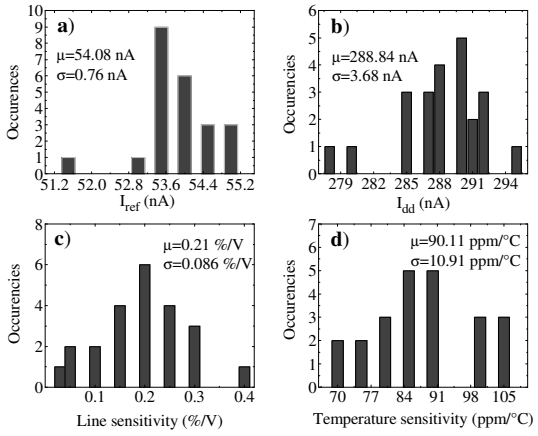

Figure 4. Distribution over 23 samples of: a) Reference current value. b) Total current consumption. c) Line sensitivity of the reference current. d) Temperature sensitivity of the reference current between 27 and 80°C (the mean value is higher than the sensitivity measured between 0 and 80 °C, due to the good circuit behavior at low temperatures).

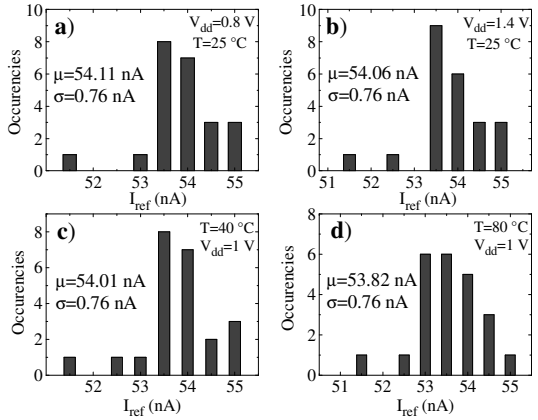

Figure 5. Distribution over 23 samples of the reference current value: a) At V_{dd}=0.8 V, T=25 °C. b) At V_{dd}=1.4 V, T=25 °C. c) At V_{dd}=1 V, T=40 °C. d) At V_{dd}=1 V, T=80 °C.

V. CONCLUSION

We have proposed a nanopower reference current generator with a low dispersion due to process variability. We have shown that very good results can be obtained with the choice of n-well diffused resistors, which are usually available in a standard CMOS technology and which are intrinsically less process sensitive than poly resistors or MOSFETs. In our case, the use of diffusion resistors in a bandgap architecture allows us to obtain a reference current very stable with respect to process variations and with a very low power consumption, especially considering results based on the same architecture. The main cost of our choices in the design space is a larger area occupation, mainly due to the large resistances, needed to reduce the power consumption of the circuit.

VII. ACKNOWLEDGMENT

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REFERENCES

[1] P. R. Kinget, "Device mismatch and tradeoffs in the design of analog circuits", IEEE J. Solid-State Circuits, vol. 40, no. 6, pp. 1212-1224, Jun. 2005.

[2] A. Abdel-Hamid, A. Anchlia, S. Mamagkakis, M. Miranda Corbalan, B. Dierickx and M. Kuijk, "A standardized knobs and monitors RTL2RTL insertion methodology for fine grain SoC tuning," in Proc. IEEE 12th Euromicro Conf. Dig. Syst. Design (DSD), Arch, Methods, Tools, Aug. 2009, pp. 401-408.

[3] A. M. Pappu, X. Zhang, A. V. Harrison and A. B. Apsel, "Process-invariant current source design: methodology and examples," IEEE J. Solid-State Circuits, vol. 42, no. 10, pp. 2293-2302, Oct. 2007.

[4] X. Zhang and A. B. Apsel, "A low-power, process-and-temperature-compensated ring oscillator with addition-based current source", IEEE Trans. Circuits Syst. I, Reg. papers, vol. 58, no. 5, pp. 868-878, May 2011.

[5] R. J. Widlar, "New developments in IC voltage regulators" IEEE J. Solid-State Circuits, vol. 6, no. 1, pp. 2-7, Feb. 1971.

[6] H. Banba et al., "A CMOS bandgap reference circuit with sub-1-V operation," IEEE J. Solid-State-Circuits, vol. 34, no. 5, pp.670-674, May 1999.

[7] E. Vittoz, "The design of high performance analog circuits on digital CMOS chips", IEEE J. Solid-State-Circuits, vol. SC-20, no. 3, pp. 657-665, June 1985.

[8] B. Razavi, Design of analog CMOS integrated circuits, Singapore: McGraw-Hill, 2001, pp. 377-381.

[9] F. Fiori and P. S. Crovetti, "A new compact temperature-compensated CMOS current reference", IEEE Trans. Circuits Syst. II, vol. 52, no. 11, pp. 724-728, Nov. 2005.

[10] C.-H. Lee and H.-J. Park, "All-CMOS temperature independent current reference", Electron. Lett., vol. 32, no. 14, pp. 1280-1281, July 1996.

[11] G. De Vita and G. Iannaccone, "A 109 nW, 44 ppm/°C CMOS current reference with low sensitivity to process variations", in Proc. IEEE ISCAS, May 2007, pp. 3804-3807.

[12] H. J. Oguey and D. Aebischer, "CMOS current reference without resistance", IEEE J. Solid-State-Circuits, vol. 32, no. 7, pp. 1132-1135, July 1997.

[13] A. Bendali and Y. Audet, "A 1-V CMOS current reference with temperature and process compensation", IEEE Trans. Circuits Syst. I, vol. 54, no. 7, pp. 1424-1429, July 2007.

[14] J. Chen and B. Shi, "1 V CMOS current reference with 50 ppm/°C temperature coefficient", Electron. Lett., vol. 39, no. 2, pp. 209-210, Jan. 2003.

[15] M. Radecker, A. Knoll, R. Kocaman, V. Buguszewicz and R. Rudolf, "A wide range temperature stable integrated current reference", in Proc. IEEE ESSCIRC, Sept. 2003, pp. 583-586.

[16] B.-D. Yang, Y.-K. Shin, J.-S. Lee, Y.-K. Lee and K.-C. Ryu, "An accurate current reference using temperature and process compensation current mirror", in Proc. IEEE A-SSCC, Nov. 2009, pp. 241-244.

[17] J. Lee and S. Cho, "A 1.4-μW 24.9-ppm/°C current reference with process-insensitive temperature compensation in 0.18-μm CMOS", IEEE J. Solid-State-Circuits, to be published.

[18] F. Maloberti, Analog design for CMOS VLSI systems, New York: Kluwer Academic Publisher, 2003, pp. 59-72.

[19] W. M. Sansen, F. O. Eynde and M. Steyaert, "A CMOS temperature-compensated current reference", IEEE J. Solid-State Circuits, vol. 23, no. 3, pp. 821-824, June 1988.

[20] G. Serrano and P. Hasler, "A precision low-TC wide-range CMOS current reference", IEEE J. Solid-State-Circuits, vol. 43, no. 2, pp. 558-565, Feb. 2008.