A 300 nW, 12 ppm/°C Voltage Reference in a Digital 0.35 µm CMOS Process

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Abstract

A voltage reference has been implemented in a standard 0.35 µm CMOS process. A temperature coefficient of 12 ppm/°C is achieved in virtue of a complete suppression of the temperature dependence of the carrier mobility. The line sensitivity is 0.46 %/V and the maximum supply current, measured at 80°C, is 130 nA. The PSSR at 100 Hz and 10 MHz is -59 dB and -52 dB, respectively.

Keywords: voltage reference, CMOS, low power.

Introduction

Voltage reference generators are fundamental in a wide variety of applications, such as switched-capacitor circuits, A/D converters, DRAM, and flash memories. Since the ever increasing diffusion of battery-operated systems assumes the availability of very low power systems, the voltage reference generator has to be "power-scaled", in order to be operated with a negligible fraction of the total power budget. In this paper we present a voltage reference, which can be implemented in a truly digital CMOS technology, based on the weighted difference between the gate-source voltages of two NMOS transistors [1,2]. The circuit has a power consumption of a few nW at most, and is characterized by a very low temperature coefficient, in virtue of an almost perfect suppression of the temperature dependence of the carrier mobility, and by a very small area occupation, due to the absence of resistors (which are otherwise common components in voltage references).

Circuit Description

The proposed voltage reference is shown in Fig. 1. It consists of a circuit that generates a bias current I_0, given by (1) below, almost independent of the supply voltage V_{DD}; I_0 is then injected into an active load (M_7-M_{10}) to generate the reference voltage. In the current generator, shown in the left half of Fig. 1, M_1 and M_2 operate in the subthreshold region, while M_3 and M_4 are in strong inversion and saturation [2]. It can be shown that the expression for I_0 is

$$I_0 = \frac{m^2 V_T^2 k_4}{2}\left(\frac{N}{N-1}\right)^2 \ln^2\left(\frac{W_2/L_2}{W_1/L_1}\right) = \frac{\mu_n C_{ox} V_T^2}{2} h \,, \qquad (1)$$

where $N = \sqrt{k_3/k_4}$ ($k=\mu_n C_{ox} W/L$), C_{ox} is the oxide capacitance, μ_n is the electron mobility, V_T is the thermal voltage, V_{th} is the threshold voltage of the NMOS transistor, and m is the subthreshold swing parameter. The active load used to generate the reference voltage consists of two NMOS transistors, M_7 and M_8, biased by I_0, and a voltage divider formed by M_9 and M_{10}. All transistors in the active load operate in the saturation region. The output voltage V_{REF} is

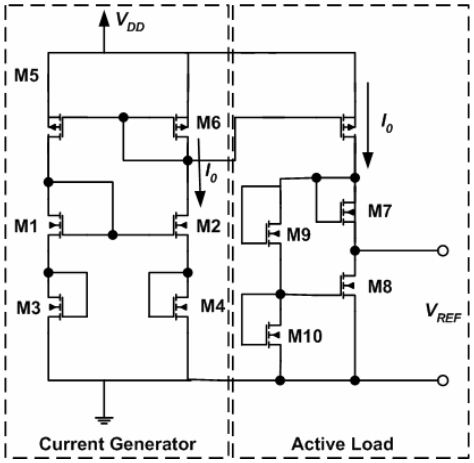

Fig. 1: Proposed Voltage Reference Circuit.

$$V_{REF} = V_{th} + \left[\frac{1}{\sqrt{k_8}}\left(1+\sqrt{\frac{W_{10}/L_{10}}{W_9/L_9}}\right) - \frac{1}{\sqrt{k_7}}\right]\sqrt{2I_0} \,. \qquad (2)$$

Most of the bias current I_0 must flow through M_7 and M_8 rather than through M_9 and M_{10}, in order to ensure the optimal temperature compensation. The use of an active voltage divider, instead of a passive resistive divider as in [2], allows the dramatic improvement of the performance of the voltage reference, in terms of power dissipation, area occupation, and temperature coefficient as well, as we will show in detail in the next sections. Indeed, since only a negligible fraction of I_0 must flow through the voltage divider, very large resistances are needed when I_0 is very small [2], resulting in a much larger area occupation than with an active divider. Conversely, for a given available area, the use of an active divider drastically reduces the minimum manageable value of I_0, and power consumption as a consequence. Even more importantly, the use of an active divider allows us to improve the temperature coefficient of the voltage reference, since two second-order effects, i.e., the body effect and the channel length modulation effect, can be cancelled. This will be discussed in the following.

Temperature Compensation

Since the threshold voltage of an NMOS transistor has an approximately linear negative dependence (with coefficient K_{t1}) on the temperature T, by differentiating (2) with respect to T we obtain that the dependence of (2) on T vanishes if the following condition is met:

$$\sqrt{\frac{W_{10}/L_{10}}{W_9/L_9}} = \frac{qK_{t1}}{k_B}\sqrt{\frac{W_8/L_8}{h}} + \left(\sqrt{\frac{W_8/L_8}{W_7/L_7}} - 1\right), \qquad (3)$$

where k_B is Boltzmann's constant and q is the electron charge. As clear from (3), the temperature dependence of the mobility is completely suppressed, and not just at the reference

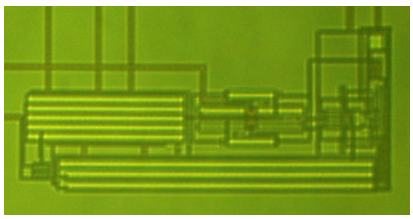

Fig. 2: Die Photograph (core).

temperature as in other solutions reported in the literature [1]. Thus, by dimensioning transistors M_9 and M_{10} according to (3), we can obtain a very low (vanishing, ideally) temperature coefficient over a wide temperature range.

We take now into account the second-order effects previously mentioned, but neglected in [2], starting with the channel length modulation effect. When (3) is fulfilled, the temperature coefficient is given by

$$\frac{\partial}{\partial T}V_{REF} \cong \frac{\lambda}{4}K_{t1}\left(2V_{th} - V_{REF}\right), \qquad (4)$$

where λ is the channel length modulation coefficient. On the other hand, when the body effect is considered and (3) still holds , the temperature coefficient is given by

$$\frac{\partial}{\partial T}V_{REF} \cong \frac{\gamma}{2}\frac{\partial \phi_f}{\partial T}\left(\frac{1}{\sqrt{\phi_f - V_{BS9}}} - \frac{1}{\sqrt{\phi_f - V_{BS7}}}\right), \qquad (5)$$

where γ is a process constant, and φ_f is the surface potential of the MOS transistor. Thus, choosing $V_{REF} = 2V_{th}$ (= 0.9 V in our case) and $V_{BS9} = V_{BS7}$, both effects on the temperature coefficient are cancelled. It is interesting to compare this favorable situation with what can be achieved with the circuit proposed in [2], where a resistive divider is used; in this case, (4) and (5) can be rewritten as (6) and (7) below, where R_1 and R_2 are the two resistances of the voltage divider:

$$\frac{\partial}{\partial T}V_{REF} \cong \frac{\lambda}{4}K_{t1}\left[\left(1+\frac{R_1}{R_2}\right)V_{th} - V_{REF}\right], \qquad (6)$$

$$\frac{\partial}{\partial T}V_{REF} \cong \frac{\gamma}{2}\frac{\partial \phi_f}{\partial T}\left(\frac{1}{\sqrt{\phi_f}} - \frac{1}{\sqrt{\phi_f - V_{BS7}}}\right). \qquad (7)$$

As clear from (7), the only way to reduce the body effect on the temperature coefficient would be to set V_{REF}=-V_{BS7} as low as possible, but still high enough to guarantee that M_8 works in the saturation region (as an example, V_{REF} was 168 mV in [2], where the impact of the body effect could be attenuated, but not cancelled). However, if a low reference voltage is chosen, the effect of the channel length modulation on the temperature coefficient, given by (6), cannot be cancelled in general, as this would require a very low value of V_{th} (which, in our case, is as high as 0.45 V). Thus, both contributions from (6) and (7) will result in a poorer temperature coefficient for the circuit in [2], compared to the solution proposed here.

Experimental Results

The voltage reference has been implemented in a standard digital 0.35 µm CMOS process. The die photograph of the core circuit is shown in Fig. 2. Fig. 3a shows the output voltage dependence on temperature, and Fig. 3b the PSRR for V_{DD}=3V. The measured temperature coefficient at V_{DD}=2 V and V_{DD}=3 V is 15 ppm/°C and 12 ppm/°C, respectively, and

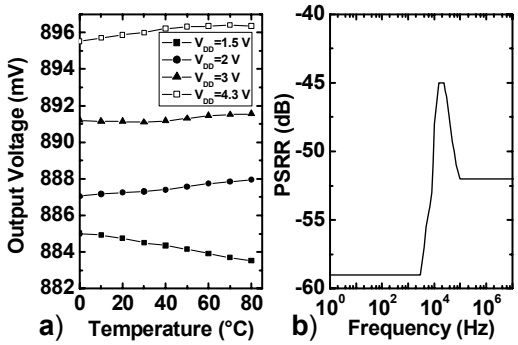

Fig. 3: a) Output voltage vs. temperature for 4 values of the supply voltage, b) PSRR at room temperature and for V_{DD}=3 V.

TABLE I: COMPARISON WITH OTHER VOLTAGE REFERENCES

	This work	Leung [1]	De Vita [2]	Leung [3]	Banba [4]
Technology	0.35 µm CMOS	0.6 µm CMOS	0.35 µm CMOS	0.6 µm CMOS	0.4 µm CMOS
Supply Voltage (V)	1.5 to 4.3	1.4 to 3	1.5 to 4.3	0.98 to 1.5	2.2 to 4.4
Supply Current(µA)	0.08@1.5 V 0.11@4.3V	<9.7	1.5@1.5V 2.4@4.3V	<18	>2.2
V_{ref}	891.1 mV	309.3mV	168 mV	603 mV	515 mV
TC (ppm/°C)	12	36.9	25	15	117
Line Sensitivity	0.46 %/V	0.08 %/V	0.95 %/V	0.73 %/V	0.21 %/V
PSRR @100 Hz @10 MHz	V_{DD}=1.5 -59 dB -52 dB	V_{DD}=1.4 -47 dB -20 dB	V_{DD}=1.5 -65 dB -57 dB	V_{DD}=0.98 -44 dB -17 dB	N.A.
Chip Area (mm^2)	0.015	0.055	0.08	0.24	0.1

increases to 18 ppm/°C at V_{DD}=4.3 V and 22 ppm/°C at V_{DD}=1.5 V. At room temperature the current drawn is 110 nA at the maximum supply voltage (4.3 V) and 80 nA at the minimum supply voltage (1.5 V). At 80 °C the absorbed current is 130 nA at 4.3 V and 90 nA at 1.5 V. The main features of the circuit are summarized in Table I, along with those of other comparable circuits available in the literature and implemented in standard CMOS processes. The voltage reference exhibits the lowest power consumption (by at least one order of magnitude), the lowest area occupation (due to the absence of resistors) and the lowest temperature coefficient, due to the neutralization of two important second-order effects. For these reasons, the proposed circuit represents a very significant improvement on [2] (in particular, the temperature coefficient has been halved), despite the apparently minor architectural changes.

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