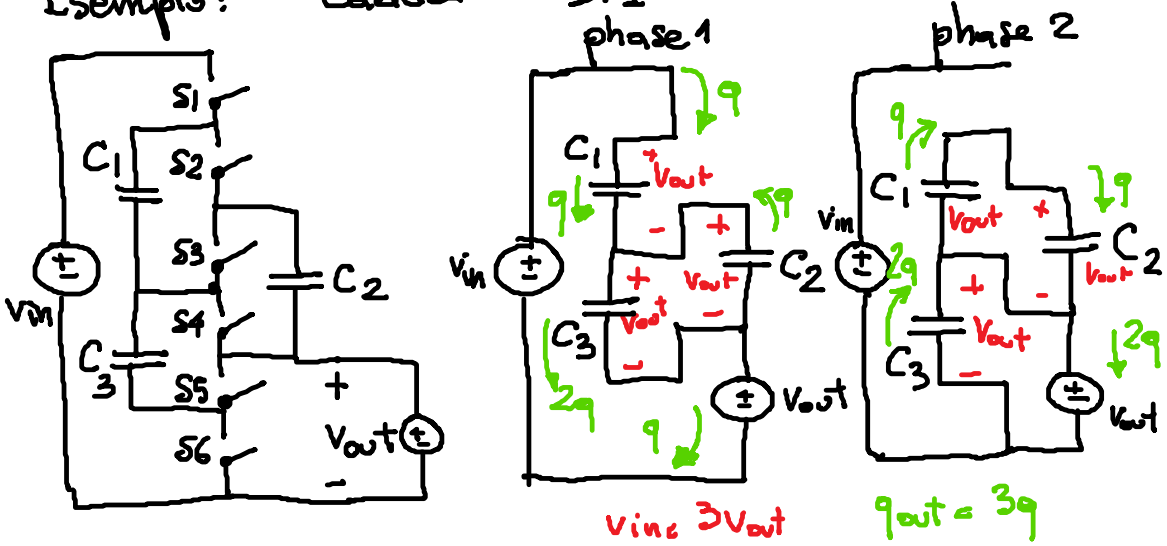
Convertitori DCDC Switched Capacitor (SC)

- inductor-less

Esempio: Ladder 3:1



- Slow Switching Limit SSL [low fs]
  - Cs reach final charge state during each phase
  - We can neglect Rs
- Fast Switching Limit FSL [high fs]
  - Capacitors' voltages do not change.

SSL

- vettori moltiplicatori di carica

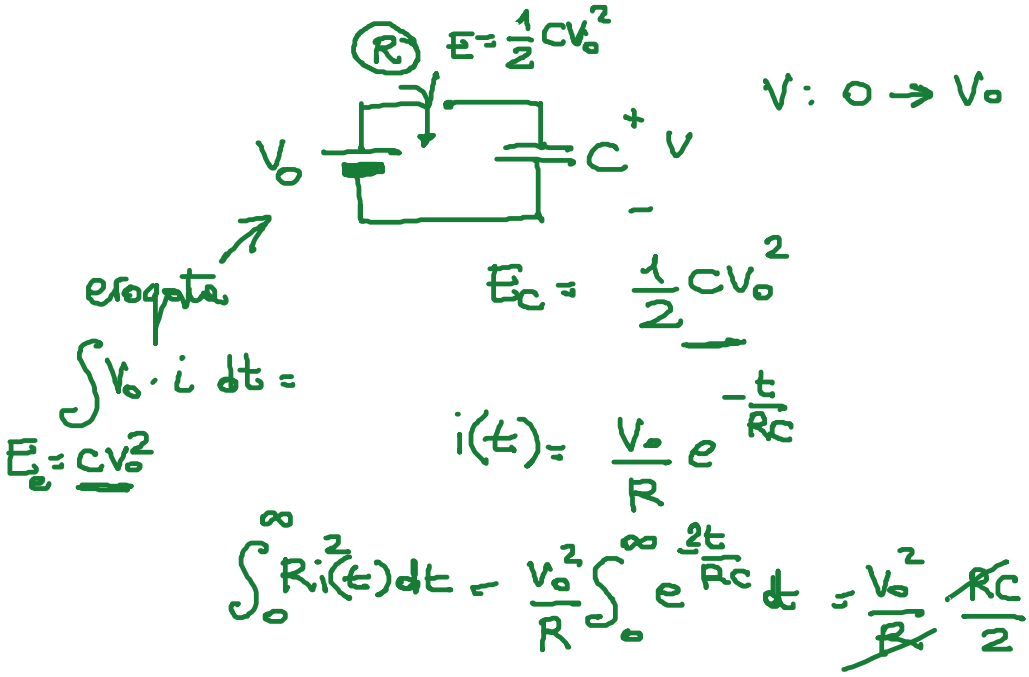
phase 1) $\vec{a}^{(1)} = \left[a_{out}^{(1)} \quad a_{c_1}^{(1)} \quad \cdots \quad a_{c_n}^{(1)} \quad a_{in}^{(1)} \right]$

↑ frazione della carica che viene fornita in uscita per ciascun periodo

per il ladder 3:1

$$\vec{a}^{(1)} = \left[\frac{1}{3} \quad \frac{1}{3} \quad \frac{-1}{3} \quad \frac{2}{3} \quad -\frac{1}{3} \right]$$

$$\vec{a}^{(2)} = \left[\frac{2}{3} \quad -\frac{1}{3} \quad +\frac{1}{3} \quad -\frac{2}{3} \quad 0 \right]$$



Teorema di Tellegen

$$\vec{v} \cdot \vec{i} = 0$$

$$V_{out} i_{out} + \sum_{i \in cap} v_{c,i}\, i_{c,i} + V_{in}\, i_{in} = 0$$

$$\begin{cases} V_{out}\, a_{out}^{(1)} + \sum_{i \in cap} v_{c,i}^{(1)}\, a_{c,i}^{(1)} + V_{in}\, a_{in}^{(1)} = 0 \\ V_{out}\, a_{out}^{(2)} + \sum_{i \in cap} v_{c,i}^{(2)}\, a_{c,i}^{(2)} + V_{in}\, a_{in}^{(2)} = 0 \end{cases}$$

$$a_{out}^{(1)} + a_{out}^{(2)} = 1 \qquad -a_{c,i}^{(1)} = a_{c,i}^{(2)}$$

$-V_{out}$ = 0 a vuoto

Sommiamo

$$V_{out} + \sum_{i \in cap} \left[v_{c,i}^{(1)} - v_{c,i}^{(2)} \right] a_{c,i}^{(1)} + V_{in} \left[a_{in}^{(1)} + a_{in}^{(2)} \right] = 0$$

$$\Delta V_{out} = V_{out} - V_{out}^{(0)} = -\sum_{i \in cap} \left(V_{c,i}^{(1)} - V_{c,i}^{(2)} \right) a_{c,i}^{(1)}$$

Ricordare l'apice (1)

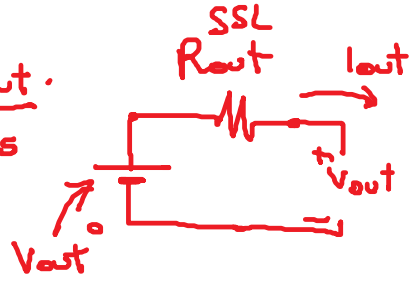
$$a_{c,i}^{(1)}\, q_{out} = \frac{a_{c,i}^{2}}{C_i}\, q_{out}$$

$$\Delta V_{out} = -\sum_{i \in cap} \frac{a_{c,i}^{2}}{C_i}\, q_{out}$$

$$q_{out} = I_{out} \cdot \frac{1}{f_s}$$

$$\Delta V_{out} = \left[-\sum_{i \in cap} \frac{a_{c,i}^{2}}{C_i f_s} \right] I_{out}$$

$$R_{out}^{SSL}$$



[min R_{out} se $C_i \propto a_{c,i}$]

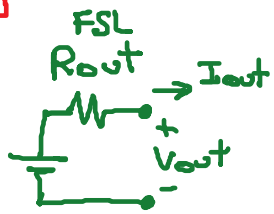
FSL

R_i resistance of switch i

vettori moltiplicatori di carica

	S1	S2	S3	S4	S5	S6
$a_s^{(1)} =$	$\frac{1}{3}$	0	$\frac{1}{3}$	0	$-\frac{2}{3}$	0
$a_s^{(2)} =$	0	$\frac{1}{3}$	0	$\frac{1}{3}$	0	$-\frac{2}{3}$

switch i $\quad i_{s,i}^{(1)} = 2\, a_{s,i}^{(1)}\, q_{out}\, f_s$



Power dissipated internally

$$P_{FSL} = \sum_{i \in switch} \frac{1}{2} R_i \left[i_{s,i}^{(1)2} + i_{s,i}^{(2)2} \right] =$$

$$= \underbrace{q_{out}^2 f_s^2}_{I_{out}^2} \underbrace{\sum_i 2 R_i \left[a_{s,i}^{(1)2} + a_{s,i}^{(2)2} \right]}_{R_{out}^{FSL}}$$

ottimizz se $w_i \propto a_{s,i}$

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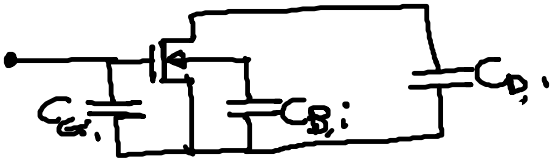
In generale $\quad R_{out} \overset{\sim}{=} \sqrt{R_{out}^{SSL\,2} + R_{out}^{FSL\,2}}$

Altre perdite

1) Switching Loss $\quad P_{SW} = f_s \sum_{i \in switch} C_{G,i} V_{G,i}^2 + C_{D,i} V_{D,i}^2 + C_B V_{B,i}^2$

$P_{SW} \propto f_s, A_{SW}$



2) Bottom plate parasitic capacitance

$P_{CAP} \propto f_s, A_{CAP}$ $\quad \Longrightarrow \quad P_{CAP} = f_s \sum_{i \in cap} C_{BP,i} V_{BP,i}^2$

3) Equivalent Serie Resistance

$$P_{ESR} = I_{OUT}^2 R_{ESR}$$

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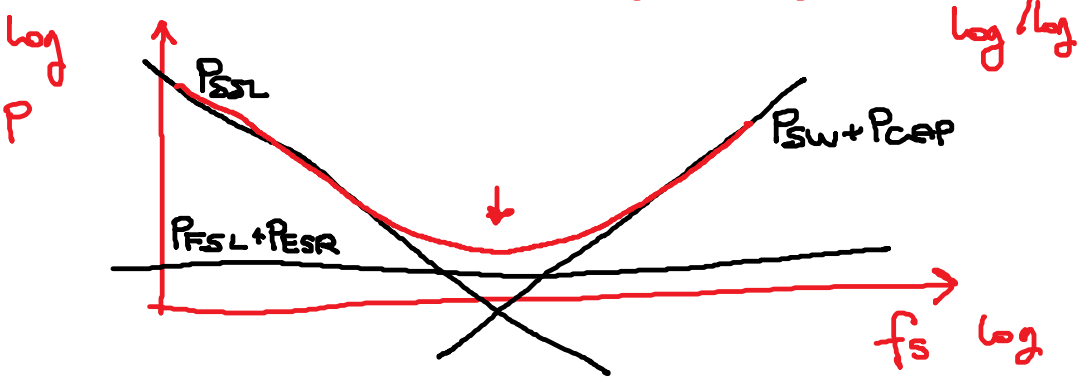
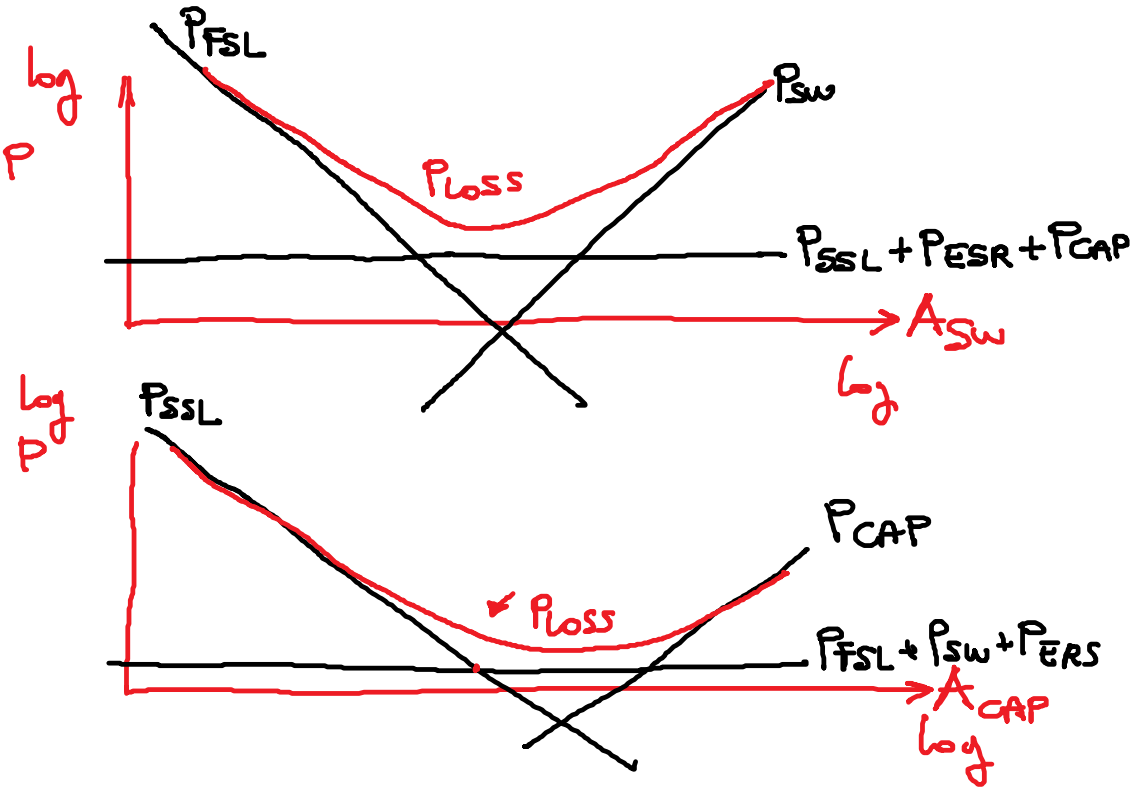
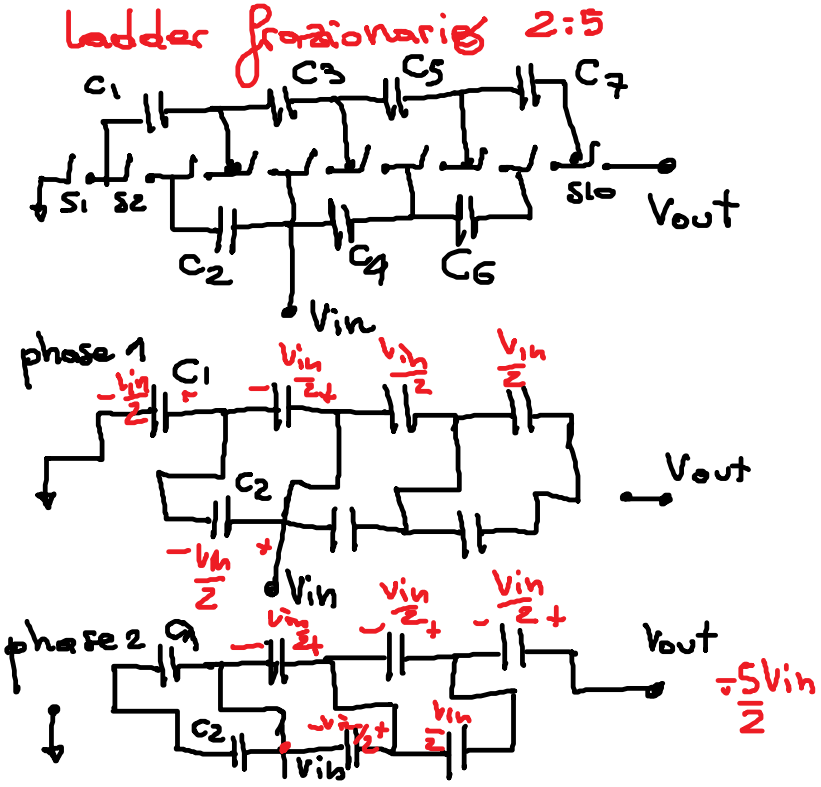
$$P_{LOSS} = \sqrt{P_{SSL}^2 + P_{FSL}^2} + P_{SW} + P_{CAP} + P_{ESR}$$

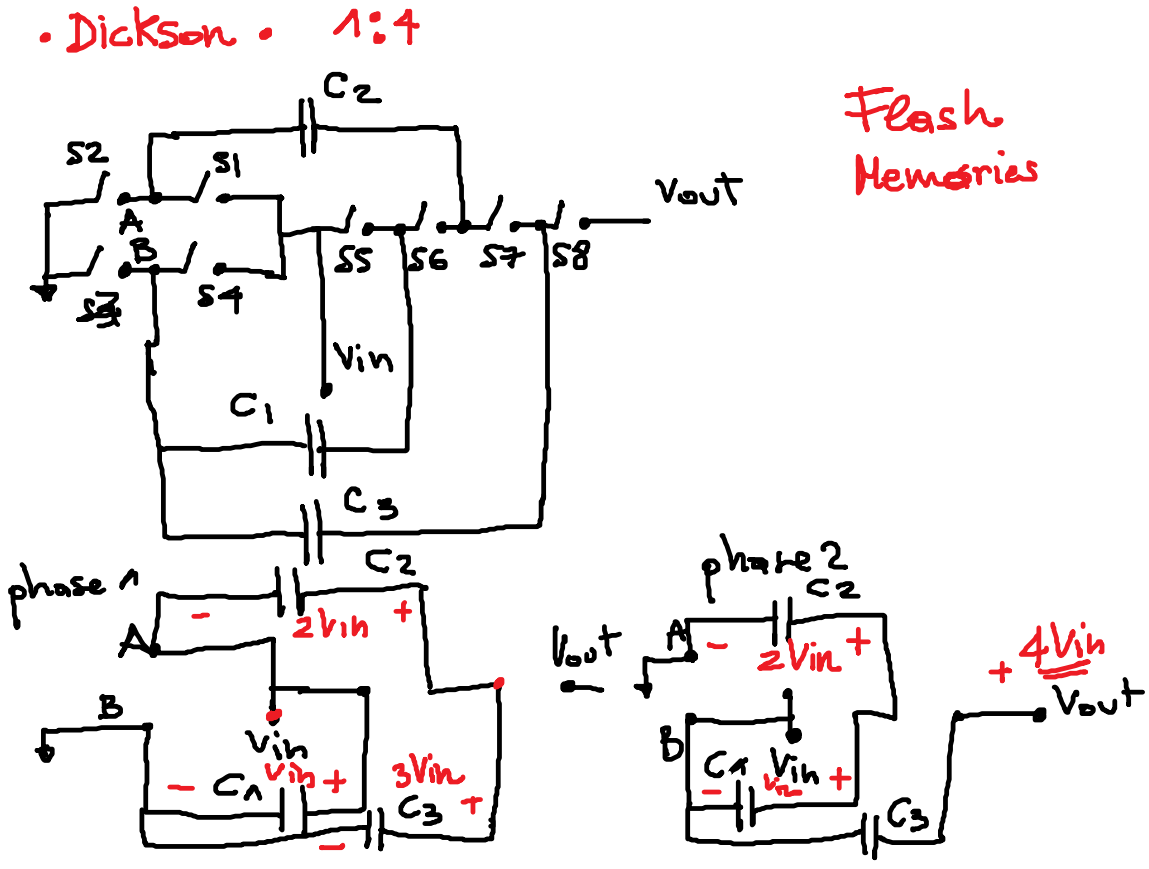
$$\eta_{\text{efficienza}} = \frac{V_{out} I_{out}}{V_{out} I_{out} + P_{LOSS}} \simeq \underline{\underline{50-90\,\%}}$$

SPAZIO DI PROGETTO : f_s, A_{CAP}, A_{SW}






Ladder frazionario 2:5
C1
C3
C5
C7
S1
S2
S10
Vout
C2
C4
C6
Vin
phase 1
phase 2
-5Vin/2


• Dickson • 1:4
Flash Memories
C2
S2
S1
A
B
S3
S4
S5
S6
S7
S8
Vout
Vin
C1
C3
phase 1
2Vin
3Vin
phase 2
4Vin